Fabrication of three-terminal resonant tunneling devices in silicon-based material

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Laterally gated three-terminal resonant tunneling devices have been fabricated from $Si/Si_{1-x}Ge_x$ double-barrier structures grown by atmospheric pressure chemical vapor deposition. The gate is insulated from the submicrometer vertical channel by a low-temperature oxide and the entire fabrication scheme is compatible with current silicon technology. At $T=77$ K the resonant peak current can be modulated by 25% by applying a moderate gate voltage; at $T=4.2$ K, current modulation reaches 50%. We present calculations demonstrating that devices fabricated from optimized $Si/Si_{1-x}Ge_x$ structures will pinch off fully at moderate gate voltages and operate at liquid nitrogen temperatures.

Semiconductor nanostructures attainable by modern epitaxial and lithographic techniques are expected to give rise to new quantum electronic and optoelectronic devices that will push semiconductor technology beyond the limits of large-scale integration. Among the various quantum-effect structures created in the laboratory, few have been as intensively studied as the double-barrier resonant tunneling structure (DBRTS), originally fabricated by Chang, Esaki, and Tsu in 1974.[1] In recent years, literally hundreds of articles describing the incorporation of the DBRTS and its variants into semiconductor devices have been published.[2] Yet, in the vast majority of these publications the DBRTS is utilized essentially as a two-terminal device inserted in a larger circuit, while reports of three-terminal DBRTS realizations have been few. The first attempts to laterally gate a DBRTS with a rectifying Schottky gate deposited directly on n-GaAs/AlGaAs material were reported by Kinard *et al.*,[3] who observed a small reduction of the resonant current with gate voltage V_g. More recently, two groups applied the same technique to smaller, higher-quality DBRTS[4,5] and fabricated devices that could be pinched off at liquid-helium temperatures by gate voltages $V_g \leqslant -3$ V. In addition, there have been several attempts to fabricate a DBRTS in the plane of a modulation-doped heterostructure with potential barriers produced by the biasing of nanolithographic gates,[6–8] but the relatively low and wide barriers created by this technique have led to smeared current-voltage (I-V) characteristics compared to epitaxially grown vertical DBRTS.

Recent advances in the epitaxial growth of $Si/Si_{1-x}Ge_x$ heterostructures have opened new possibilities for the fabrication of Si-based DBRTS.[9–12] In addition to the intrinsic interest of transferring heterostructure band-gap engineering to silicon, the advantages of silicon processing technology and usable oxides confer the opportunity to modify and improve DBRTS devices. In this report we present the first realization of a laterally gated, vertical, submicrometer p-type $Si/Si_{1-x}Ge_x$ DBRTS with an oxide-insulated gate electrode, where the resonant peak current can be reduced by 25% by applying a fairly low $V_g=1.5$ V at $T=77$ K. Further, at $T=4.2$ K the device can be operated in enhancement mode and current modulation between $V_g=-1.2$ V and $V_g=1.2$ V reaches 50%. While the application of higher gate voltages and complete device pinch off are hindered by gate leakage currents in these early devices, we also demonstrate that improved DBRTS design, reduction of the lateral extent of the device, and more controlled oxide deposition should result in three-terminal resonant tunneling devices with fully transistor-like low voltage operation.

The starting material for our devices consisted of a wafer of p-type $Si/Si_{1-x}Ge_x$ DBRTS grown by atmospheric pressure chemical vapor deposition on a standard p-Si substrate. The details of the epitaxial growth and DBRTS design have already been published.[13,14] In this wafer the undoped active region consisted of a narrow ~35 Å $Si_{0.75}Ge_{25}$ well clad by ~40 Å Si barriers, with the double-barrier structure in turn clad by undoped ~225 Å $Si_{1-x}Ge_x$ spacer regions in which the Ge content was gradually graded down from $Si_{0.75}Ge_{25}$ to pure Si. As a result, holes tunnel from a $Si_{0.75}Ge_{25}$ emitter region into a narrow $Si_{0.75}Ge_{25}$ well through a Si barrier. The nominal difference from the DBRTS of Ref. 14 was the reduction of the barrier thickness with the aim of increasing current density in submicrometer devices.

The fabrication sequence of the three-terminal DBRTS devices is illustrated in Figs. 1(a)–1(e). Using electron-beam lithography and lift off we deposited Ti/Al contact metal in the form of squares ranging from $D=20$ μm to $D=2000$ Å on the side. Then, a low-damage[15] electron-cyclotron resonance (ECR) plasma reactive ion etching processing using $CBrF_3$ and SF_6 was employed to etch device pillars through the active DBRTS region using the contact metal as a mask—the etch was calibrated to produce an undercut, as shown in Fig. 1(a). The gate oxide was deposited at 250 °C from silane and high-purity O_2,[16] conformally covering the metal-capped $Si/Si_{1-x}Ge_x$ pillar, and 500 Å of Ti/Al gate metal were deposited in a self-aligned manner, as shown in Fig. 1(b). A second, much thicker low-temperature oxide deposition completely buried the device. This layer was planarized by polishing and then etched back in the ECR

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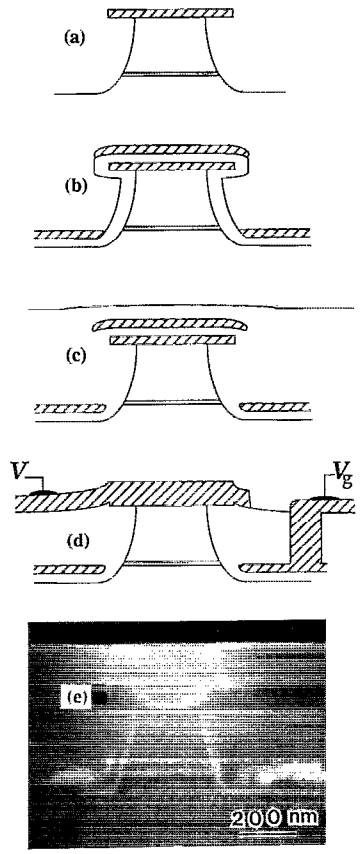

FIG. 1. Schematic fabrication sequence for the laterally gated $Si/Si_{1-x}Ge_x$ double-barrier resonant tunneling structure: Hatched regions are metal, the double-line indicates the active double-barrier region (not to scale). (a) After electron-beam lithography, contact metal lift off, and electron-cyclotron plasma reactive ion etching; (b) after gate oxide and self-aligned gate metal deposition; (c) after thick oxide deposition, planarization, and partial etchback; (d) after metal pad deposition—source-drain V and gate V_g biasing is with respect to the backside substrate contact (not shown); (e) cross-sectional SEM photograph after partial etchback, to be compared with (c).

machine using CF_4 and O_2 until the top contact metal was exposed—see Fig. 1(c) for an intermediate point in the etchback process. Finally, optical lithography, wet etching and metal liftoff were employed to connect the gate and the top contact to pads, as shown in Fig. 1(d). Figure 1(e) shows a cross-sectional scanning electron-microscopy (SEM) photograph through a nominally 3000 Å wide metal line that was located in the immediate vicinity of the submicron devices and underwent identical processing steps—compare with Fig. 1(c).

The $T=77$ K depletion mode operation of a $D=2000$ Å DBRTS device is shown in Fig. 2(a). At $V_g=0$ the source-drain (I-V) characteristic exhibits a resonant peak at $V_p\sim570$ mV with a peak-to-valley ratio of 1.5, corresponding to holes tunneling through the lowest-lying light-hole subband in the well (at this temperature the heavy-hole resonances in this material show up weakly in the conductance—for a discussion of heavy- and light-hole tunneling resonances in $Si/Si_{1-x}Ge_x$ DBRTS see Ref. 14). By applying a positive bias V_g to the gate electrode we deplete the vertical channel from the side and reduce the current scale of the

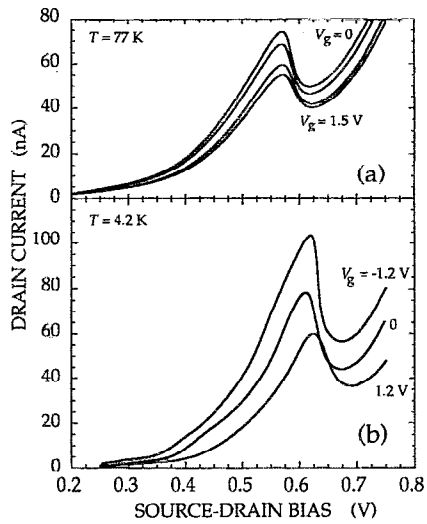

FIG. 2. (a) (I-V) characteristics of a laterally gated DBRTS of nominal $D=2000$ Å at $T=77$ K vs gate bias $V_g=0$, 0.5, 1.0, and 1.5 V. (b) (I-V) characteristics of the same device at $T=4.2$ K and $V_g=0,\pm1.2$ V.

source-drain (I-V), while the (I-V) line shape remains essentially unchanged—see Fig. 2(a). At $V_g=1.5$ V the peak current is reduced by ~25%. Increasing V_g further at $T\Rightarrow77$ K, however, results in unacceptable gate leakage currents, as does operating the device in enhancement mode ($V_g<0$). At $T=4.2$ K the gate leakage problem is less severe and the device can be operated in both depletion and enhancement modes. This is illustrated in Fig. 2(b), where we show the source-drain (I-V) at $V_g=0$, and ±1.2 V. The resonant peak current at $V_g=-1.2$ V is almost a factor of 2 larger than at $V_g=1.2$ V.

While the gated (I-V) characteristics of Fig. 2 unambiguously demonstrate the three-terminal transistor-like operation of our $Si/Si_{1-x}Ge_x$ DBRTS device, there is a clear need for improving the design and fabrication process to produce devices that can be fully pinched off without sizable leakage currents. An obvious focus for improvement is the low-temperature gate oxide deposition process, which should permit the application of higher gate voltages.[16] Yet even in the low gate voltage regime $|V_g|<2$ V, our numerical simulations show that full depletion should be achievable by altering the DBRTS active region design. Consider the simplified model of the active region shown in the inset of Fig. 3. Essentially, the gated DBRTS device consists of heavily p-doped electrodes, where the gate bias-induced depletion is small, and the undoped active region of total length L—barriers, well, and undoped ~225 Å $Si_{1-x}Ge_x$ spacer regions outside the barriers—where the depletion is larger and is essentially limited by the p-doped regions. Clearly, the effectiveness of the gate depends strongly on L: The side depletion in the active region increases with L and hence complete pinch off should arrive at a lower gate bias. We have calculated the depletion and hence the diameter of the electrically active channel in the plane of the well in a $D=2000$ Å device [the calculation used a cylindrical channel with an effective diameter of 2400 Å, since ECR etching

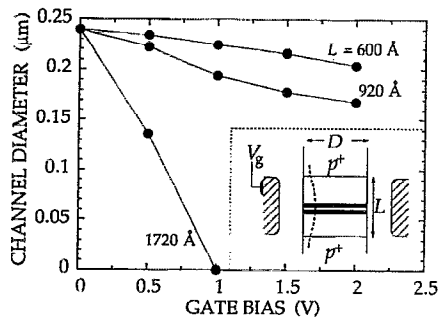

FIG. 3. Calculated diameter of the electrically active vertical channel vs gate bias V_g for different values of nominally undoped active DBRTS region length L (at $V_g=0$ channel diameter ~2400 Å for nominal device size $D=2000$ Å). Lines connecting the points are guides to the eye. Inset shows a schematic cross section through the device, dashed line indicates the equipotentials For the device in Fig. 2 $L\sim600$ Å.

smoothes the square corners of the original metal contact and the diameter of the pillar in the plane of the well is larger than the nominal contact metal pad—see Fig. 1(e)]. The following parameters and simplifying approximations were employed: Gate oxide thickness of 600 Å; p doping of 5×10^{18} cm^{-3} in the electrodes; $Si/Si_{1-x}Ge_x$ valence-band offset of $0.8x$ in eV (valid for the $x\leqslant0.25$ Ge contents of our layers[17]); vertical symmetry about the plane of the DBRTS well (this assumes the 500-Å-thick gate electrode is perfectly aligned with the active region, see inset of Fig. 3); gate leakage and the source-drain bias set to zero. The boundary of the electrically active channel was taken as the point where the calculated potential exceeded the Fermi level by $3kT\sim20$ meV (at $T=77$ K). The results are shown in Fig. 3 for $0\leqslant V_g\leqslant2.0$ V and $L=600$, 920, and 1720 Å: The first value corresponds to the DBRTS design reported in this letter, the second represents the approximate critical thickness limit[18] on our structure with Ge content $x\leqslant0.25$, while the last value would require redesigning the DBRTS with lower Ge content in the well and spacer regions. We find that for $L=600$ Å the vertical channel diameter is only reduced ~250 Å at $V_g=1.5$ V, predicting a current reduction of ~20%—in reasonable agreement with the experimental result shown in Fig. 2. For $L=920$ Å the channel diameter is reduced ~600 Å at $V_g=1.5$ V; while for $L=1720$ Å full pinch-off is achieved at $V_g\geqslant1.0$ V. Consequently, a redesigned DBRTS with increased undoped spacer regions accompanied, if necessary due to critical thickness considerations, by reduced Ge content in the $Si_{1-x}Ge_x$ layers should result in improved three-terminal resonant tunneling characteristics, including complete pinch off at low to moderate V_g (thicker Si barriers could be used to compensate for reduced barrier heights). Finally, since the gate-induced sideways depletion of the vertical channel remains unchanged to first order as the channel diameter D is decreased, fabricating devices with $D<2000$ Å should also reduce the gate voltage required for complete pinch off.

In conclusion, we have fabricated the first laterally gated Si-based double-barrier resonant tunneling device and demonstrated its three-terminal operation. Our calculations indicate that by improving the quality of the deposited gate oxide and optimizing the double-barrier structure to promote more effective sideways depletion of the vertical channel, our approach should result in devices that would pinch off completely at moderate gate voltages and operate at liquid-nitrogen temperatures.

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