# Double-Gate MOSFETs: Is Gate Alignment Mandatory?

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## Abstract

*Double-gate (DG) MOSFETs promise to enhance transistor capabilities beyond the limits of conventional CMOS technology. In this paper, we study for the first time the impact of gate misalignment in "non-ideal" DG devices that may be much easier to fabricate than self-aligned versions.*

*Drain current, transconductance, series resistance effects, subthreshold slope and carrier concentration profiles are simulated for different architectures, based on a 50nm long SOI MOSFET. We compare single gate, ideal aligned DG, and non-aligned DG transistors in which unequal gate lengths are used to compensate for the gate misalignment. We find that non-aligned DG devices are competitive with and even, in some cases, superior to ideal DG MOS, albeit with unusual $g_m$ curves.*

## 1. Introduction

The main difficulty in manufacturing DG MOSFETs is to maintain the front and back gates self-alignment while aggressively reducing the device dimensions. DG processes proposed so far are extremely complicated [1,2,3]. The technology can be greatly simplified if some degree of misalignment is tolerated. In this paper, we examine the impact of gate misalignment on DG device characteristics. We compare the simulated characteristics of several transistors: a single-gate (SG) 50nm MOSFET (Fig.1-a), an ideal aligned DG MOSFET with two 50 nm gates (Fig.1-b), and non self-aligned DG MOSFETs with 50nm and 100nm gates [4]. The latter were studied in six different configurations:

100nm front-gate ($G_1$), 50nm back-gate ($G_2$), with various gate offsets (Fig.1-d,e,f).

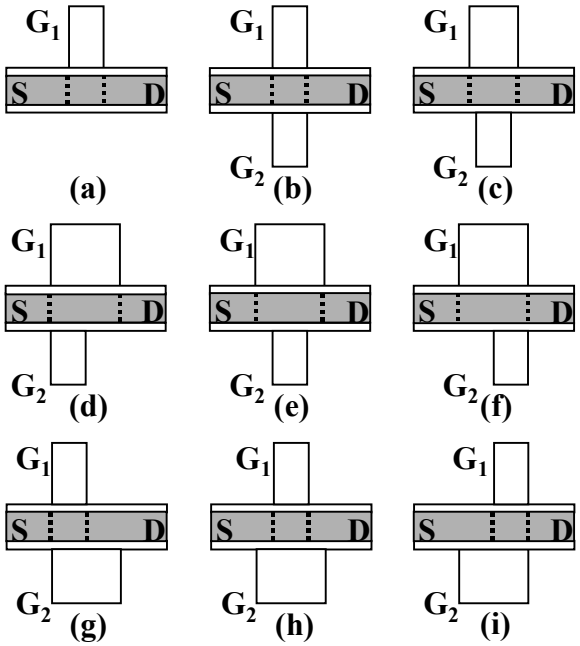


Figure 1. The different architectures.

50nm front-gate, 100nm back-gate, with various gate offsets (Fig.1-g,h,i).

Another $G_1$=70nm transistor (Fig.1-c) was also simulated. All our transistors have a 12nm thick Si film (i.e. negligible quantum effects), n-poly Si gates, 2nm gate oxides, undoped channel, and elevated source (S) and drain (D) regions. A maximum 25nm offset is assumed, corresponding to state-of-the-art e-beam overlay accuracy. The front gate is the one used for self-aligned S/D implantation (Fig. 2) and thus determines the effective S/D length of our transistors (diffused doped regions reach the front gate edges, represented by dashed lines in Fig.1). All the simulations were carried out using the Athena and Atlas modules of Silvaco.

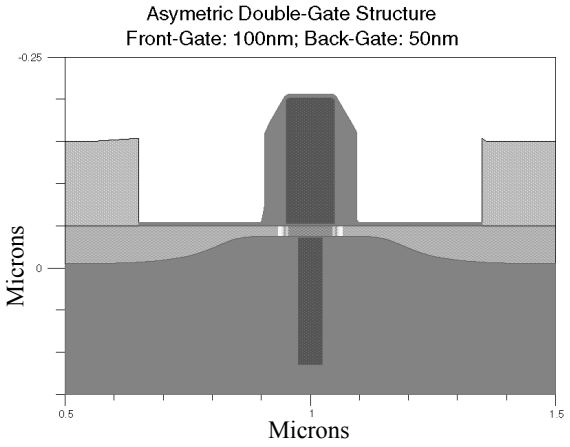


Figure 2. Example of structure 1-e.

## 2. Static I(V) Characteristics

Figure 3 shows the simulated $I_D(V_G)$ characteristics of different devices for $V_D$=1V. As can be expected, all DG devices have much better subthreshold slopes (60mV /decade) and provide more current drive than the regular single-gate 50nm transistor. Devices (d,e,f) have a longer effective channel, and therefore lower current and transconductance. The DIBL and field encroachment effects are almost nonexistent in thin DG MOSFETs.

A striking feature is that the highest current is not produced by the ideal aligned DG transistor 1-b, as one might expect, but rather by transistor 1-h.

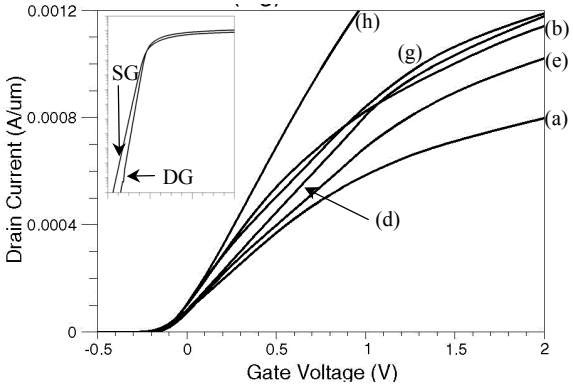


Figure 3. $I_D(V_G)$ curve for $V_D$=1V, inset shows subthreshold slope.

This can be explained by the effect of source series resistance, which is lower in transistor 1-h because of charge accumulation in the source region produced by the back-gate voltage. By contrast, transistor 1-g does not benefit from this effect because there is no overlap of the source and back-gate. Further, misaligned transistors 1-d and 1-g outdrive the aligned 1-b device at higher $V_G$ because of a higher transconductance that will be discussed later.

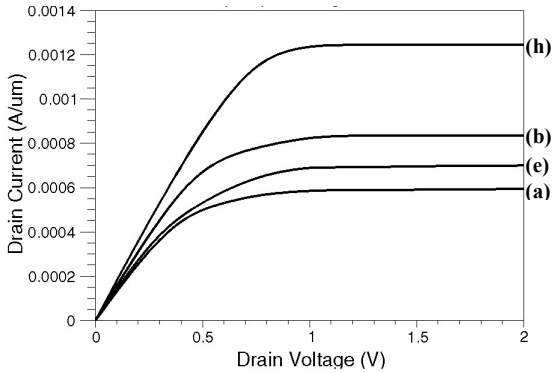


Figure 4. $I_D(V_D)$ for $V_G$=1V.

The $I_D(V_D)$ curves at $V_G$=1V, shown in Fig. 4, explicitly demonstrate the current drive advantages of aligned (centered) DG devices. The gain in saturation current over the SG 50nm MOSFET is ~17% for DG

device 1-e, ~39% for 1-b, and ~110% for 1-h (Table 1).

## 3. Transconductance

Gate misalignment further changes the shape of the transconductance $g_m$, shown in Fig. 5. Again, device 1-h has the highest $g_m$. We focus on the importance of gate misalignment for $g_m$ in Figs. 6 and 7, where devices 1-d, 1-e, 1-f and 1-g, 1-h, 1-i are compared, respectively.

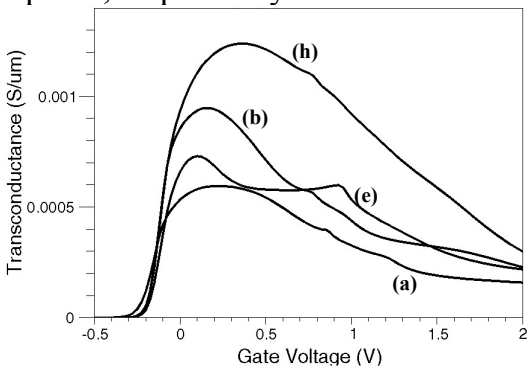


Figure 5. Transconductance for $V_D$=1V for various structures.

Our transconductance model includes two key mechanisms: influence of series resistance and coupling between front and back channels. The carrier profiles across the 12nm Si film show significant volume inversion, at least in weak and moderate inversion (Fig.8). In strong inversion we can assume two separate inversion layers controlled by the front and back-gate.

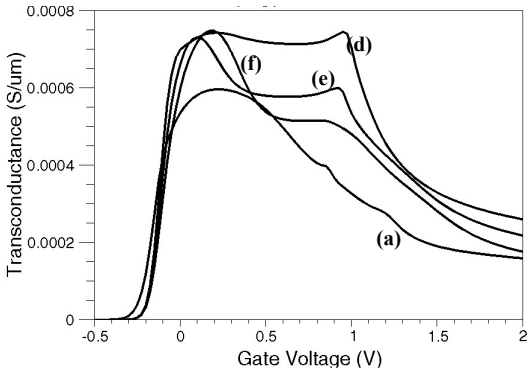


Figure 6. Transconductance for $V_D$=1V for devices 1-d, 1-e and 1-f.

The $g_m$ of DG devices comes from a superposition of these two terms. The double-peaked $g_m$ structure observed in many devices arises because front and back-gate terms peak at different $V_G$ and differ in magnitude due to source series resistance $R_S$. Indeed the effective $V_T$ for the two gates in non-symmetric structures is different, at least at large $I_D$. This is clearest in Fig. 6, where the front-gate is wider, so the source implantation does not reach the back-gate in devices 1-e and 1-f, leading to ever larger $R_S$ as one goes from 1-d to 1-f. As a result, the back-gate term (second peak) in the $g_m$ becomes progressively smaller.

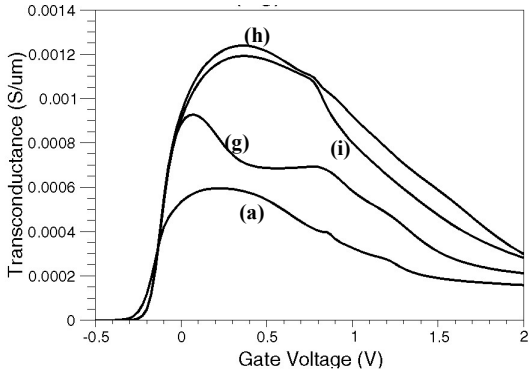


Figure 7. Transconductance for $V_D$=1V for devices 1-g, 1-h and 1-i.

By contrast, in Fig. 7, the devices have a smaller front-gate (and effective gate length) and $R_S$ of devices 1-h and 1-i is drastically reduced by the charge accumulation in the source region due to the back-gate. As a result, neither term contributing to $g_m$ is reduced or strongly shifted along the $V_G$ axis due to $R_S$, resulting in a large, *single* $g_m$ peak. Somewhat counterintuitively, device 1-g does have some $R_S$ (since back-gate accumulation in the source does not help here) and hence retains the double-peaked $g_m$ line shape. Our explanation is consistent with the disappearance of the double-peaked $g_m$ from all structures when $I_D$ is

small ($V_D$=50mV). In this case, the maximum is reached for structures 1-h and 1-i.

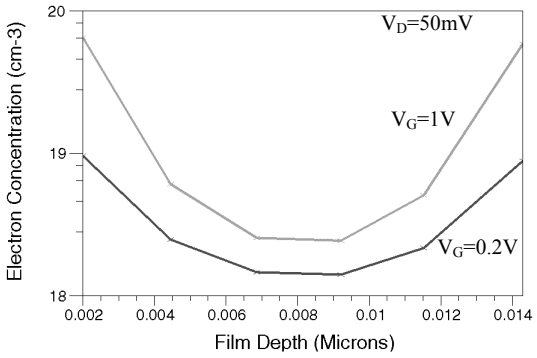


Figure 8. Electron concentration profile in the middle of device 1-e.

## 4. Dynamic considerations

Further ac simulations are necessary to check whether the current drive gains obtained in DG devices under static conditions are not negated by the higher capacitances expected in some of the DG structures (particularly 1-g, 1-h, and 1-i, where the smaller front-gate leads to overlap between the S/D implanted regions and the back-gate). We carried out a preliminary small signal simulation to extract the gate capacitances for the various proposed architectures. The results shown in the last line of Table 1 represent the total gate capacitance of DG MOSFETs.

## 5. Conclusions

The main point of this paper is that asymmetric non-self-aligned double-gate transistors not only provide superior performance to a single-gate MOSFET with the same gate length, but can be comparable to or, in some regards, superior to ideal self-aligned double-gate devices. These non-self-aligned DG devices, which ensure gate overlap by using unequal gates [4], may be considerably easier to fabricate in the planar mode, without recourse to difficult selective epitaxy.

Table 1. Summary of main results.
All results are **normalised** with respect to device **1-a.**

| Structures | 1-a | 1-b | 1-d,e,f | 1-g,h,i |
|---|---|---|---|---|
| **normalised** $I_{Dsat}$ for $V_G$=1V | 1 | 1.39 | 1.4 (d)<br>1.17 (e)<br>1.12 (f) | 1.42 (g)<br>2.1 (h)<br>2 (i) |
| **normalised** $g_m$ peak for $V_D$=1V | 1 | 1.58 | 1.25 (d)<br>1.22 (e)<br>1.25 (f) | 1.55 (g)<br>2.1 (h)<br>2 (i) |
| **normalised** Total gate capacitance | 1 | 2.1<br>2 gates | 2.8 (e)<br>2 gates | 2.8 (h)<br>2 gates |

## 6. Acknowledgements

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## 7. References

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