Double-Gate MOSFETs: Performance and Technology Options

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The advantages of double-gate (DG) SOI MOSFETs over conventional, single-gate transistors are described in terms of performance and potential for ultimate scaling. The peculiarity of DG-MOSFETs is that the top and bottom gates are biased simultaneously to establish equal surface potentials: $V_{G2} = V_{G1}$ for identical gate oxides, or $V_{G2} = V_{G1}(t_{OX2}/t_{OX1})$ to compensate for the difference in front and back oxide thickness. In fully depleted transistors with a thin enough film, controlling the channel from both sides, forces most of the carriers to flow in the middle of the film, according to the volume inversion concept [1]. Volume inversion results in excellent properties, which will be reviewed in this paper. In particular, the carrier mobility is enhanced, so that the transconductance in double-gate mode exceeds twice the value observed in single-gate mode. A DG-MOSFET is more than the sum of two classical transistors.

An efficient DG fabrication process should allow for variable transistor width and ultra-short channel, with a uniform Si film thickness, low series resistance, and an ultra-thin film. Different approaches, already demonstrated, will be discussed:

- **Delta structure.** The Si film is etched and a very narrow island is isolated. After oxidation, the gate is deposited (Fig. 1(a)). The conduction is horizontal, however the Si membrane and the inversion charge sheet have a vertical configuration [2]. Other solutions exist for preparing vertical membranes, like the Fin-gate MOSFET (Fig. 1 (c)) [3]. Extremely short devices (20 nm) can be fabricated with perfect alignment of the two gates. However, the transistor width, which controls the total current, is limited by the film thickness (0.1–0.2 μm).
- **Gate-All-Around (GAA) structure.** This device has a planar configuration. The body of the GAA transistor consists in a Si membrane, which is formed by etching a cavity in the BOX (Fig. 1 (b)) [4]. The technology is relatively simple and the gates are self-aligned. The critical issue is to achieve a thin enough Si membrane.

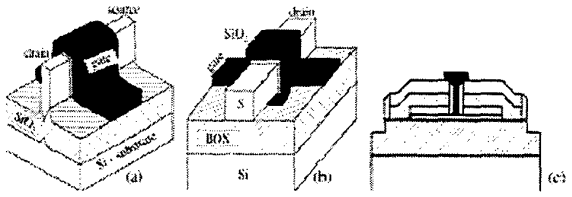

Fig. 1: Schematic illustrations of delta structure (a), gate-all-around (GAA) (b), and Fin-gate (c) MOSFETs.

- **DG-MOSFET by epitaxial lateral overgrowth (ELO).** The Si film is oxidized and patterned (Fig. 2(c)), then a poly-Si back gate is deposited and oxidized. Single-crystal Si is grown from a nearby seed and planarized [5]. The critical problem is the film thickness (100 nm) and the alignment of the two gates.
- **Bonded DG-MOSFET.** The transistor body is defined from a bulk-Si wafer by LOCOS isolation (Fig. 2d)). After gate oxidation, a back gate is deposited and the oxidized structure is bonded to a "passive"

wafer. The back of the initial, "active" wafer is etched off, the LOCOS oxide serving as an etch-stop. After turning the structure upside-down, the front oxide and gate are processed [6]. The weak points are the gate alignment and the accuracy of the LOCOS thickness.

- **Horizontal DG-MOSFET with epitaxially deposited source and drain.** The challenge of this process is to achieve a free standing ultra-thin membrane from an SOI substrate, by either tunnel epitaxy [7] or a SiGe intermediate sacrificial layer [8]. Both fabrication sequences are very complex. Once the body membrane, and the top/bottom gates are completed, the source and drain regions are deposited epitaxially (Figs. 2a) and (b)).

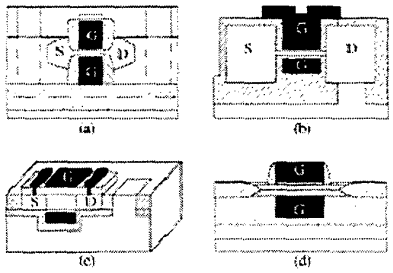

Fig. 2: Various architectures for double-gate (DG) SOI MOSFET.

We believe that other technological processes will be developed in the future. In general, it is assumed that an ideal DG MOSFET must be symmetrical, with mandatory self-aligned front and back gates. Such a device is difficult to fabricate. To circumvent this problem, we have explored the possibility of a slight misalignment of the gates [9], compensated by an increase of the back gate length [6]. The simulation of the asymmetrical DG transistors shown in Fig 3 shows excellent performance: ideal subthreshold slopes (60 mV/dec at 300K), higher drain saturation current and better transconductance than in symmetric DG-MOSFETs. These results will be explained in detail.

Figure 3. Asymmetrical DG with 50 nm front gate and 100 nm back gate.
Back gate can be centred (a), shifted towards the drain (b), or towards the source (c).

In conclusion, we expect the double-gate SOI transistor to succeed beyond the frontiers of the conventional CMOS. More research is needed to complete and fully understand the device characteristics, and to optimize the technology. Some degree of asymmetry is acceptable for relaxing the process constraints.

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