Double-Gate SOI MOSFETs with Asymmetrical Configuration

F. Allibert[1,2], A. Zaslavsky[3] and S. Cristoloveanu[1]
(1) Laboratoire de Physique des Composants à Semiconducteurs (UMR CNRS & INPG) ENSERG, BP 257, 38016 Grenoble Cedex 1, France
(2) SOITEC S.A., Chemin des Franques, Bernin, 38926 Crolles, France
(3) CEA-LETI, 17 rue des Martyrs, F-38054 Grenoble Cedex 9, France
E-mail : frederic.allibert@cea.fr, Tel. : 33-438-789-403

Introduction. Double-gate (DG) MOSFETs are attracting interest as "perfect" devices for the last stages of Si microelectronics. Current technology and modeling efforts are focused on ideal DG-MOSFETs with one surrounding gate or two symmetrical gates [1-3]. However, no sufficiently simple process to achieve ideal structures has been demonstrated to date. DG-SOI technology constraints can be greatly relaxed if some degree of gate placement asymmetry is acceptable. We have recently shown that such gate asymmetry can actually improve the current drivability and transconsductance [4]. In this paper, we investigate additional features, performance (parasitic capacitances, switching capability, etc) and applications of slightly asymmetric DG-MOSFETs.

Device architecture. In asymmetric DG MOSFETs (Fig. 1), the channel length (50nm or less) is defined by the front gate, while the back gate is longer [5, 6]. This difference in length compensates for the misalignment Δ of the two gates. The offset parameter is $\Delta = 0$ for ideally aligned gates, $\Delta < 0$ for a front gate shift towards the source and $\Delta > 0$ for opposite shift (Fig. 1, Table 1).

The simulated structure takes into account the key constraints involved in the fabrication (based on wafer bonding) and operation of realistic DG-MOSFETs: ultra-thin SOI film (12nm, free of quantum effects) to develop volume inversion, planar SOI technology, low channel doping (high mobility), elevated source/drain (S/D) regions (low series resistance), ultra-short channel (the front gate and spacers are used for self-aligned S/D implantation), and thin 2nm gate oxides. The gate material is n^+ poly-Si. Simulations were perfomed using Silvaco Athena and Atlas. Asymmetric devices are compared to the ideal DG (both gates 50nm, $\Delta = 0$) and conventional 50-nm-long single-gate (SG) MOSFETs.

Results and discussion. All simulated asymmetric devices demonstrated static characteristics comparable or even superior to those of the "ideal" DG-MOSFET: 60mV/decade subthreshold-swing, negligible DIBL and enhanced transconductance. The values of I_D for $V_G = V_D = 1V$ (Fig. 2) are counter-intuitive and illustrate the advantage of the asymmetric devices. The transistor yielding the lowest drain current is the symetrical 50/50nm DG. This was explained in [4] by the higher source and drain resistance. Since the front (smaller) gate is used for self-aligned S/D implantation, the doped regions overlap the back gate of the 50/100nm devices. When the back gate is biased, it creates an accumulation layer in this overlapping area, significantly reducing the S/D access resistance. This explains why device 3, with lowest total series resistance, has the highest I_D drive. We conclude that the asymmetric DG MOSFETs takes advantage of two main mechanisms: double gate effect and electrically controlled junctions [7].

Special features in the transconductance (extended "high g_m" range, plateau, double peak) were tentatively explained by the coupling between the two channels and series resistances [4].

The characteristics of asymmetric DG MOSFETs outperform those of both SG and ground-plane MOSFETs. Indeed, if the bottom gate is grounded or biased (for V_T adjustment), the subthreshold swing (Fig. 6) is degraded [8]. In other words, a ground plane with a thin buried oxide, is not an optimal solution. Asymmetric front and back oxides should be used instead.

We also performed dynamic simulations. Fig. 3 shows a transient I_D for devices 1 and 3 (see Table 1). V_G was shifted from 0 to 1V in 10 ps, with $V_D = 1V$. No difference in "turn-on" time was detected. The gate-drain (C_{GD}) and total gate (C_G) capacitances (Fig. 4) were calculated by superposing a small ac signal on a V_D ramp. A maximum increase of C_{GD} of 40% is observed at low V_D, but the value remains small ($\approx$1.5 fF/μm). The increase in C_G is proportional to the total gate area.

Logic function. The DG device was also tested for OR logic functionality. If the two gates are biased separetely, the transistor will be on if at least one gate has a positive bias. The logic diagram (Fig. 5) shows that this OR function has a on/off current ratio of more than 80 dB - sufficient for conventional logic circuitry.

Conclusion. Relaxing the self-alignment constraint on DG architecture does not imply inferior performance. Our simulations indicate no major disadvantages to asymmetric 50/100nm DG. In fact, these DG MOSFETs show better static characteristics than their symetrical (50/50nm) counterparts and can be used for enhanced current and transonductance (when $V_{G1} = V_{G2}$) or to generate new logic functions (when V_{G1} and V_{G2} are biased independently).

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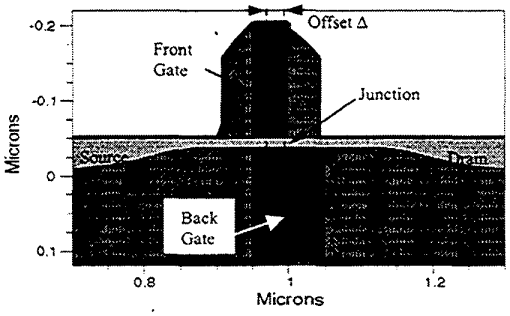

Fig. 1: Schematic representation of device 2 (Δ=-25nm).

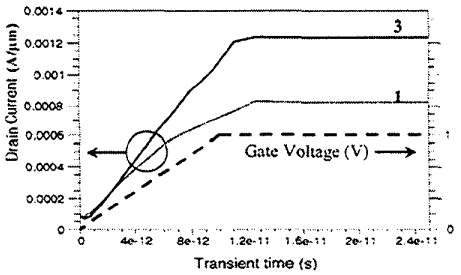

Fig. 3: Drain transient current at V_D=1V.

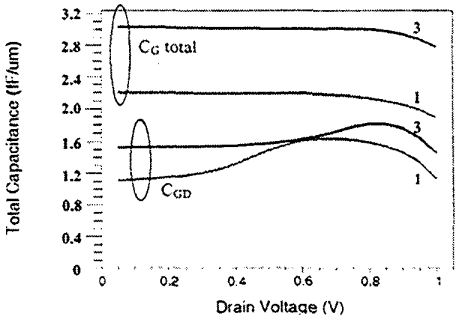

Fig. 4: Total gate C_G and gate-drain C_{GD} capacitance in devices 1 and 3 (fF/μm).

Table 1: Parameters of devices corresponding to Fig. 1.

Structure	1	2	3	4
L1 (nm)	50	50	50	50
L2 (nm)	50	100	100	100
Offset Δ(nm)	0	-25	0	25

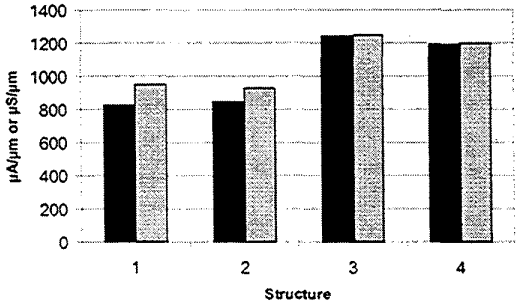

Fig. 2: Drain current at V_G= 1V; V_D= 1V (black), and transconductance peak at V_D= 1V (grey), for the various structures in Table 1.

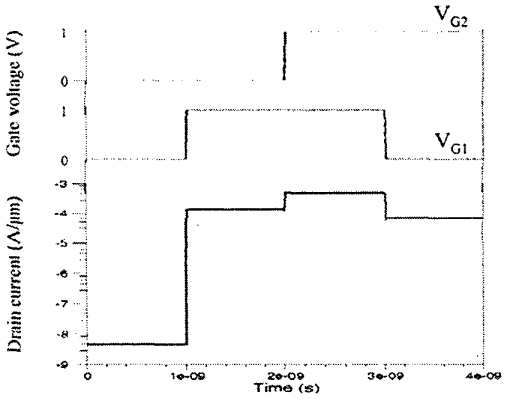

Fig. 5: Logic diagram of a DG MOSFET with gates biased independently, showing the OR function.

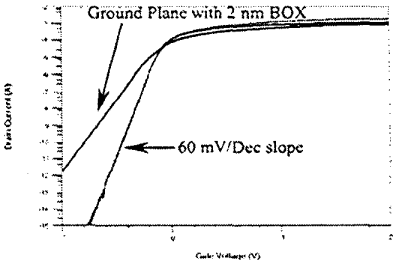

Fig. 6: Degradation of the subthreshold slope.