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From SOI materials to innovative devices

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Abstract

Novel device architectures and materials are required to extend the limits of ULSI microelectronics. Recent properties of UNIBOND® and SOS substrates, determined with the pseudo-MOSFET technique are described. The discussion of advanced SOI devices includes two basic aspects: the scaling of conventional MOSFETs and the design of alternative structures. We discuss the effects resulting from the reduction in channel width, length and thickness and present the merits of more innovative transistors with ground-plane, dynamic-threshold or double-gate. © 2001 Published by Elsevier Science Ltd.

1. Introduction

The recent take-off of SOI technology for VLSI applications is explained by a combination of several effects: rapid progress in SOI substrates (quality and cost), the relatively easy transfer of classical CMOS processing to partially depleted SOI, and inherent gains in performance and power dissipation [1]. However, the use of SOI is far from limited to classical CMOS and offers a range of new possibilities, both in the domain of alternative materials and for innovative SOI-specific devices. In this paper we focus on characterization of SOI material quality by the pseudo-MOSFET (Ψ-MOS) technique [2] and on the design, simulation, and experimental characterization of novel SOI components.

2. Materials

Silicon-on-insulator wafers, and especially bonded wafers, offer new possibilities in material structure and device architecture. Different options, such as silicon film on highly resistive silicon substrates (for RF applications), silicon-on-quartz, or silicon-on-sapphire (SOS) are already available. Other promising structures, such as silicon-on-nothing, compound and wide-gap semiconductor films on oxidized silicon substrates, buried structures, various types of uncommon stacking, or extremely thin active films, have already shown promise of expanding the frontiers of the conventional Si technology. It should be noted that buried structures can take the form of a material modification prior to bonding (for example, ground-plane (GP) MOSFETs) or of bonded CMOS circuitry.

For either conventional CMOS or exotic applications, the material quality is of utmost importance, since the parameters of the active film, buried oxide, silicon/oxide and oxide/substrate interfaces or the substrate underneath the BOX will determine the performance of specific structures. For this reason, and because the

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quality of the material is always an issue in microelectronics, wafer characterization is a major concern. A large number of methods is available for this purpose: Hall effect, spreading resistance, Ψ-MOS technique [3], deep-level transient spectroscopy, device-based characterization (transistor and capacitance measurements), etc. The Ψ-MOS technique is of particular interest because it permits on-wafer measurements with a minimum of processing, thus reducing the process-induced material modifications.

2.1. Pseudo-MOSFET technique

The Ψ-MOSFET is an SOI-specific transistor where the buried oxide (BOX) acts as a gate oxide. It is possible to use the Ψ-MOSFET much as one would use a standard MOS transistor to evaluate parameters such as carrier lifetime, doping, interface states density, threshold and flat-band voltages, subthreshold swing, carrier mobility, etc. Only results concerning the mobility and interface state density are presented here because they reveal the most about the film and Si/BOX interface quality.

The Ψ-MOS technique is very easy to apply. It uses the substrate as a gate and the BOX as the gate oxide, while the source and drain are formed by two needles set with a given pressure on the active film (see inset in Fig. 1(b)). The pressure applied on the needles helps pierce the native oxide and creates Ohmic contacts which serve as source and drain. The electron/hole conduction takes place along the active film/BOX interface.

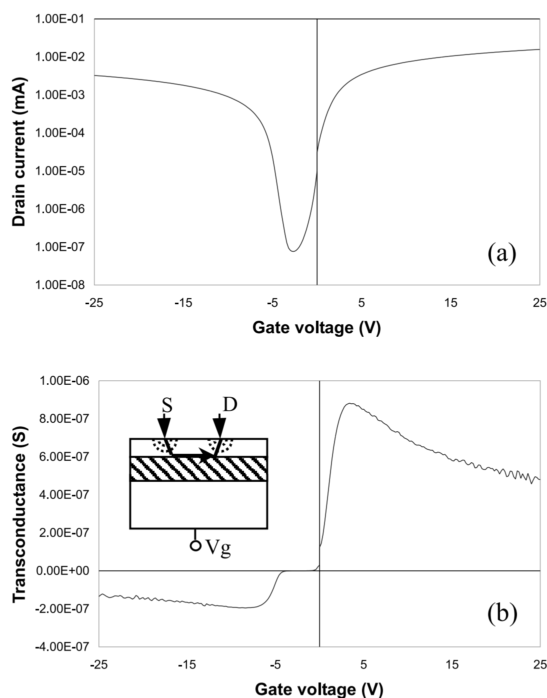

Fig. 1. (a) Drain current and (b) transconductance obtained with the Ψ-MOS method in UNIBOND®.

When the substrate is biased, an inversion layer appears above the BOX (i.e. at the bottom of the silicon film) and the conduction channel is created between source and drain, just as in a regular CMOS transistor. Fig. 1(a) and (b) show the perfectly MOS-like drain current and transconductance characteristics as a function of gate voltage in a Ψ-MOS transistor. One difference between the Ψ-MOS transistor and regular MOSFETs is that it can be operated as either p-MOS or n-MOS because there is no intentionally doped source or drain, while the substrate gate can attract either electrons or holes to the Si/BOX interface depending on gate voltage polarity.

2.2. Evolution of UNIBOND® properties

The results shown in Table 1 have been obtained on various UNIBOND® wafers arranged in chronological order: wafer A, the oldest, is several years old, while wafer F, the most recent among those presented here, was processed during the summer of 2000.

Table 1 reflects the overall progress of the material properties. Note the steady reduction of the interface state density (D_{it}) at the active Si/BOX interface. This feature and the improved quality of the film explain the increase in carrier mobility and transconductance peak (G_{max}, measured for $V_D = 100$ mV), particularly for electrons.

2.3. Extension to recent silicon-on-sapphire materials

The very thick sapphire insulator normally prevents the application of the Ψ-MOS to characterize SOS wafers (the necessary operating gate voltages would be in the 10–100 kV range). In our case however, the sapphire substrate was thinned down to 30 μm by etch-back, grinding and mechanical polishing [4]. The thinned insulator substrate allowed us to operate the Ψ-MOS transistor using reasonable voltages, from 0 to 1100 V. “Classical” drain current curves are presented on Fig. 2.

The results obtained for these specimens are: 29 $cm^2\,V^{-1}\,s^{-1}$ electron mobility at the silicon/sapphire interface, and interface state density of 1.5×10^{12} cm^{-2} eV^{-1}. The difference between the threshold and flat-band voltages is about 1400 V.

These results show that the electron mobility is still significantly impacted by lateral stress and interface defects, in spite of the significant progress achieved by solid-phase epitaxial regrowth and annealing.

Table 1
Pseudo-MOSFETs results in various generations of UNIBOND® wafers

Wafer	$G_{max}-$ (nS)	$G_{max}+$ (nS)	μ_p (cm^2 V^{-1} s^{-1})	μ_n (cm^2 V^{-1} s^{-1})	D_{it} ($\times 10^{11}$ cm^{-2} V^{-1})
A [3]	−69.4	290	158	511	5.8
B [3]	−76.3	284	160	535	4.3
C [3]	−79	362	165	632	3.5
D [4]	−110	339	169	610	2.8
E	−97	446	165	745	1.9
F	−107	460	177	747	1.0

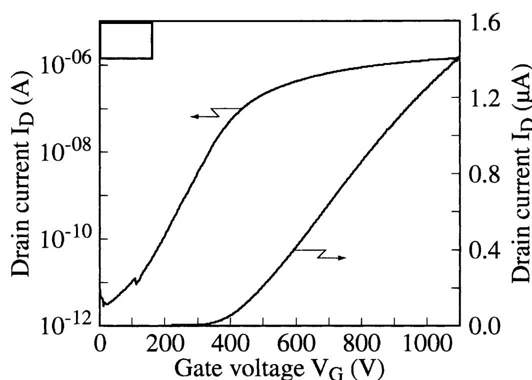

Fig. 2. Drain current in a SOS wafer.

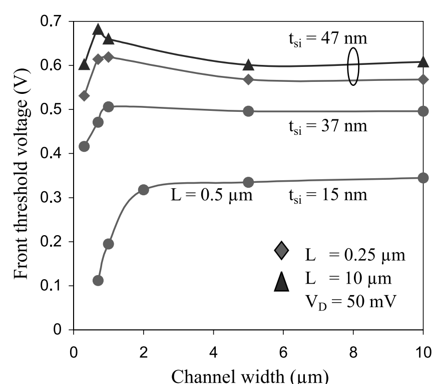

Fig. 3. Threshold voltage reduction with channel width and length.

3. Devices

The advantages of SOI over bulk-silicon substrates have been demonstrated in terms of performance, reliability [1] and new opportunities (scaling, architecture) for the future generations of devices. With the progress of SOI technologies, we explore the limits of SOI using fully-depleted (FD) SOI MOSFETs with very short channel (<0.1 μm), narrow channel (<0.3 μm), ultra-thin Si film (<20 nm), thin and/or low-κ BOX, low doping and mid-gap metal gate. New architectures for ultimate SOI transistors such as dynamic-threshold (DT-MOS), ground-plane or double-gate (DG) SOI MOSFET are also under investigation. In the following sections, we will discuss and illustrate, with selected examples, some of the characterization, simulation and modeling issues that arise in these devices.

3.1. Narrow-channel MOSFETs

The interest in SOI technology for low-power and low-voltage VLSI applications has led to the need for very small devices. Small geometries mean short but also narrow channels. If short-channel effects have been studied extensively, there are relatively few results on narrow-channel effects. We investigate narrow-channel effects in fully depleted, LOCOS isolated n-MOSFET devices where the peculiar lateral topography leads to a parasitic conduction path between source and drain. The main effect of this parasitic conduction, which takes place along the highly inhomogeneous edges of the Si island (see inset of Fig. 4), on the device characteristics is the reduction of the threshold voltage (Fig. 3) and effective carrier mobility with decreasing width [5]. The experiments also demonstrate an improvement in the floating body effects and breakdown voltage in narrow MOSFETs. The thinner film and thicker gate oxide of the lateral transistor, where the carrier lifetime is reduced, explain these results. Neither short-channel/narrow-channel coupling nor special front-gate/back-gate coupling was observed. In ultra thin (15 nm) SOI films, both short-channel and narrow-channel effects are attenuated.

A physical compact model based on the variation of film and oxide thickness along the width direction helps to simulate the experimental trends. The model reproduces the front- and back-gate characteristics, shown in Fig. 4. This systematic exploration of various narrow-channel effects is of high interest for low-power/voltage CMOS applications and for further optimization of lateral isolation techniques.

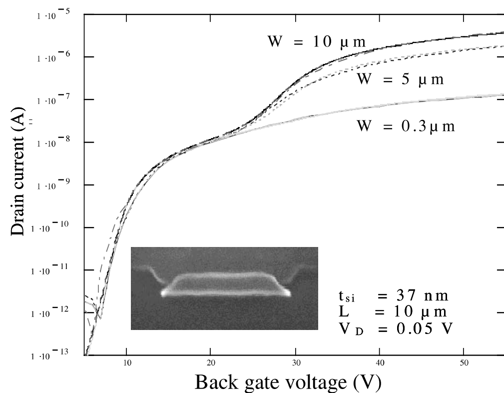

Fig. 4. The effect of parasitic sidewall transistor (see inset) on the back-gate subthreshold characteristics.

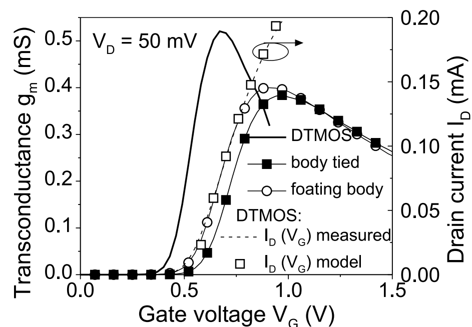

Fig. 5. Transconductance and current versus gate voltage in DT, body-grounded and floating body MOSFETs with $L = 0.25$ μm and $W = 10$ μm [7].

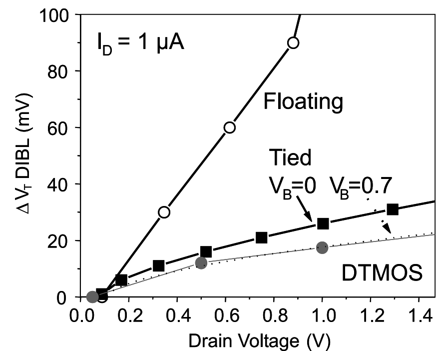

Fig. 6. DIBL roll-off in floating, body-grounded and DT-MOS transistors as a function of drain voltage V_D.

3.2. Dynamic-threshold MOSFET

3.2.1. Static characteristics

The dynamic-threshold transistor (DT-MOSFET) is normally configured by connecting the body to the gate. This transistor offers enhanced current drive, speed and V_T scalability and thus stands as a good candidate for the future ultra-low voltage (<0.6 V) CMOS applications [6]. The operating principle of this device is that the gate voltage is also applied to the body, dynamically reducing the threshold voltage which, in turn, increases the subthreshold slope and drain current. On the other hand, when the gate is not biased, the threshold voltage remains high, maintaining a low leakage current.

Systematic measurements of DT-MOSFET characteristics have been performed to explore and quantify its enhanced performance. We found that the transconductance is greatly improved (as compared with the floating body or the body-tied devices, the transconductance enhancement at low V_G exceeds 35%, see Fig. 5). A simple compact model, allowing circuit designers to anticipate the performance of the DT-MOSFET and to simulate its main parameters has been developed [7]. This model yields an enhancement factor α (calculated from the transistor's technological parameters) that quantifies the DT-MOSFET's advantages over a body-grounded device:

$$V_{T,DT} \approx V_{T,BG}/(1+\alpha), \quad S_{T,DT} \approx S_{T,BG}/(1+\alpha),$$
$$\mu_{DT} \approx (1+\alpha)\mu_{BG}$$

where S_T refers to the subthreshold slope and the subscripts DT and BG label dynamic-threshold and body-grounded devices respectively.

At low temperature, the advantage arising from DT-MOS operation becomes greater still: the transconductance increases more rapidly than in a grounded-body transistor. A possible reason is the improvement in the carrier mobility, which at low temperature is limited by ionized impurity scattering. Indeed, the space charge region is narrower in a DT-MOSFET, being controlled by both the surface potential and the body potential. Another significant advantage of the body potential control is the reduction in short-channel effects such as DIBL and V_T roll-off, illustrated in Fig. 6.

3.2.2. Dynamic characteristics

Dynamic-threshold operation need not imply a physical connection between body and gate. A similar effect happens in dynamic regime: when the gate voltage is switched high, the body is temporarily charged by majority carriers released from the expanding depletion region. Conversely, when the gate is turned off, a deep depletion region is formed and the body potential drops below zero. These effects give rise to the so-called current overshoot and undershoot, respectively, which are current transients governed by generation-recombination mechanisms and junction leakage. It is clear that when the device is operated at high frequency the overshoot

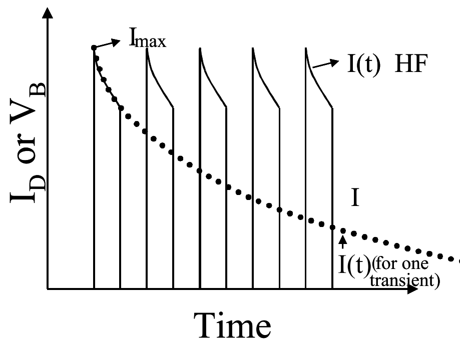

Fig. 7. Drain current I_D or body potential V_B in a transistor clocked at high frequency compared to a single switching event (- - -).

effect persists, inducing a "permanent" positive biasing of the body that is beneficial in terms of current gain. Fig. 7 illustrates the variation of the average current and body potential as a function of gate signal period.

3.3. Ground-plane MOSFET

In SOI transistors, the fringing fields within and underneath the BOX are the cause of a supplementary drain-induced barrier lowering (DIBL) [8]. The effect of the lateral penetration of the field is equivalent to an undesirable biasing of the transistor's back interface: the back channel becomes slightly inverted which lowers the threshold voltage – see Fig. 8 for geometry. Numerical simulations show that the introduction of a ground plane (that is, a conductive plane kept at a zero potential), located just below a (preferably thin) BOX, can attenuate this phenomenon. The purpose of the ground plane is to prevent substrate depletion underneath the BOX and hence limit the lateral penetration of the drain-induced electric field. For the ground plane to be effective the substrate/body capacitance should be greater than the drain/body capacitance (which is true roughly if $t_{BOX} < L/2$, where L is the channel length) [9].

Fig. 9 shows that if the body doping is an important parameter in the reduction of DIBL for "thick" films, it becomes irrelevant when the thickness decreases under about 150 Å (for $L = 0.1$ μm), though the ground plane is still effective. In other words, the requirement for a high doping is relaxed, which is greatly beneficial in terms of mobility and transconductance.

3.4. Extremely thin SOI MOSFET

The recent progress in wafer uniformity and device processing allows the fabrication of extremely thin (1–5 nm) SOI MOSFETs (inset in Fig. 10), which offer very attractive prospects in terms of performance and quantum properties.

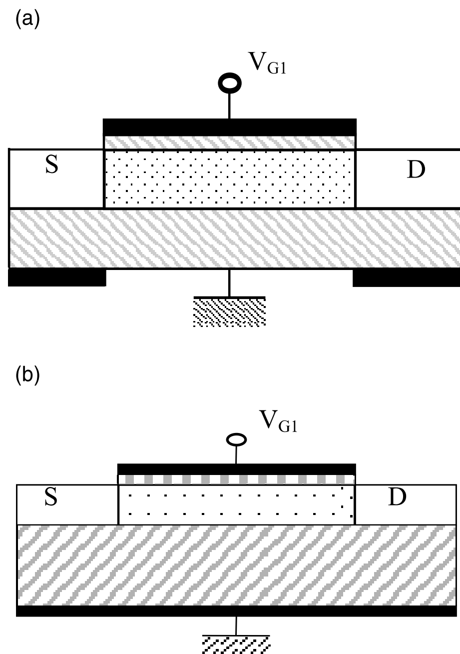

Fig. 8. (a) Partial ground-plane SOI MOSFET and (b) ground-plane SOI MOSFET.

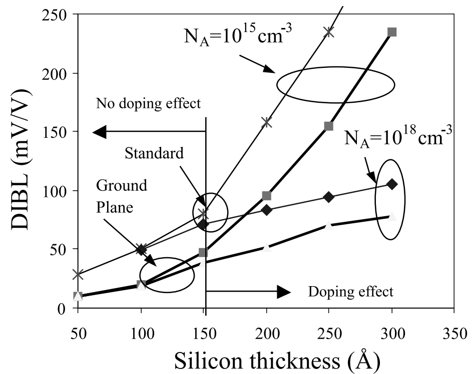

Fig. 9. Simulated DIBL vs. Si thickness in standard and ground-plane structures ($L = 0.1$ μm) for high and low doping.

These devices work on the same model as the regular fully-depleted MOSFETs but with much thinner Si films. The I_D (V_G) curves are typical (Fig. 10), although unusually strong couplings appear between the front and the back gates and between the film and the substrate. Interesting thickness-related effects on the carrier mobility, threshold voltage, subthreshold swing and transconductance are also observed [10]. The film is too thin to be simultaneously inverted at the top interface and accumulated at the back one. A consequence of this

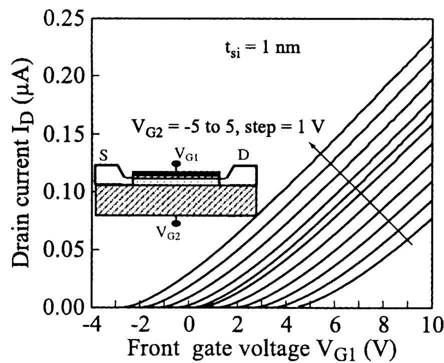

Fig. 10. Drain current vs. gate bias in a 1 nm thick transistor (inset) with $L = 30$ μm and $W = 100$ μm.

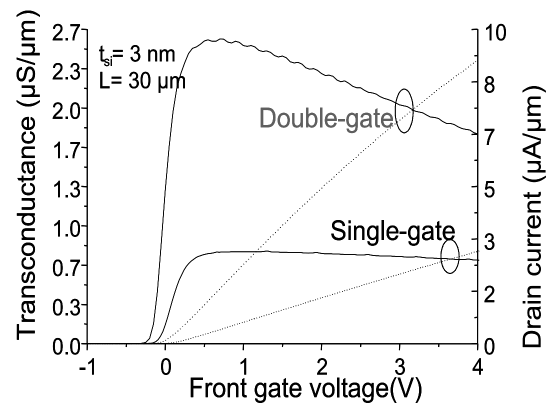

Fig. 11. Drain current and transconductance vs. front gate bias for a 3 nm thick transistor ($W = 3$ μm, $L = 30$ μm). In the DG regime, $V_{G2} = 1.24V_{G1}$ [10].

is a constant subthreshold swing. The substrate underneath the BOX can become depleted, which leads to an apparent increase of the BOX thickness, and in a decrease of its apparent capacitance.

The special distribution of minority carriers in these ultimate thin-film devices is governed by quantum confinement. Thus, for example, the threshold voltage increases as the film thickness is reduced below 10 nm. The availability of room-temperature quantum effects in ULSI-compatible Si devices opens up novel devices with strong, controllable voltage nonlinearities. For example, gate-controlled negative differential conductance characteristics should become available in ultra-thin SOI MOSFETs with thin tunneling gate oxides, as carriers tunnel from the gate into the quantized density of states in the channel. Similar characteristics, albeit at rather low current levels, have already been demonstrated in three-terminal Esaki diodes, where the current flows by interband tunneling from the n-MOS channel into the p-type drain [11]. Integrating such devices with SOI MOSFETs promises unusual circuit functions and higher logic functionality.

3.5. Double-gate MOSFET

The peculiarity of double-gate transistors (DG-MOSFETs) is that the top and bottom gates are biased simultaneously, $V_{G2} = V_{G1}(t_{OX2}/t_{OX1})$. This difference in biasing compensates for the slight difference in front and back oxide thickness and guarantees nearly identical surface potentials.

In a partially-depleted transistor with a thick enough active layer, two independent channels are formed close to the interfaces, while the central region of the film remains undepleted [1]. The resulting current is nothing but the sum of the contributions of two independent transistors. On the other hand, in fully depleted transistors with a thin enough film, controlling the channel from both sides at the same time forces most of the carriers to flow through the middle of the film (especially around the threshold voltage), according to the volume inversion concept [12]. The electrons are then localized further from the oxide interfaces and hence suffer less surface roughness scattering. Furthermore, when both gates are biased simultaneously, the potential fluctuations arising in the plane of the Si channel from the fluctuations in the distance between the gate and the channel are averaged out, since the oxide thickness fluctuations in the BOX and top oxide are likely to be uncorrelated. As a result, the carrier mobility in a DG-MOSFET can exceed that of a standard, single-gate device with the same channel parameters. Fig. 11 shows the comparison between a 3 nm thick DG-MOSFET operated with only one or both gates. The transconductance in DG mode exceeds twice the value observed in single-gate mode. This demonstrates that a DG-MOSFET is more than the sum of two classical transistors.

The challenge for achieving strong volume inversion is the fabrication of very thin film transistors, with well aligned front/back gates. On the other hand, there is little doubt that the ultimate scaled MOSFET will have a DG ... if a reasonable technological solution is uncovered. So far, DG-MOSFETs have been fabricated by a number of different approaches.

- Delta structure. The Si film is etched such that a very narrow island is isolated. After oxidation, the gate is deposited, see Fig. 12(a). The conduction is horizontal, however the Si membrane and the inversion charge sheet have a vertical configuration [13]. Other solutions exist for defining such a vertical membrane, like the Fin-gate MOSFET shown in Fig. 12(c) [14]. Extremely short devices (20 nm) can be fabricated with perfect alignment of the two gates. However, the amount of current drive available in such devices

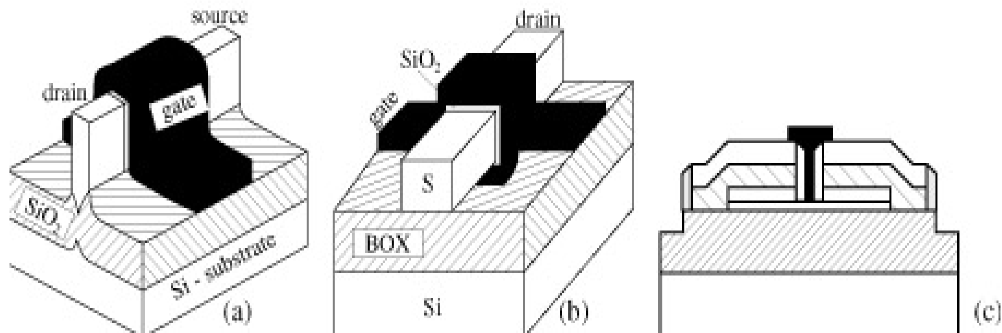

Fig. 12. Schematic illustrations of (a) delta structure, (b) GAA and (c) Fin-gate MOSFETs.

is questionable, especially since the transistor width is defined by the film thickness (0.1–0.2 μm).

- Gate-all-around (GAA) structure. This device has a planar configuration. The body of the GAA transistor consists in a Si membrane which is formed by etching a cavity in the BOX, underneath the silicon film, as illustrated in Fig. 12(b) [15]. The technology is relatively simple and the gates are self-aligned. The critical issue is to guarantee a thin enough Si membrane.
- DG-MOSFET by epitaxial lateral overgrowth (ELO). The Si film is oxidized and patterned, as shown in Fig. 13(c). A poly-Si back gate is deposited and oxidized. Then, single-crystal silicon is grown laterally and vertically from a nearby seed. The structure is planarized, using the step difference of the pattern as a thinning mark. The front oxide and gate are aligned to the back gate [16]. The body is horizontal, as in the GAA transistor. The critical problem here is the thickness of the Si film (100 nm) and the alignment of the two gates.

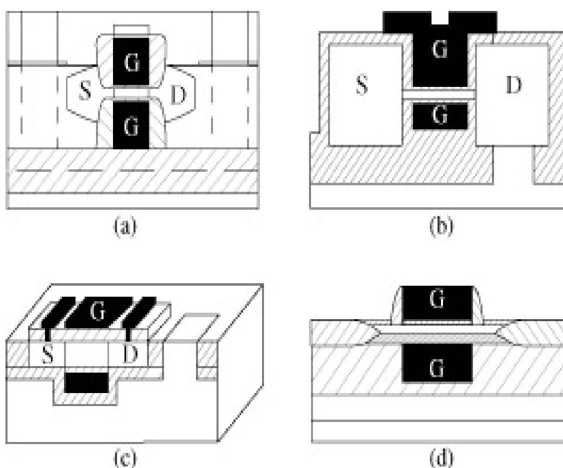

Fig. 13. Various architectures for DG SOI MOSFET.

- Bonded DG-MOSFET. The transistor body is delineated from a bulk-Si wafer by LOCOS isolation (Fig. 13(d)), and after gate oxidation, a back gate is deposited on ... top. This structure is covered with oxide and bonded to a “passive” wafer. The back of the initial, “active” wafer is etched off, the LOCOS oxide serving as an etch-stop. After turning the structure upside-down, the front oxide and gate are processed [17]. This technology depends on the quality of the gate alignment and the accuracy of the LOCOS thickness.
- Horizontal DG-MOSFET with epitaxially deposited source and drain. The challenge of this process is to achieve a free standing ultra-thin membrane from an SOI substrate, by either tunnel epitaxy [18] or a SiGe intermediate sacrificial layer [19]. Both fabrication sequences are very complex. Once the membrane, i.e., transistor body, and the top/bottom gates are completed, the source and drain regions are deposited epitaxially, as shown in Fig. 13(a) and (b).

We believe that there is still room for other technological processes to be proposed. Most likely, it will be based on a smart-cut sequence which offers unchallenged flexibility. The main constraints for DG-MOSFETs are: (i) self-alignment of front and back gates, (ii) thin horizontal or vertical membrane for the transistor channel, (iii) adjustable transistor width, and above all, (iv) manufacturability.

4. Conclusion

SOI enables the design of transistors that may succeed beyond the frontiers of the conventional CMOS technology. SOI circuits deserve a dedicated technology and design to push the limits of microelectronics. As the quality of the material improves and the technology is better controlled, the processing of these alternative devices becomes more and more realistic.

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