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Solid-State Electronics 48 (2004) 877–885
SOLID-STATE ELECTRONICS
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Blue sky in SOI: new opportunities for quantum and hot-electron devices

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The review of this paper was arranged by Prof. S. Cristoloveanu

Abstract

The combination of silicon-on-insulator (SOI) substrates with ultrathin Si and insulator layers opens new opportunities for quantum effect and hot-electron devices. Unlike their III–V predecessors, these devices have the crucial advantage of potential integrability with dominant silicon technology. We discuss three examples of such SOI devices: a three-terminal real-space transfer transistor with a low-barrier dielectric; a vertical tunneling transistor with an ultrathin tunneling gate oxide; and a lateral interband tunneling transistor. None of these devices has progressed beyond a rudimentary proof-of-concept demonstration, but the strong nonlinearities of their characteristics deriving from quantum tunneling or hot-electron injection, as well as their unique scaling behavior, make them an interesting playground for innovative device research.

1. Introduction

Silicon-on-insulator (SOI) transistors built in thin fully-depleted Si channels on top of an insulating buried oxide are predicted by the current technology roadmaps [1] to take over from bulk Si CMOS devices over the next few years, because of their superior scaling properties, enhanced performance, and improved device isolation. In the mainstream silicon technology, there is an ongoing debate about the most appropriate double-gate SOI transistor geometry and fabrication sequence that will meet the architectural demands for end-of-roadmap Si transistors [1]. At the same time, the continuing miniaturization of SOI devices, with available Si channel and gate insulator thickness dropping to the nanoscale, as well as integration of ultrathin SOI with novel dielectrics and gate materials, is opening the door to quantum effect and hot-electron devices. A number of such devices, based on quantum tunneling, hot-electron injection or charge quantization, have been demonstrated in III–V heterostructures over the past two decades [2]. Yet the great success of III–V heterostructures, due to the bandgap engineering capabilities of modern epitaxy, has not led to technological insertion, as the mainstream semiconductor technology continues to be dominated by Si CMOS. Today, it appears hardly conceivable that any stand-alone III–V quantum effect or hot-electron architecture will make inroads against Si ULSI [3], so the search for ULSI-compatible innovative devices acquires a particular urgency.

In this paper we will present three device structures that appear suitable for exploitation in the SOI world: a real-space transfer (RST) injection transistor, a lateral interband tunneling transistor (LITT), and a vertical tunneling transistor (VTT). All of these devices can and have been envisaged in III–V heterostructures, but SOI implementations offer both compatibility and functional advantages. Further, some of these devices can also be operated in the standard transistor mode, with a drift-diffusion current flowing between source and drain

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[1] The latest publicly released version of the ITRS roadmap is available on the http://public.itrs.net web site.

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doi:10.1016/j.sse.2003.12.031

modulated by the third, gate electrode. We should stress that none of these SOI devices has progressed beyond a rudimentary proof-of-concept demonstration and, as we will discuss below, they all require some fabrication advances beyond the current state of the art. We also stress that our list of quantum effect and hot-electron devices could be complemented by other types of structures, such as the gated quantum dots built in SOI that show strongly nonlinear conductance due to single-charge tunneling [4–6]. What we hope to convey is that novel devices and functionalities can still be grafted onto the rapidly growing SOI technology—an opportunity that device physicists should not miss.

2. Real-space transfer transistors in SOI

The RST transistor (also known as a charge injection transistor) is a three-terminal semiconductor device based on real-space transfer of hot electrons into the collector [7]. Two possible device structures are illustrated in Fig. 1. The bottom-collector configuration of Fig. 1(a) has been typically used in III–V heterostructures; the top-collector version of Fig. 1(b) is advantageous in terms of speed [8], but has been difficult to implement in heterojunctions. With the source grounded, a drain voltage V_D accelerates the electrons in the source–drain channel. These electrons equilibrate their energy via electron–electron collisions and become "hot", with an approximately Maxwellian distribution characterized by an effective temperature $T_E > T$ (where T is the lattice temperature). Given an appropriately low ΔE_C barrier between the channel and the collector, RST of electrons into the collector at sufficiently high T_E produces a strong negative differential resistance (NDR) in the $I_D(V_D)$ circuit for a fixed V_C. Such transistors have been implemented in a number of semiconductor heterostructures, mostly III–V but also Si/SiGe [9,10]. The room temperature characteristic of a bottom-collector InGaAs/InAlAs RST transistor is shown in Fig. 1(c) [11].

The potential usefulness of RST transistors derives from a number of factors. First, the efficient control of the injection current I_C by the heating voltage V_D enables ultrahigh-speed operation of the device as an amplifier. In fact, since a top-collector device can be operated both as a field-effect transistor (FET), where the collector electrode acts as a gate and modulates the source–drain current I_D, and an RST transistor, where the drain

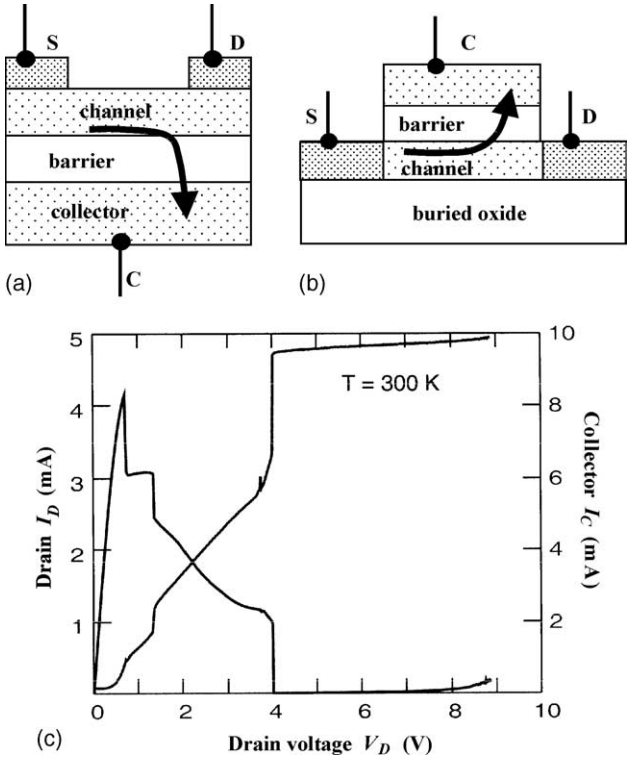

Fig. 1. Schematic diagram of real-space transfer transistors. (a) Bottom-collector configuration, used in many III–V implementations of the RST transistor; (b) top-collector configuration, readily amenable to SOI implementation; (c) characteristics on a bottom-collector III–V RST transistor at $V_C = 3.9$ V at $T = 300$ K (source–drain separation of 1 μm and collector stripe width of 25 μm). Note the strong NDR in the drain circuit [12].

controls the collector injection current I_C, the speed issue can be compared experimentally. In a III–V device with $L_G = 1$ μm gate length, the RST mode was shown to be a factor of three faster [12].

Second, the source and drain in an RST transistor are obviously symmetric, leading to additional logic functionality. In a device with two contacts to the channel, the output I_C current in the RST mode is invariant under an interchange of the source and drain V_S and V_D, so the device exhibits an exclusive *or* dependence of I_C on V_S and V_D input voltages regarded as binary logic signals. More powerful *ornand* logic functionality is obtained in an RST device with three input terminals, where the output current has either *or* or *nand* dependence on the voltage applied to any two of the three electrodes, depending on the voltage applied to the third electrode [10,13]. To be sure, the RST transistor, because of its power dissipation is not competitive as a LSI logic element. However, it can find applications as an ultrafast "smart" switch of large currents between two circuits. Interestingly, in III–V structures the logical functionality can be transferred into the opto-electronic domain by implementing a p-type direct bandgap collector electrode [10].

Finally, the very strong NDR observed in the channel circuit allows the RST transistor to be used as a voltage controlled oscillator of ultrahigh bandwidth. In a well-designed RST transistor, at sufficiently high collector bias V_C, nearly all of the channel current is diverted into the collector (in other words, the NDR in the drain circuit can have a very high peak-to-valley ratio, $>10^3$). When biased into the NDR regime, the device is unstable. With an *LC* load, a single RST transistor can be used as a voltage controlled oscillator, with the oscillations can be turned on and off by V_C.

The technological potential of RST transistors, given their speed and functional advantages, would be greatly enhanced if they were implemented in a technologically compatible fashion. Here we argue that SOI offers a unique opportunity. Consider the device illustrated in Fig. 2, which contrasts a bulk Si transistor and an SOI transistor with a narrow undoped Si channel, both capped with a gate dielectric. If the dielectric is SiO_2, the band offset is large ($\Delta E_C > 3$ eV) and hot-electron emission is strongly suppressed—fortunately for the standard MOSFET operation, since there the hot electrons mean gate leakage. However, there is currently an enormous research effort into alternative high-κ dielectrics, in order to enhance the gate-to-channel capacitance (and hence the MOSFET transconductance). A number of metal oxides that have been investigated for high-κ applications, such as zirconium silicates and barium oxides, have relatively low ΔE_C, in the 0.50–0.8 eV range [14]. While such low barriers are problematic for standard MOSFETs, they provide an ideal opportunity for RST transistors. Implementation of RST

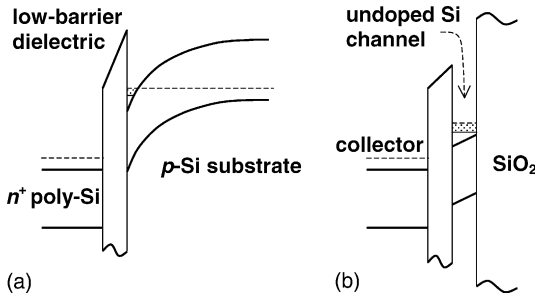

Fig. 2. Schematic vertical band diagram through the proposed silicon RST transistor with a low-barrier (high-κ) dielectric: (a) implemented on a Si substrate; (b) implemented in SOI with a thin Si channel.

transistors in SOI has a number of other potential advantages.

Thus, for efficient RST transfer to occur, the hot electrons should be kept in the close vicinity of the barrier. In a bulk Si transistor, this could be accomplished with relatively heavy substrate doping of 10^{18} cm^{-3} or higher, as shown in Fig. 2(a). However, this introduces a large parasitic input capacitance, since the drain is the input electrode in the RST mode. Moreover, it may also adversely affect the onset of RST process. Indeed, assuming that the dominant energy loss mechanism is associated with the emission of optical phonons (true only at relatively low T_E), the energy balance equation can be written as,

$$k(T_E - T) = e\mu F^2 \tau_E \tag{1}$$

where τ_E is the energy relaxation time constant, μ is the channel mobility and F is the electric field in the channel, $F \sim V_D/L_G$. For given F, the excess carrier temperature is proportional to the mobility, which should be much higher in an undoped SOI channel of Fig. 2(b) than in a heavily-doped bulk inversion channel of Fig. 2(a). Once the RST process is well established, the principal energy loss mechanism becomes the flux of hot electrons over the barrier and into the collector, rather than optical phonon emission, and Eq. (1) no longer holds [15]. By the time this regime is established, electron transport along the channel typically reaches saturation velocity and mobility becomes less important, just as in the case of conventional transistors. But even then, the reduced parasitic capacitance in SOI would mean that SOI-based RST devices would be limited by the energy equilibration time in Si, expected in the subpicosecond range. It is worth noting that SOI RST devices should be faster than their GaAs-based counterparts, because GaAs suffers from intervalley scattering that delays the RST onset [16].

Thus, the ULSI-driven research programs aimed at high-κ gate dielectrics, may have already contributed a

valuable niche SOI application: low-barrier dielectrics may provide the material base for SOI RST implementation and open a variety of useful circuit applications. As discussed above, SOI-based RST transistors with their minimized drain capacitance should perform better than previously explored compound semiconductor devices—and they can be produced today. In a more futuristic vein, if a p-type direct-gap semiconductor could be used for the collector layer on top of the low-barrier-oxide dielectric layer in Fig. 2(b), an optically functional Si-based logic device would result.

3. Vertical tunneling transistor in SOI

Another device class that was originally proposed and realized in III–V material but appears eminently suitable for SOI implementation is the vertical tunneling transistor (VTT) with lateral extraction of the operating tunnel gate current I_G [17]. The principle of operation is illustrated in Fig. 3(a). Electrons tunnel from the gate electrode into the quantum well, where two-dimensional (2D) subbands E_N arise from size quantization. Elastic tunneling into reduced dimensionality states conserves energy and transverse momentum, so the tunneling current depends on the alignment between E_N and the occupied states in the gate [18]. This alignment, in turn, is controlled by the voltage on the back-gate electrode V_{BG}, which induces an electric field that changes the 2D confining potential and alters the alignment between the channel and the gate [2,17]. In principle, once E_1 is lowered below the bottom of the occupied states in the gate electrode, the tunneling current is cut off by the energy and transverse momentum conservation, leading to NDR in the $I_G(V_{BG})$ characteristic and hence a negative transconductance, $g \equiv \partial I_G/\partial V_{BG} < 0$. The tunneling I_G is extracted laterally, via a separate contact to the quantum well. Since the charge in the quantum well responds to the back-gate, it might appear that V_{BG} would be screened by this charge, leading to an absence of control of the tunneling current by V_{BG}. However, adding electrons to a 2D system raises its Fermi level, so that it is energetically favorable that part of the V_{BG}-induced electric field still penetrates through to the top barrier (this was discussed in terms of an effective quantum capacitance in Ref. [17]).

The first VTT devices were fabricated in the GaAs/AlGaAs material system more than a decade ago [19], where a thicker second AlGaAs barrier separated the GaAs quantum well from the substrate (see Fig. 3(a), but with GaAs and AlGaAs instead of Si and SiO_2). One difficulty with these III–V devices was making good ohmic contact to the quantum well without introducing leakage to the substrate. This problem is obviated in SOI, where the buried oxide is essentially impenetrable and where the device of Fig. 3(a) can be fabricated by a fully technological transistor process, with an ultrathin undoped Si channel to foster size quantization and a tunneling gate oxide.

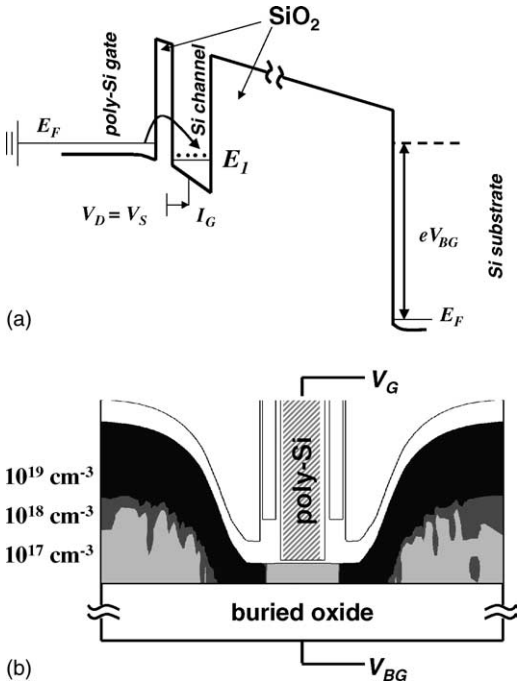

Fig. 3. (a) Schematic vertical band diagram through the VTT under bias, indicating the electron tunneling into the quantized Si channel (only the lowest subband E_1 is shown) and their subsequent lateral extraction via the (shorted) source and drain contacts. Control of the tunneling current I_G via V_{BG} is due to the penetration of the electric field through the Si channel, which alters the alignment of E_1 with poly-Si gate. (b) Simulation of the fabricated prototype: the Si film thickness under the gate is ~5 nm thick, the front gate oxide is ~1 nm. Gray-scale shows the 10^{19}, 10^{18} and 10^{17} cm^{-3} doping contours in the source and drain extensions, given by the Silvaco simulator using actual processing parameters. The channel under the gate is undoped.

Proof-of-concept SOI VTT devices were recently fabricated on standard UNIBOND SOI substrates (200 nm of undoped Si on top of 400 nm of buried oxide) using an existing CMOS mask set [20]. The active region Si was thinned to 50 nm using repeated sacrificial oxidation and removal and then locally thinned to $t_{Si} \sim 5$ nm in the gate region [21]. The thermal gate oxide was kept as thin as possible by densifying the native oxide, resulting in ~1 nm SiO_2. After in situ doped poly-Si gate material (P-doped to ~10^{19} cm^{-3} range), the device followed standard transistor processing using e-beam gate level lithography ($L_G = 0.1$ μm), nitride spacers, and low-energy (3 keV) As source/drain implants. The fabrication sequence was simulated on Silvaco software, using the actual implantation and activation anneal parameters and the resulting cross-sectional view of the

device is illustrated in Fig. 3(b), including the doped source and drain extension contours. The simulation of low-energy implantation into very thin SOI layers may not be entirely reliable, but it is certain that the Si channel under the gate is essentially undoped.

Despite the ultrathin Si channel and gate oxide, these devices successfully operated as standard transistors, with good subthreshold slope and acceptable drain-induced barrier lowering, as shown in Fig. 4(a) [20,22]. The negative threshold $V_T < 0$ was due to the n^+-poly-Si gate material. Once the channel is depleted with $V_G < V_T$, an even more negative V_G results in a slowly increasing and relatively temperature-insensitive tunneling current through the ultrathin gate oxide. The transistor can also be turned on using the substrate back-gate voltage V_{BG}, although fairly large biases $V_{BG} > 10$ V are required.

The tunneling operation of the VTT is shown in Fig. 4(b). The source and drain electrodes are shorted together and biased to a fixed voltage V_D with respect to the grounded gate electrode. The tunneling current I_G is then modulated by V_{BG} and the resulting transconductance g first increases and then drops, with one or more clear minima in-between. The initial increase of g with V_{BG} corresponds to the V_{BG}-induced lowering of E_1 with respect to the gate, leading to a higher I_G. The eventual drop in g at large V_{BG} ($V_{BG} > 15$ V, see Fig. 4(b)), corresponds to a large carrier density being established in the Si channel, which screens the V_G-induced electric field. The minima in g at intermediate V_{BG} corresponds to the E_1 subband going out of alignment with the occupied states in the gate (at larger $V_S = V_D$ other higher-lying E_N participate, whereas a potential difference between source and drain smears out the structure

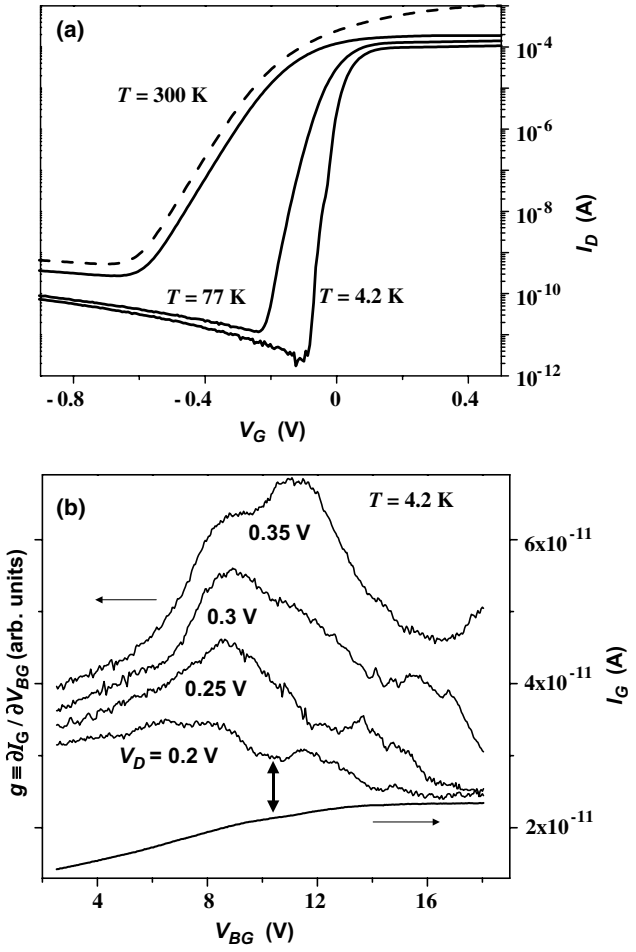

Fig. 4. (a) Standard $I_D(V_G)$ transfer characteristics at $T = 300$, 77, and 4.2 K for $V_D = 0.1$ V (and 0.6 V at $T = 300$ K, dashed line), $V_{BG} = 0$. The negative threshold V_T is due to the n^+-poly-silicon front gate. (b) Tunneling $I_G(V_{BG})$ characteristic at $T = 4.2$ K for $V_S = V_D = 0.2$ V (arrow marks the transconductance $g \equiv \partial I_G/\partial V_{BG}$ minimum), together with smoothed $g(V_{BG})$ for various $V_S = V_D = 0.20$–0.35 V.

in g because energy E_1 varies along the channel with respect to the occupied states in the gate). In these early, proof-of-concept devices, g does not really go negative and the V_{BG} required to modulate I_G is unacceptably large. However, a truly uniform (and thinner) Si channel, a uniform gate tunneling barrier, and a much thinner buried oxide (an expected development in SOI) would lead to much sharper features at noncryogenic temperatures. Finally, just as in RST transistors, a well-controlled gate dielectric with smaller $\Delta E_C \sim 1$ V would, in principle, increase the magnitude of tunneling I_G while retaining the prospect of room temperature operation.

4. Lateral interband tunneling transistor in SOI

The above-described RST and VTT devices diverged from the transistor paradigm in that current flow left the channel, either by hot-electron real-space transfer or by tunneling through a thin barrier. A different type of device, based on interband tunneling as in the Esaki diode [23] but with gate control of the tunneling current, lends itself to SOI implementation. The lateral interband tunneling transistor (LITT) is based on a heavily-doped lateral pn junction in an ultrathin Si channel on SOI, with a standard gate oxide and a gate electrode overlapping the junction depletion region—a schematic illustration is shown in Fig. 5. The gate voltage V_G controls the interband tunneling current by adding a vertical electric field component to the lateral F of the reverse-biased pn junction. This principle of operation is reminiscent of gate-induced drain leakage (GIDL) in bulk Si MOSFETs, where the parasitic GIDL current arises due to tunneling between the drain and the body—however, in our device the source–drain tunneling current is the main current component. Although no adequate quantitative model exists for interband tunneling in indirect materials like Si, the available expressions with adjustable parameters for the electron–phonon coupling constant all predict a sharp near-exponential rise of the current with the electric field F [24]. While this appears promising for high-gain amplification, adding a third terminal to a heavily-doped pn junction without simultaneously introducing leakage and parasitic capacitance is not an easy task.

One approach to gating the interband tunneling process, demonstrated first in III–V material [25] and subsequently in Si [26,27], is to fabricate an actual MOSFET but with the drain doped the opposite of the source. Then, the gate voltage V_G influences F (and hence the interband tunneling current) between the inversion channel and the drain. The effective cross-sectional area of the channel-drain pn junction is then kept small by the physical depth of the inversion channel, but the very existence of the inversion channel increases the device area and adds to the gate capacitance. An alternative LITT implementation, which avoids the inversion channel altogether, is a heavily-doped pn junction in a thin Si channel in an SOI geometry, as in Fig. 5. The thin Si channel reduces the source–drain capacitance and leakage current, while V_G (of either polarity) adds to the drain-voltage controlled lateral F in the junction. The device can be operated in either forward or reverse source–drain bias, but reverse V_D appears more promising for high-speed applications because of absent minority carrier injection. In principle, a very narrow ($\leqslant$10 nm) gate should overlap the depletion region only, minimizing the gate capacitance. Then, the ideal device would occupy very little area, as dictated by the source and drain contacting requirements, have very low overall capacitance, and exhibit different scaling behavior from MOSFETs (or any other device with an inversion channel, including the counterdoped tunneling transistors of Refs. [25–27]).

An ideal LITT device with an ultranarrow gate overlapping the lateral heavily-doped pn source–drain junction would require a specialized mask set with

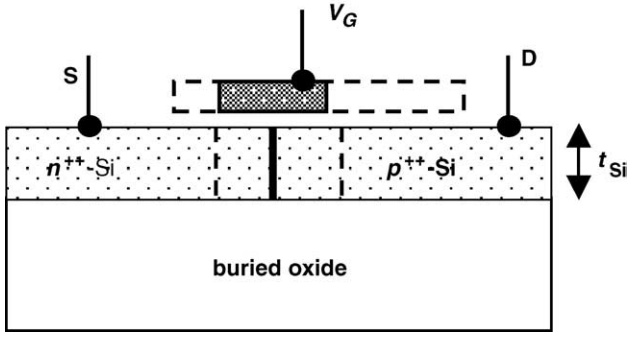

Fig. 5. Schematic layout of an LITT implemented in SOI, bold line marks the pn junction while the dashed lines indicate the corresponding lateral depletion region. In the ideal LITT, the gate overlaps the depletion region only to minimize capacitance (hatched); in the first fabricated prototypes, the gate overlapped source and drain space charge regions (dashed).

e-beam gate lithography at the limits of modern fabrication capabilities. On the other hand, proof-of-concept devices have been fabricated by a standard SOI MOS process with double implantation sequence employed for the source–drain pn junction [28]. After thinning the SOI Si channel to 40–50 nm Si thickness, the active area was doped p^+ by B implantation (in the $2–6\times10^{19}$ cm^{-3} range). After annealing to activate the B implant, half the active area was covered using a shifted active area mask level and the exposed source region was implanted n^{++} with P, aiming for $n^{++} \sim 10^{20}$ cm^{-3} effective doping (doping levels were estimated by Silvaco process simulation). Subsequent processing followed the standard MOS sequence with 4 nm deposited gate oxide and optical lithography for gate definition. The minimum gate length $L_G = 0.35$ μm was employed to ensure the overlap between the gate and the pn junction—however, this meant a significant overlap between the gate and the source and drain regions, as shown in Fig. 5. Good source and drain contacts were achieved even to the thinnest $t_{Si} \sim 40$ nm Si channels.

The room temperature $I_D(V_G/V_D)$ characteristics of reverse-biased ($V_D < 0$) LITT devices with ~40 nm Si film thickness, $L_G = 0.35$ μm gate length and 10 μm gate width, are shown in Fig. 6(a) for V_G ranging up to ±5 V. As expected, V_G of either polarity can turn the tunneling I_D current on at moderate drain bias $V_D = -1$ V. However, the required $|V_G| \geqslant 4$ V values are rather large, indicating a small built-in lateral electric field F due to insufficient junction doping levels. This explanation is consistent with the doping split dependence of the LITT characteristics: identically processed devices with lower doping on the p side exhibited even less current [28]. Furthermore, at $V_G = 0$, when the junction field F is almost entirely due to V_D, large reverse drain voltages ~ −3 V are required before I_D begins to flow, again confirming insufficient junction doping. As expected, the drain current in the LITT is independent of L_G.

Not only is the complex dependence of interband tunneling on the electric field F not well understood, but the spatial variation of F poses a difficult electrostatic problem. A given V_G accumulates one side of the np junction and depletes the other. As a result, the dependence of F and hence I_D on V_G polarity is asymmetric because of the differences in the doping level (n^{++} source more heavily doped than p^+ drain) and because of the workfunction difference between the n^+-poly-Si gate and the drain. Systematic Silvaco device simulations with the aim of correlating calculated maximum field F_{MAX} values with device parameters have been carried out, using both the actual double-implanted devices we fabricated experimentally and model devices with thinner Si channel and gate oxide, as well as abrupt pn junctions with a narrow L_G overlapping the depletion region only (see Fig. 5) [29]. A comparison of F_{MAX} as a function of V_G (for $V_D = -1$ V) for the real double-implanted device and a model device consisting of an ideally abrupt 1.5×10^{19}: 4.5×10^{19} cm^{-3} pn junction in a thinner $t_{Si} = 8$ nm channel with $L_G = 9$ nm and 2 nm gate oxide is shown in Fig. 6(b). Much higher F_{MAX} values for the

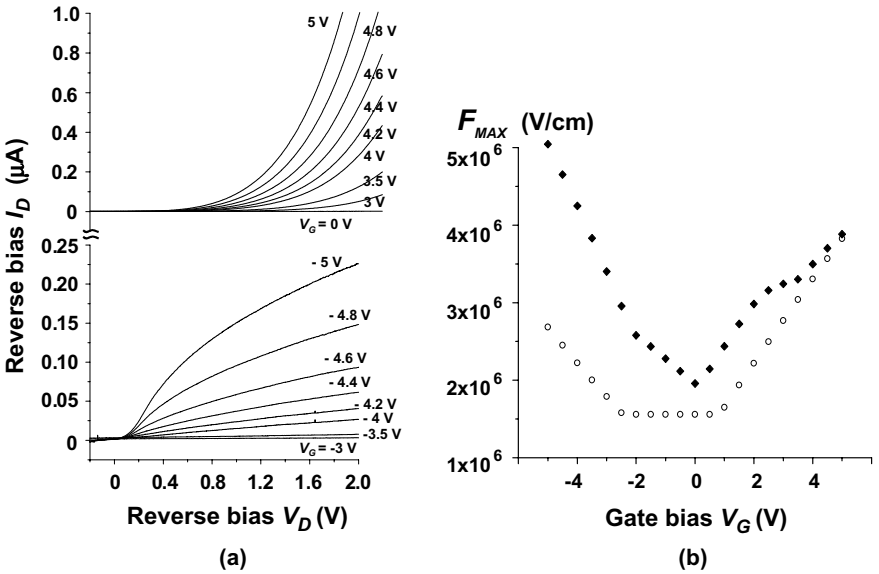

Fig. 6. (a) Reverse-bias $I_D(V_D, V_G)$ curves for LITT with pn junction doping of 6×10^{19}:10^{20} cm^{-3} at $T = 300$ K as a function of V_G (device parameters: $L_G = 0.35$ μm, $W = 10$ μm, Si film thickness $t_{Si} \sim 40$ nm, gate oxide ~5 nm). (b) Simulated maximum electric field F_{MAX} vs. V_G at $V_D = 1$ V in the fabricated double-implanted prototype devices (circles) and a model device with a perfectly abrupt pn 1.5×10^{19}:4.5×10^{19} cm^{-3} junction, thinner silicon channel $t_{Si} = 8$ nm, $L_G = 9$ nm, and 2 nm gate oxide (diamonds).

same biasing conditions would lead to higher transconductance and hence better performance. It should be noted that the asymmetry of F_{MAX} about $V_G = 0$ in the real device arises from the use of n^+-Si gate material. If this is undesirable, a mid-gap gate material with a symmetric workfunction with respect to the n and p sides of the LITT or an intentional pn doping asymmetry (as in the ideally abrupt device of Fig. 6(b)) will solve the problem. We also note that very thin SOI channels $t_{Si} < 10$ nm and oxides <2 nm have already been demonstrated in above-described VTT structures [20], and sub-10 nm gate lengths have also been reported in SOI MOSFET structures [30], so the main obstacle to the ideal LITT fabrication consists of aligning an abrupt junction with the gate.

Unlike a normal MOSFET, the LITT current has no obvious current saturation mechanism: I_D should increase with both V_D and V_G, limited only by extrinsic factors, such as series resistance in the contacts. If we consider LITT operated in reverse bias for high-speed analog amplification, the limitation on its high-frequency operation arises essentially from the capacitance, since there is no minority carrier storage. However, given the absence of the inversion channel, the gate capacitance in the ideal LITT of Fig. 5, where a narrow gate overlaps the source–drain depletion only, is minimal. As for the source–drain capacitance, it depends on the doping level of the pn junction. Even true Esaki diodes, with highly degenerate doping on both sides of the junction, have good high-speed response in forward bias [31]. In the LITT, the trade-off between source–drain capacitance (increasing with pn junction doping) and the tunnel resistance (decreasing with pn junction doping) will determine the proper design point.

It should be mentioned that the double implantation procedure employed to produce the first LITT devices is far from ideal, with the source region undergoing two high-dose implantations and the junction sharpness suffering from lateral diffusion during activation. Epitaxial regrowth of the source region would certainly be better, although the resulting nonplanar FET layout would complicate the gate level lithography. Like many other SOI device concepts, the LITT still awaits an optimized, technological fabrication process.

Finally, it should be emphasized that with source and drain contacts of opposite polarity, the LITT is not affected by short channel effects and does not obey the scaling limitations of a MOSFET. This may become critical for future end-of-the-roadmap ULSI devices.

5. Conclusion

In this paper we have briefly presented three device prototypes that had their beginnings in III–V heterostructures but can be advantageously implemented in SOI. More generally, the ultrathin Si layers becoming available in SOI, in combination with Si-based heterostructures, ultrathin oxides and other Si-compatible dielectrics, beckon device physicists and designers to transfer the entire arsenal of bandgap-engineered, size and charge quantized device ideas to the world of silicon technology.

Acknowledgements

We are grateful to S. Cristoloveanu, M. Mastrapasqua, and S. Deleonibus for useful discussions, and to D. Mariolle, C. Aydin and D. Fraboulet for technical assistance. The work at Brown and Stony Brook has been supported by the AFOSR MURI program (award #F49620-00-1-0331, managed by T. Steiner). S.L. has also been supported by the NY Center for Advanced Technology in Sensor Systems, funded by the NY State Office of Science, Technology and Academic Research (NYSTAR). A.Z. is grateful for a productive sabbatical stay in the Micro-electronics Department at LETI-CEA and visits to the IMEP-ENSERG laboratory in Grenoble.

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