HTML ABSTRACT + LINKS

Ultrathin epitaxial germanium on crystalline oxide metal-oxide-semiconductor-field-effect transistors

E. J. Preisler and S. Guha[a)]
IBM T. J. Watson Research Laboratory, Yorktown Heights, New York 10598

B. R. Perkins, D. Kazazis, and A. Zaslavsky
Division of Engineering, Brown University, Providence, Rhode Island 02912

(Received 31 January 2005; accepted 19 April 2005; published online 26 May 2005)

Ultrathin films of single crystal Ge (100 Å or less) have been grown epitaxially on a lattice matched high-κ crystalline oxide, lanthanum-yttrium-oxide, in turn grown on Si. Back-gated germanium-on-insulator field-effect transistors have been fabricated and measured from these germanium-on-insulator layers for Ge layers in the 30-600 Å range. The best devices exhibit an I_{on}/I_{off} ratio over 10^3 at room temperature and 10^5 at $T=77$ K. These ultrathin devices can be fully depleted and inverted, enabling both p and n channel operation in the same device. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1941451]

Germanium is increasingly being explored as a viable alternative to silicon in high performance field-effect transistors (FETs) due to its higher electron and hole mobilities and its compatibility with lower processing temperatures.[1] Any Ge based technology will likely be ultra-thin germanium-on-insulator (GOI) based, since substrate leakage and cost issues preclude a bulk Ge substrate based technology. In this article, we describe properties of all-epitaxial UTGOI field effect devices, as a step toward realizing this technology.

To date, GOI structures have been achieved either by wafer bonding,[2] selectively segregating Ge from a strained SiGe layer,[3] or most recently by liquid-phase epitaxial regrowth directly on a silicon substrate.[4] Here we examine FETs made in thin Ge layers grown on an epitaxial insulating template, in turn grown on a Si (111) substrate.[5,6] It is shown that these layers are suitable for device fabrication and that the epitaxial oxide, a lanthanum-yttrium oxide ternary that is lattice matched to silicon, can serve as a high-κ back-gate dielectric, enabling the fabrication of back-gated transistors. It is further shown that the thinnest GOI layers ($\leqslant 50$ Å) can be fully depleted and inverted by the back-gate voltage V_{GS}, making both N-channel and P-channel transistor operations available in the same device structure.

All of the structures used in this study were grown on n-type Si (111) substrates with resistivities of either 0.005 or 20 $\Omega\cdot$ cm. Wafers were cleaned with a standard HF-last (RCA) process and then introduced to vacuum. The wafers were outgassed to 740 °C after which approximately 50 Å of epitaxial silicon was grown to produce a flat and reproducible Si (7×7) reconstructed starting surface. Wafers were then transferred *in situ* to a second growth chamber where the epitaxial $(La_{0.27}Y_{0.73})_2O_3$ (hereafter LaYO) insulating layer was grown.[5] The LaYO layer was smooth and epitaxially aligned with the substrate as verified by a streaky reflection high energy electron diffraction pattern that repeated itself with every 60° of substrate rotation. Unintentionally doped, amorphous Ge was then deposited at room temperature followed by solid-phase epitaxial regrowth in the presence of an Sb surfactant as described elsewhere.[6] The Sb is not required for creating a single crystal GOI layer but serves to passivate the Ge, leading to a two dimensionally smooth Ge layer.[6] The LaYO layers ranged from 100 to 450 Å in physical thickness, whereas the GOI layers ranged from 30 to 700 Å. In some samples the Ge layers were capped with ~100 Å Al_2O_3 to passivate the top Ge surface.

In the initial set of samples grown on lightly doped Si (111) with 300 Å LaYO insulating layers, ring-shaped pseudo-FET (Ψ-FET) structures[7] were fabricated by lithographically defining Al metal contacts for annular source and drain, as shown in Fig. 1. The devices were isolated by etching the Ge down to LaYO using H_2O_2. There are no high-temperature steps in the process enabling the characterization of as close to "as-grown" GOI material as possible. Several sets of ring-shaped-gate Ψ-FETs with different effective channel (W/L) ratios (6.86, 5.72, 4.53 and 3.51) were fabricated for each GOI sample.

The $I_{DS}(V_{DS},V_{GS})$ Ψ-FET characteristics for devices with five different GOI thicknesses are shown in Fig. 1. The leakage current to the substrate was negligible, being below the scale shown in Fig. 1 for the current. In thick GOI, the

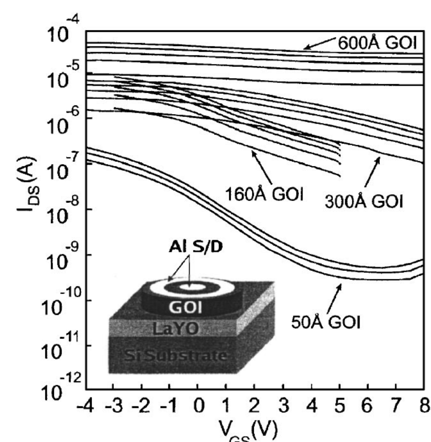

FIG. 1. Room-temperature $I_{DS}(V_{GS},V_{DS})$ characteristics of germanium-on-insulator ring-geometry Ψ FETs (see inset for geometry) vs Ge layer thickness, with $D=0.01-0.05$ V in 10 mV steps. The LaYO thickness was the same, 300 Å for all samples. All of the data shown are for Ψ FETs with an effective W/L ratio of 6.86.

[a)]Author to whom all correspondence should be addressed; electronic mail: guha@us.ibm.com

 © 2005 American Institute of Physics

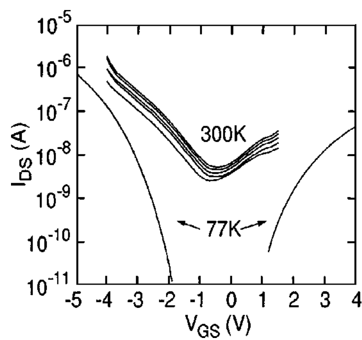

FIG. 2. $I_{DS}(V_{GS}, V_{DS})$ characteristics for a 50 Å Ge on 200 Å LaYO GOI back-gated transistors measured at T=300 and 77 K; V_{DS}=0.01–0.05 V in 10 mV steps for 300 K data and 50 mV for 77 K.

back gate shows little control over the drain current, and the FET cannot be turned off. However, as the GOI thickness is decreased, the transconductance increases and the residual I_{off} current at large $V_{GS}>0$ drops dramatically, by nearly five orders of magnitude. As the layer thickness at ~100 Å becomes comparable to the V_{GS}-induced depletion layer at the LaYO/Ge interface, the channel resistivity diverges. Note that all of the samples whose data are shown in Fig. 1 have the same 300 Å LaYO thickness.

A back-gated FET made from 50 Å GOI on 200 Å LaYO grown on a heavily doped *n*-Si (111) substrate was measured at both T=300 and 77 K and the data are shown in Fig. 2. At T=300 K, the channel current is minimized near $V_{GS}\sim -1$ V and is then increased for positive V_{GS}, indicating that the carrier polarity has been inverted; an I_{on}/I_{off} ratio of nearly 10^3 is measured in the best devices, as limited by gate leakage at large V_{GS}. At T=77 K, the channel current level decreases considerably, becoming negligible between −2 and +1.5 V and about five decades of subthreshold swing is achieved. Lower temperatures seem to freeze out the background channel carriers, increasing the on/off ratio of the device, but also increase the device contact resistance (we note that the contacts in these proof-of-concept devices were simple Al or Ti/Al metal evaporated directly onto the Ge layer). At T=77 K, the limiting factor in I_{on}/I_{off} ratio is leakage through the gate at high $V_{GS}<-5$ V.

Figure 3 shows the room temperature $I_{DS}(V_{DS}, V_{GS})$ characteristics on both logarithmic and linear scales of a FET made from a 30 Å GOI layer grown on 300 Å of LaYO, with a 100 Å Al_2O_3 cap layer. This FET was made with an effective channel length of ~10 μm, using Ti/Al evaporated metal contacts (the Al_2O_3 cap layer was removed by sputtering in a nitrogen plasma and then using HF). At this very small Ge layer thickness, the entire Ge layer can be thought of as the "channel" of the FET. The I_{on}/I_{off} ratio is not as large as the best device in Fig. 1, but still comparable to ultrathin SOI transistors[8,9] and bulk Ge FETs.[1] Significantly, this device is clearly ambipolar, with *P*-channel and *N*-channel operations available in the same structure as a function of V_{GS}. As can be seen in Fig. 3(a), the drain current I_{DS} is minimized at V_{GS}=−1 V and reasonably symmetric ambipolar characteristics are measured for $V_{GS}<-1$ V (*P* channel) and $V_{GS}>-1$ V (*N* channel). At high positive V_{GS} the transconductance is degraded, most likely by the asymmetric series resistance of the Ti/Al:Ge contacts. Still, as can be seen in the linear-scale output characteristics of Fig. 3(b), the *N*-channel and *P*-channel operations of the same

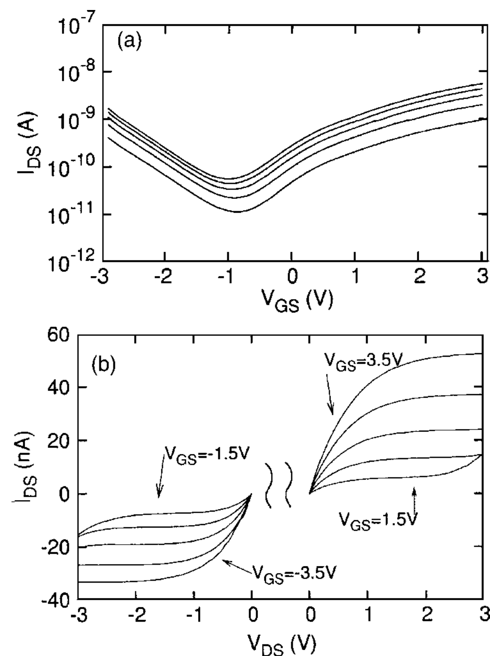

FIG. 3. Room temperature transistor characteristics of an ultrathin 30 Å Ge channel on 300 Å LaYO backgated GOI FET: (a) $I_{DS}(V_{GS})$ curves at V_{DS} =0.01–0.05 V in 10 mV steps; (b) $I_{DS}(V_{DS})$ curves at fixed V_{GS} values as shown. Note the good ambipolar transistor characteristics, with similar current drive for *N*-channel and *P*-channel operation of the same device.

device is reasonably symmetric, with comparable current drive at similar $|V_{GS}|$. As with the device in Fig. 2, the on-state current is eventually limited by the breakdown of the oxide at large V_{GS}. The gate leakage varies from device to device, indicating that the LaYO insulating layer is not completely uniform.

In order to correlate device performance with material parameters, we have simulated the operation of the back-gated FET shown in Fig. 3 on the Silvaco industrial device simulator.[10] In the simulation, the *n*-Si substrate was set to 10^{19} cm^{-3} *n*-type doping to match the substrates used in the real samples and the LaYO layer was modeled by an SiO_2 layer with a dielectric constant set to 18. A GOI layer of 30 Å thickness with various doping levels and otherwise standard Ge properties was used. The contact metal was set to have a work-function Φ_m=4.33, which corresponds to the titanium adhesion layer in the Ti/Al contacts. By changing the background channel doping level, the V_{GS} corresponding to the I_{DS} minimum changes, and can be adjusted to match the observed voltage. The result for two different *n*-Ge doping levels N_D is shown in Fig. 4. A doping level $N_D=8\times10^{18}$ cm^{-3} results in a minimum in conduction at about −1 V. Our simulation ignores interface charge, and possible charge dipole effects, so the actual value of N_D has a large uncertainty. Still, in both *P*-channel and *N*-channel operations, the subthreshold swing of measured and simulated characteristics is almost the same and equal to 1 V per decade. Although the qualitative agreement with the simulation is good, the overall current level in the real device at high V_{GS} is quite a bit lower than expected. This is probably due both to series resistance in the contacts and the likely degradation of Ge carrier mobility in the ultrathin GOI channel compared to bulk Ge. Improved contacts and Hall effect measurements on the ultrathin GOI layers are in progress to

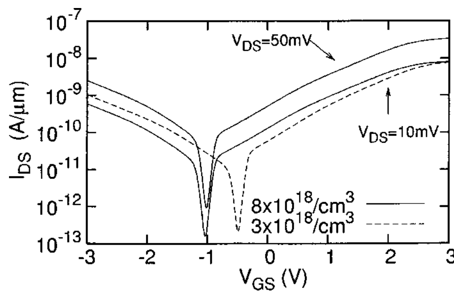

FIG. 4. Simulated $I_{DS}(V_{GS})$ characteristics at low V_{DS} for the sample of Fig. 3 for different background *n*-type channel doping levels N_D: solid lines — $N_D=8\times10^{18}$ cm^{-3} and $V_{DS}=10$ and 50 mV; dashed line - $N_D=3\times10^{18}$ cm^{-3}. The $N_D=8\times10^{18}$ cm^{-3} result corresponds best to the minimum channel conduction occurring at $V_{GS}\sim-1$ V, see Fig. 3.

determine the mobility and current drive of our GOI FETs as a function of structural parameters.

In conclusion, back-gated FET devices fabricated on ultra-thin GOI layers grown on an epitaxial insulating oxide on Si (111) have been demonstrated. The thinnest GOI layers show the hallmarks of a fully depleted layer, with very low intrinsic conductivity at a back-gate bias $V_{GS}\sim-1$ V. The application of V_{GS} below (above) −1 V can turn on the hole (electron) current I_{DS} in the channel. Given the very primitive contacting scheme, these proof-of-concept ambipolar FETs show good $I_{DS}(V_{GS},V_{DS})$ transistor characteristics with approximately equal current drive for *N*- and *P*-channel operations in the same structure. The I_{on}/I_{off} current ratio reaches three decades at room temperature and five decades at $T=77$ K, and is limited by the gate leakage at large V_{GS}. Future studies will focus on reducing the background doping in the Ge channel, improving the uniformity of the LaYO buried insulator, and developing an ohmic contacting procedure to the thin GOI layers.

The work at Brown has been supported by the AFOSR MURI program (Award No. F49620-00-1-0331, managed by T. Steiner) and the NSF (Award No. DMR-0223943). The Brown authors acknowledge use of the Microelectronics Central Facility at Brown, supported by the NSF MRSEC (Award No. DMR-0079964).

[1]H. Shang, K-L. Lee, P. Kozlowski, C. D'Emic, I. Babich, E. Sikorski, M. Ieong, H.-S. P. Wong, K. Guarini, and W. Haensch, IEEE Electron Device Lett. **25**, 135 (2004).
[2]C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M. F. Li, and D. L. Kwong, *IEEE Symposium VLSI Technology, June 2003*, p. 119.
[3]S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, Appl. Phys. Lett. **83**, 3516 (2003).
[4]Y. Liu, M. D. Deal, and J. D. Plummer, Appl. Phys. Lett. **84**, 2563 (2004).
[5]S. Guha, N. A. Bojarczuk, and V. Narayanan, Appl. Phys. Lett. **80**, 766 (2002).
[6]N. A. Bojarczuk, M. Copel, S. Guha, V. Narayanan, E. J. Preisler, F. M. Ross, and H. Shang, Appl. Phys. Lett. **83**, 5443 (2003).
[7]S. Cristoloveanu, D. Munteanu, and M. Liu, IEEE Trans. Electron Devices **47**, 1018 (2000).
[8]C. B. Oh, M. H. Oh, H. S. Kang, C. H. Park, B. J. Oh, Y. H. Kim, H. S. Rhee, Y. W. Kim, and K. P. Suh, *Tech. Digest IEDM, 2003*, p. 2.3.1.
[9]C. Fenouillet-Beranger, T. Skotnicki, S. Monfray, N. Carriere, and F. Boeuf, Solid-State Electron. **48**, 961 (2004).
[10]Our simulations were carried out using Silvaco's process simulation *Athena* (VER. 5.2.0.R) and device simulation *Atlas* (VER. 5.7.45.C) software packages.