Correct Biasing Rules for Virtual DG Mode Operation in SOI-MOSFETs

Akiko Ohata, Jeremy Pretet, Sorin Cristoloveanu, and Alexander Zaslavsky

***Abstract*—The appropriate biasing rules for virtual double-gate (DG) operation of silicon-on-insulator (SOI)-MOSFETs are investigated. The cause for the optimistic subthreshold swing, achieved by the conventional biasing rule, is discussed and a correct methodology is proposed. Furthermore, we select the proper threshold voltages for the virtual DG operation based on the condition that both interfaces are simultaneously inverted.**

***Index Terms*—Field-effect transistors (FETs), MOS devices, silicon-on-insulator (SOI) technology.**

I. Introduction

The fully depleted silicon-on-insulator (SOI) transistor with ultrathin bodies and double-gate (DG) architecture [1] is a promising candidate for the 10–20 nm channel length era. However, the experimental comparison of DG and single-gate (SG) MOSFETs is not easy. For example, triple-gate and gate-all-around DG MOSFETs cannot be operated in the SG mode. Comparing the DG and SG MOSFETs fabricated with different technologies is also debatable because material and processing issues can interfere with the purely physical mechanisms. The usual procedure is to operate the same transistor either in the SG mode or in the DG mode (i.e., the virtual DG operation) [2]–[4]. These measurements have produced useful insight but also astonishing results: a subthreshold swing below 60 mV/dec and a huge gain in the DG transconductance [3]. The purpose of this brief is to examine the appropriate biasing for a reliable comparison of the SG and DG modes.

II. Virtual DG Operation

Conventional DG operation is achieved when the inversion charges at the front and back channels are identical. This yields

$$V_{G2} - V_{T2} = \frac{t_{\mathrm{ox}2}}{t_{\mathrm{ox}1}}(V_{G1} - V_{T1}) \tag{1}$$

where $V_{T1,2}$ are the threshold voltages for the front/back channels, $V_{G1,2}$ are the front-/back-gate biases, and $t_{\mathrm{ox}1,2}$ are the front-/back-gate oxide thickness, respectively. It can be extended to the case of very thin films, where the front and back channels are no longer independent, being separated by a region of volume inversion [2], since the charge balance in (1) is independent of the coupling between the front and the back channels. In the following section, we will demonstrate that the biasing rule of (1) for the virtual DG operation should be used with extreme care.

The N-channel MOSFETs used for measurement have been fabricated at LETI (Grenoble) on standard Unibond wafers with 400-nm-thick buried oxide. The transistor body, left undoped (initial doping: $N_A = 5 \times 10^{14}$ cm^{-3}), has been thinned by sacrificial oxidation. The gate oxide was $t_{\mathrm{ox}1} = 4.5$ nm. The virtual DG transistor can be emulated by applying a voltage V_{G2} to the silicon substrate.

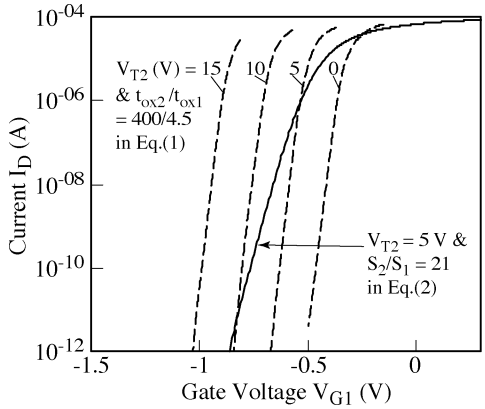

Fig. 1. Subthreshold characteristics in a virtual DG MOSFET biased according to (1) and (2). The solid line indicates the correct measurements using the bias conditions of (2): $\Delta V_{G2} = 21\ \Delta V_{G1}$ for $V_{T2} = 5$ V and $S_2/S_1 = 21$ (experimental values). The dashed lines show the wrong measurements according to (1) (i.e., $\Delta V_{G2} = 89\ \Delta V_{G1}$) for various offset voltages (V_{T1}, V_{T2}). V_{T1} is determined from I_D–V_{G1} measurements when a constant back-gate voltage (V_{T2}) is applied.

A. Weak Inversion

The dashed lines in Fig. 1 show the subthreshold characteristics in a virtual DG transistor, biased according to (1). The measured subthreshold swing appears to be $S = 30$ mV/dec. Similar overoptimistic results were reported in the literature. These results are of course unrealistic, simply because the minimum theoretical value at 300 K is $S_{\min} = 2.3kT/q \approx 60$ mV/dec.

The origin of the error is that, in weak inversion, the current increases exponentially with $(V_G–V_T)/S$, whereas in strong inversion $I_D \sim (V_G–V_T)/t_{\mathrm{ox}}$. In order for the front and back charges to be perfectly balanced, (1) must be replaced with

$$V_{G2}–V_{T2} = \frac{S_2}{S_1}(V_{G1}–V_{T1}) \tag{2}$$

where $S_{1,2}$ are the swings measured independently for the front and back channels (see the solid line in Fig. 1). $S_{1,2}$ can be written as [3]

$$S_{1,2} = 2.3\frac{kT}{q}\left(1+\frac{C_{\mathrm{it}1,2}}{C_{\mathrm{ox}1,2}}+\frac{C_{\mathrm{si}}}{C_{\mathrm{ox}1,2}}\frac{C_{\mathrm{ox}2,1}+C_{\mathrm{it}2,1}}{C_{Si}+C_{\mathrm{ox}2,1}+C_{\mathrm{it}2,1}}\right) \tag{3}$$

where $C_{\mathrm{si}} = \varepsilon_{\mathrm{si}}/t_{\mathrm{si}}$ is the depleted film capacitance, $C_{\mathrm{ox}1,2} = \varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}1,2}$ are front-/back-gate oxide capacitances, and $C_{\mathrm{it}1,2} = qD_{\mathrm{it}1,2}$ are interface-trap capacitances. Under the condition $C_{\mathrm{it}1,2} \ll C_{\mathrm{ox}1,2}$, S_2/S_1 can be rewritten as

$$\frac{S_2}{S_1} = \frac{t_{\mathrm{ox}2}}{t_{\mathrm{ox}1}}\frac{C_{\mathrm{si}}+C_{\mathrm{ox}2}}{C_{\mathrm{si}}+C_{\mathrm{ox}1}}. \tag{4}$$

Since $C_{\mathrm{ox}2} \ll C_{\mathrm{ox}1}$, the difference between the biasing rules of (1) and (2) is very significant: S_2/S_1 is always smaller than $t_{\mathrm{ox}2}/t_{\mathrm{ox}1}$. In our experiment, $S_2/S_1 = 21$ whereas $t_{\mathrm{ox}2}/t_{\mathrm{ox}1} = 89$. Thus, in the virtual-DG operation according to (1), an over voltage is applied to the back-gate (as compared with the front-gate voltage) so that the subthreshold swing, which is referred to the front-gate voltage, is underestimated.

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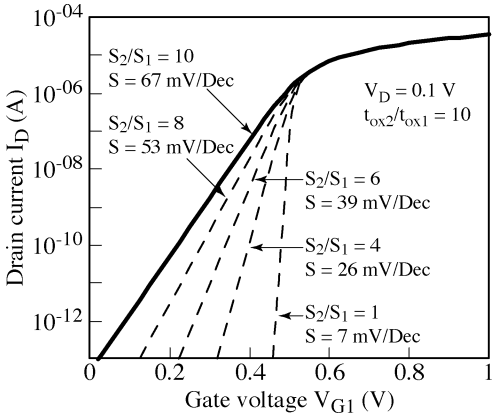

Fig. 2. Simulations using (1) for $t_{\mathrm{ox2}}/t_{\mathrm{ox1}} = 10$ (i.e., $\Delta V_{G2} = 10\ \Delta V_{G1}$) and various S_2/S_1 ratios. These curves have been obtained by using the model described reference [5] and by considering two independent channels (front and back). Only the bold curve is correct because for $S_2/S_1 = t_{\mathrm{ox2}}/t_{\mathrm{ox1}} = 10$, equation (1) is identical to the accurate (2).

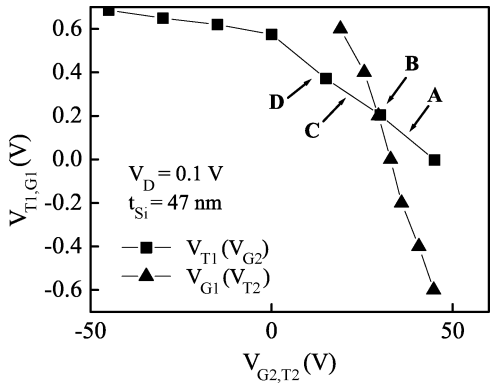

Fig. 3. Front-channel threshold voltage versus back-gate bias $V_{T1}(V_{G2})$ and back-channel threshold voltage versus front-gate bias $V_{G1}(V_{T2})$ for a 47-nm-thick transistor ($L = 10\ \mu$m, $W = 10\ \mu$m).

A clarifying example is provided in Fig. 2, where the DG curves have been simulated for a fixed ratio $t_{\mathrm{ox2}}/t_{\mathrm{ox1}} = 10$ and several ratios of S_2/S_1. For $S_2/S_1 = 1$, the bias according to (1) yields a record swing of 7 mV/dec. This extravagant result is due to the fact that the back-gate bias, imposed by (1) (i.e., $\Delta V_{G2} = 10\ \Delta V_{G1}$), was actually 10 times larger than that normally expected from (2) (i.e., $\Delta V_{G2} = \Delta V_{G1}$). The current increases mainly due to the back channel buildup. However, the swing is referred to the front-gate bias and artificially appears to be 10 times lower than the real value. For comparison, a proper device biasing according to (2) results in a reasonable value of 67 mV/dec; the bold curve in Fig. 2 was obtained for $S_2/S_1 = 10$ when (1) and (2) become identical and yield $\Delta V_{G2} = 10\ \Delta V_{G1}$. It is worth noting that in extremely thin transistors, where the film capacitance prevails, (1) and (2) are less contrasted.

B. Threshold Voltages for the Virtual DG Mode

We know that (1) is perfectly valid in strong inversion mode. However, $V_{T1,2}$ vary with the opposite gate bias. In general, $V_{T1,2}$ are improperly taken from measurements performed with the opposite gate grounded. The virtual DG operation implies that when one gate reaches inversion, the other gate should also be in inversion. This situation can be obtained by investigating the coupling effect between the front- and back-gate interfaces in the SG mode operation as explained below.

Fig. 3 shows the variation of both the front and back threshold voltages with the opposite gate bias. These relationships (i.e., the coupling effect) basically follow the theory [6]. The correct $V_{T1,2}$ values to be inserted in (1) are provided by point B, which represents the intersection of the two curves plotted in Fig. 3. Otherwise, the potentials at the two interfaces are unbalanced. Fig. 4 compares DG-like transconductance curves measured using several pairs of (V_{T1}, V_{T2}) values, corresponding to points A, B, C, and D in Fig. 3. Only curve B is representative of the genuine DG operation, while the other curves lead to an underestimate of the transconductance. Therefore, this proposed selection rule of threshold voltages for the virtual DG mode should be used for any comparison of SG and DG MOSFETs in terms of performance and scalability.

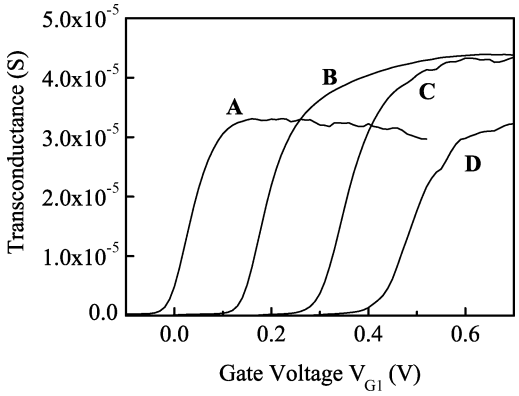

Fig. 4. Transconductance versus front-gate voltage for 47-nm-thick transistor ($L = 10\ \mu$m, $W = 10\ \mu$m) in the virtual DG mode: the offset voltages $V_{T1,2}$ in (1) correspond to points A, B, C, and D shown in Fig. 3.

III. Conclusion

The proper biasing rule for the virtual DG mode operation in SOI-MOSFETs was proposed. In weak inversion, the subthreshold swing ratio between the front and back channels should be used instead of the oxide thickness ratio. Furthermore, the threshold voltage of each interface should be chosen with the opposite interface in inversion. These correct threshold voltages can be obtained by investigating the coupling effect between the front and back interfaces. This method enables a reliable comparison between the SG and DG modes operation, which is useful to investigate scaling effects.

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