Negative Differential Resistance in Ultra-Thin Ge-On-Insulator FETs

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1. Introduction

As field effect transistors depart from the conventional Si/SiO_2 interface, because of gate leakage in extremely thin SiO_2 [1, 2], high-κ dielectrics open up new opportunities for semiconducting materials other than Si. Germanium is a promising candidate due to its higher and better matched electron and hole mobilities. Due to the cost and leakage of Ge substrates, most likely a Ge-based technology will be germanium-on-insulator (GeOI) based.

We report on ambipolar GeOI FETs fabricated on ultra-thin films of single crystal Ge, epitaxially grown on a high-κ crystalline lanthanum-yttrium-oxide lattice matched to Si (111) substrate. The GeOI FETs show promising transistor characteristics at room temperature, while at low temperatures they exhibit negative differential resistance (NDR) in the drain current circuit.

2. Material Growth and Device Fabrication

2.1. Structure Growth

The GeOI structures used in this study began with a 200 Å epitaxial $(La_{0.27}Y_{0.73})_2O_3$ layer (hereafter LaYO), grown lattice matched on a low-resistivity Si (111) *n*-type substrate. Amorphous Ge was then deposited at room temperature and recrystallized in the presence of a surfactant Sb monolayer, producing a smooth crystalline Ge layer of ~50 Å. A more detailed description of the growth and characterization of the LaYO and Ge layers can be found in [3, 4].

2.2. Device Fabrication

Simple FET devices, fabricated on this material structure, showing its potential use, were reported in [4], while the first ultra-thin, ambipolar devices were published in [5]. In this study, FETs were fabricated with improved source/drain contacts and a better fabrication procedure.

Source and drain were defined by optical lithography and Ti/Pd contacts of 850 Å were deposited using electron beam evaporation. The devices were isolated by etching the Ge layer using reactive ion etching and passivated using 2300 Å of PECVD SiO_2 deposited at 260 °C. The devices were annealed in forming gas for 30 min at 330 °C, which improved the subthreshold slope and current drive. Via holes were opened in the SiO_2 layer for Ti/Al bonding pads. Fabricated transistor W/L ratios are 200 µm/10 µm and 200 µm/5 µm. A schematic of the device is shown in Fig 1(a).

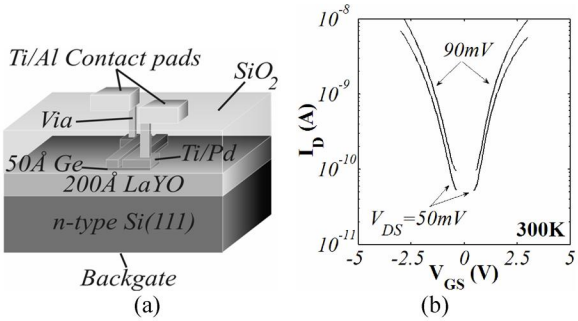

Fig. 1. (a) Schematic of the fabricated devices; (b) I_D-V_{GS} characteristics at T = 300 K.

3. Measurements and Results

3.1. Standard Transistor Characteristics

The highly doped Si substrate is used as a back-gate, with the LaYO layer as the gate dielectric. Room temperature I_D-V_{GS} characteristics are shown in Fig. 1(b) for a 10 µm long device. Clearly, the device is ambipolar, with both *P*-channel and *N*-channel operation available in the same structure, depending on the gate voltage. The device is remarkably symmetric, compared to previously published work [5], possibly due to compensation of the unintentional doping of the Ge layer. The I_{ON}/I_{OFF} ratio is about 100, which is comparable to [5] and other ultra-thin SOI transistors [6].

The I_D-V_{DS} characteristics for the same 10 µm ambipolar device are shown in Fig. 2 both for *N*-channel and *P*-channel modes. The characteristics are very symmetric with similar current drive at the same $|V_{GS}|$ and exhibit good drain current saturation. The current drive is quite low, even taking into account the ultra-thin Ge channel, possibly due to a high density of traps at the Ge/LaYO interface, as well as the residual doping in the Ge layer due to the Sb surfactant used in the recrystallization process [3]. Improvement in the interface quality is a key issue for GeOI device performance.

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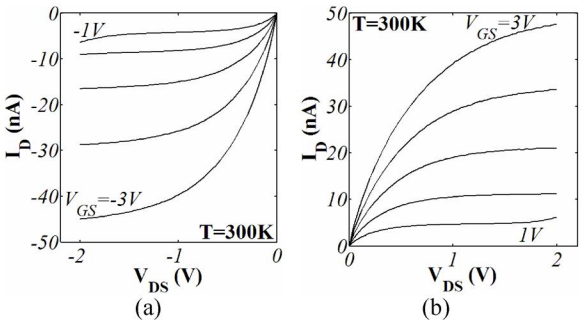

Fig. 2. (a) *P*-channel and (b) *N*-channel I_D-V_{DS} ambipolar FET characteristics at T = 300 K.

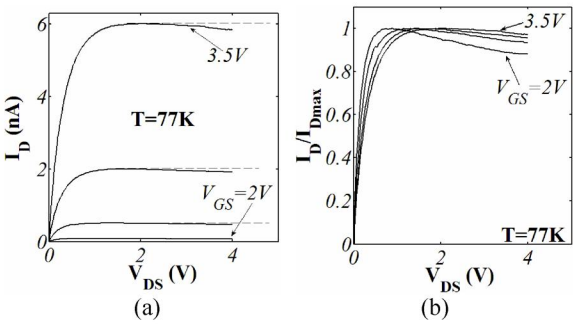

Fig. 3. (a) I_D-V_{DS} characteristics, with dashed lines marking perfect saturation; (b) normalized characteristics.

3.2. Negative Differential Resistance

The *N*-channel characteristics of the same transistor at T = 77 K are shown in Fig. 3(a). Instead of saturating perfectly, as at T = 300 K, the drain current reaches a maximum value and then decreases with increasing drain voltage, leading to negative differential resistance (NDR). A clearer picture of this NDR in the drain circuit is shown in Fig. 3(b), where the current is normalized by its maximum value for V_{GS} value. The relative peak-to-valley ratio is larger at smaller V_{GS}. The current peak position varies with electron density as well, shifting to higher drain voltages, for higher V_{GS}. The NDR effect is only observed for electrons and not for holes. It becomes somewhat stronger at lower T = 4.2 K, although higher V_{GS} are required to reach the same current drive at 4.2 K.

The observed NDR can arise from a number of phenomena. Like the celebrated Gunn effect in GaAs [7], NDR due to hot electron transfer to a low-mobility valley in the conduction band was also observed in pure bulk Ge at T < 130 K [8-10]. In our case, where the ultra-thin Ge channel is confined by LaYO and SiO_2 dielectrics, the electron energy is quantized into subbands due to the heavy and light effective masses along the (111) confinement direction. Since the in-plane effective mass is heavier in subbands arising from the light mass in the (111) direction [11], the NDR we observe may be due to intersubband transfer of electrons, analogously to the intervalley effect. However, NDR in a channel can also arise due to charge-trapping of hot electrons [12, 13] at the Ge/LaYO interface or at the top Ge/SiO_2 interface where the unintentional Sb doping of the Ge layer is possible.

4. Conclusions

In conclusion, back-gated ultra-thin GeOI FETs have been fabricated on Si substrates. These devices show ambipolar FET operation with symmetrical current drive in the *N*- and *P*-channel characteristics. At low temperatures the drain circuit exhibits NDR. Various circuit applications have been proposed for NDR devices, such as oscillators, multi-valued logic circuits and static memory cells. An all-epitaxial GeOI technology that could combine ambipolar Ge FETs with NDR devices (and possibly optoelectronic Ge-based devices), all on the same Si substrate, would be of great interest, provided the quality of the Ge channels is improved.

Acknowledgment

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References

[1] "*International Technology Roadmap for Semiconductors*", 2004 Update, http://public.itrs.net/

[2] J. Robertson and P. W. Peacock, *Microelectronic Eng.* **72**, 112 (2004).

[3] S. Guha, N. A. Bojarczuk and V. Narayanan, *Appl. Phys. Lett.* **80**, 766, (2002).

[4] N. A. Bojarczuk, M. Copel, S. Guha, V. Narayanan, E. J. Preisler, F. M. Ross and H. Shang, *Appl. Phys. Lett.* **83**, 5443 (2003).

[5] E. J. Preisler, S. Guha, B. R. Perkins, D. Kazazis and A. Zaslavsky, *Appl. Phys. Lett.* **86**, 223504 (2005).

[6] C. Fenouillet-Beranger, T. Skotnicki, S. Monfray, N. Carriere and F. Boeuf, *Solid-State Electron.* **48**, 961 (2004).

[7] J. B. Gunn, *Solid State Commun.* **1**, 88 (1963).

[8] B. J. Elliott, J. B. Gunn and J. C. McGroddy, *Appl. Phys. Lett.* **11**, 253 (1967).

[9] D. M. Chang and J. G. Ruch, *Appl. Phys. Lett.* **12**, 111 (1968).

[10] W. Fawcett and E. G. S. Paige, *J. Phys. C: Solid State Phys.* **4**, 1801, (1971).

[11] F. Stern and W. E. Howard, *Phys. Rev.* **163**, 816 (1967).

[12] T. King and D. K. Y. Liu, "*Charge Trapping Device and Method for Implementing a Transistor Having a Negative Differential Resistance Mode*", US 6479862, 2002.

[13] V. V. Afanas'ev, Y. G. Fedorenko and A. Stesmans *Mater. Sci. Semicond. Process.* **7**, 191, (2004)