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Negative differential resistance in ultrathin Ge-on-insulator FETs

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Abstract
In this paper we report on the fabrication of all-epitaxial ultrathin germanium-on-crystalline lanthanum–yttrium-oxide field effect transistors. The oxide is lattice matched to Si (1 1 1) and has a dielectric constant of ∼18. The transistors show ambipolar behaviour, both *N*- and *P*-channel operations on the same device at any temperature. The transistor characteristics have an ON/OFF ratio of 10^2 at room temperature, while at cryogenic temperatures negative differential resistance (NDR) is observed in the channel. The NDR effect, which is stronger for lower temperatures, can be attributed to a number of reasons from intervalley or intersubband electron transfer to a heavy transport effective mass (low mobility) band or to charge trapping. A germanium-on-insulator technology, provided the material (Ge and oxide) quality improves, may be useful for building circuits that combine conventional FETs with unconventional ambipolar or NDR devices all on the same substrate.

1. Introduction

For continued technology scaling, and as we approach the end of the roadmap around 2020, field effect transistors must depart from the conventional Si/SiO_2 interface. According to the ITRS [1], manufacturable solutions for gate dielectrics of equivalent oxide thicknesses (EOT) less than 9 Å that will be required after 2008 are currently not known. Gate leakage, due to direct tunnelling [2] in such extremely thin, sub-nanometre SiO_2 dielectrics, causes significant performance degradation and static power dissipation. High-κ dielectrics, on the other hand, can maintain the electrical characteristics of the thin SiO_2 dielectrics, while at the same time preventing excessive gate leakage. They are, therefore, possible candidates to replace SiO_2 in future CMOS devices.

However, the use of gate dielectrics other than SiO_2 opens up new opportunities for channel materials other than silicon. Germanium, which had long been forgotten in integrated circuit technology due to its unstable (water soluble) native oxide, is a possible candidate to replace silicon due to its higher and better matched electron and hole mobilities. Due to the cost and leakage of Ge substrates, any Ge-based technology is likely to be based on germanium-on-insulator (GeOI), with Si providing a convenient high-quality substrate.

In this paper, we report on ambipolar GeOI FETs fabricated on ultrathin films of single crystal Ge, epitaxially grown on a high-κ crystalline lanthanum–yttrium-oxide, lattice matched to an Si (1 1 1) substrate. The oxide has a dielectric constant of ∼18 [3]. The GeOI FETs show promising transistor characteristics at room temperature, while at low temperatures they exhibit negative differential resistance (NDR) in the drain current circuit. While the physical mechanism for the NDR effect is currently unclear, an improved quality material can possibly make it useful for device applications.

2. Material growth and device fabrication

2.1. Structure growth

The GeOI structures used in this study began with a highly doped Si (1 1 1) *n*-type substrate, on which 200 Å of lattice-matched $(La_{0.27}Y_{0.73})_2O_3$ (hereafter LaYO) were in turn grown epitaxially. Amorphous germanium was then deposited at room temperature and recrystallized in the presence of a surfactant Sb monolayer, producing a smooth single-crystalline germanium layer of ∼50 Å thickness. A more detailed description of the growth and characterization of the LaYO and Ge layers can be found in [4, 5].

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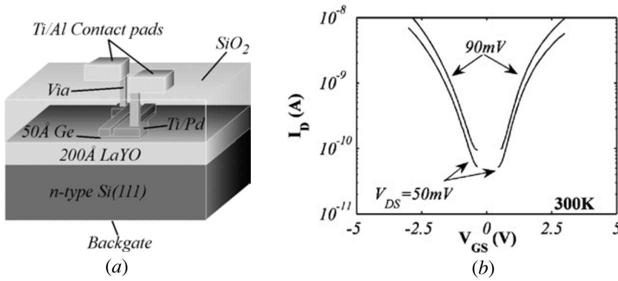

Figure 1. (*a*) Schematic of the fabricated devices; (*b*) I_D−V_{GS} characteristics at $T = 300$ K.

2.2. Device fabrication

Simple FET devices, fabricated on this GeOI material, showing its potential use, were reported in [5], while the first ultrathin, ambipolar devices were published in [6]. In this study, FETs were fabricated with improved source and drain contacts and passivation.

Source and drain were defined by optical lithography and Ti/Pd contacts of 850 Å were fabricated using electron beam evaporation and a lift-off technique. The devices were isolated by etching of Ge mesas using reactive ion etching. Then, 2300 Å of PECVD SiO_2 was deposited at 260 °C for device passivation and dielectric isolation for further metallization. The devices were annealed in forming gas for 30 min at 330 °C, which improved the subthreshold slope and current drive. Via holes were opened in the SiO_2 layer for Ti/Al bonding pads. Fabricated transistor W/L ratios are 200 μm/10 μm and 200 μm/5 μm. A schematic of the device is shown in figure 1(*a*).

3. Measurements and results

3.1. Standard transistor characteristics

The highly doped Si substrate was used as a back-gate, with the LaYO layer as the gate dielectric. Room temperature I_D−V_{GS} characteristics are shown in figure 1(*b*) for a 10 μm long device. Clearly, the device is ambipolar, with both *P*-channel and *N*-channel operations available in the same structure, depending on the gate voltage polarity. The device is remarkably symmetric, compared to previously published work [6], possibly due to compensation of the unintentional doping of the Ge layer. The I_{ON}/I_{OFF} ratio is about 100, which is comparable to [6] and other ultrathin SOI transistors [7].

The I_D–V_{DS} characteristics for the same 10 μm ambipolar device are shown in figure 2 both for *N*-channel and *P*-channel modes. The characteristics are very symmetric with similar current drive at the same $|V_{GS}|$ and exhibit good drain current saturation. The current drive is quite low, even taking into account the ultrathin Ge channel, possibly due to a high density of traps at the Ge/LaYO interface or the residual doping in the Ge layer due to the Sb surfactant used in the recrystallization process [4]. It is essential to improve the Ge/LaYO interface quality in order to improve the GeOI current levels, the subthreshold slope and the overall device performance of these GeOI transistors if this technology is to be used in actual devices.

3.2. Negative differential resistance

The *N*-channel characteristics of the same transistor at $T = 77$ K are shown in figure 3(*a*). Instead of saturating perfectly, as at $T = 300$ K, the drain current reaches a maximum value and then decreases with increasing drain voltage, leading to NDR. A clearer picture of this NDR in the drain circuit is shown in figure 3(*b*), where the current is normalized by its maximum value for V_{GS} value. The relative peak-to-valley ratio is larger at smaller V_{GS}. The current peak position varies with electron density as well, shifting to higher drain voltages, for higher V_{GS}. It becomes somewhat stronger at lower $T = 4.2$ K, as shown in figure 4, although higher gate voltages are required to reach the same current drive at 4.2 K. The NDR effect has been observed clearly and repeatedly for electrons. There is an indication of NDR for holes as well and measurements are underway to obtain a better picture of the effect in the *P*-channel operation.

It is unlikely that the observed NDR is due to self heating of the ultrathin GeOI channels. Self-heating effects observed in SOI MOSFETs at low temperatures [8] are stronger for high gate voltages and they disappear at low gate voltages. In our case, NDR is present and stronger for lower gate voltages, as shown in figure 3(*b*) and hence lower drain current levels and power consumption.

Except for self-heating, the observed NDR can arise from a number of phenomena. Like the celebrated Gunn effect in GaAs [9], NDR due to hot electron transfer to a low-mobility valley in the conduction band was also observed

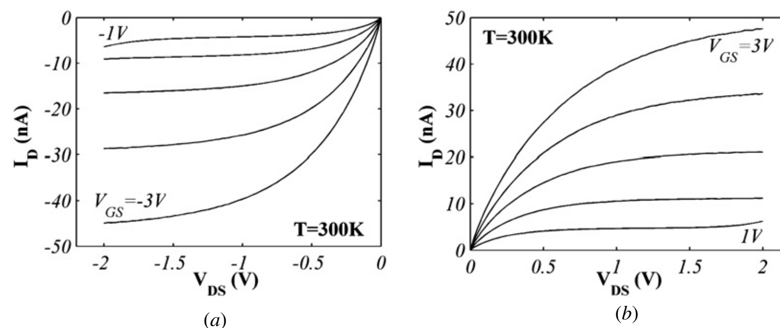

Figure 2. (*a*) *P*-channel and (*b*) *N*-channel I_D–V_{DS} ambipolar FET characteristics at $T = 300$ K.

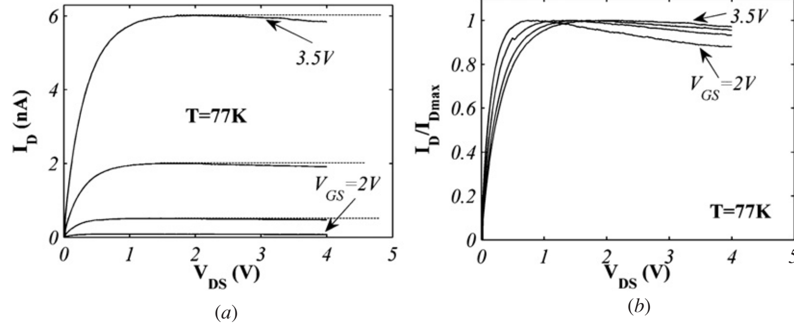

Figure 3. (*a*) I_D–V_{DS} characteristics, with dashed lines marking perfect saturation; (*b*) normalized characteristics at $T = 77$ K.

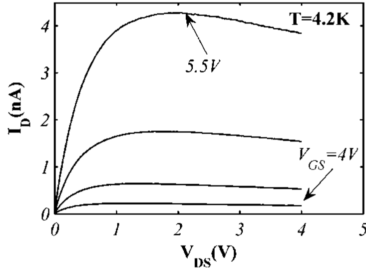

Figure 4. I_D–V_{DS} characteristics showing stronger negative differential resistance at 4.2 K.

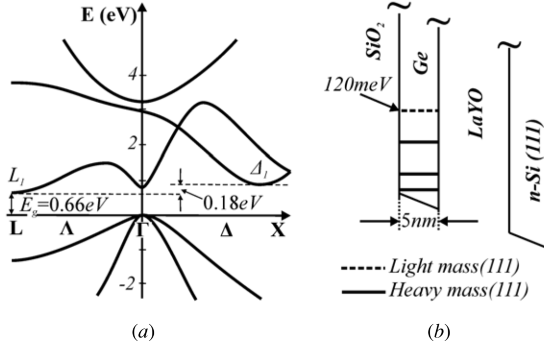

Figure 5. (*a*) Germanium band structure and (*b*) band diagram showing the quantized energy levels across the ultrathin germanium channel.

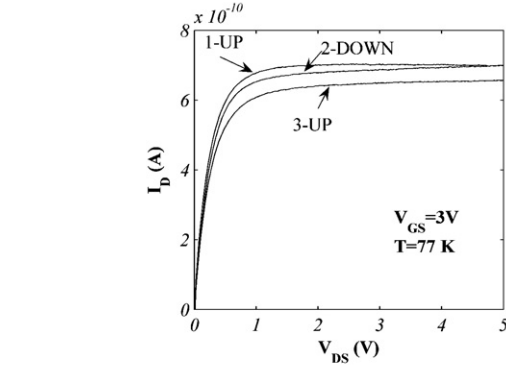

Figure 6. Continuous (non-stop) drain current measurement for drain voltages changing from 0 to 5 V (1-UP), 5 to 0 V (2-DOWN) and 0 to 5 V (3-UP) for $V_{GS} = 3$ V at $T = 77$ K.

in pure bulk Ge at $T < 130$ K [10–12]. The band diagram of germanium is shown in figure 5(*a*). The minimum of the conduction band of germanium lies at an *L*-point. Hot electrons can undergo a momentum space transfer to the Δ-minima of the conduction band. This band is characterized by a heavier effective mass (lower mobility), thus leading to negative differential resistance.

However, in our case, where the ultrathin germanium channel is confined by the LaYO and SiO_2 dielectrics, the electron energy is quantized into subbands due to the heavy and light effective masses along the (1 1 1) confinement direction, schematically shown in figure 5(*b*). The three lowest lying subbands, according to a finite square well calculation, with a barrier height of 2.3 eV [3], are due to the heavy mass along the confinement direction (1 1 1), whereas the fourth energy subband corresponds to the light mass along the confinement direction. The subbands arising from the light mass in the (1 1 1) direction correspond to a heavier in-plane (transport) mass, compared to the lowest levels [13]. An intersubband transfer of electrons from a light in-plane mass subband to a heavy in-plane mass could as well lead to the observed negative differential resistance, analogous to the intervalley transfer.

In addition, negative differential resistance in a transistor channel can also arise due to charge trapping of hot electrons [14, 15]. Interface traps located at the Ge/LaYO interface or at the top Ge/SiO_2 interface where the unintentional Sb doping of the Ge layer is possible could be the reason for the observed effect. As electrons are accelerated from the source by the drain voltage along the channel, they get trapped by interface traps and never make it to the drain, thus reducing the overall density of mobile carriers in the channel. Such high-field-induced electron trapping has been observed in GaAs/AlGaAs structures [16]. This loss of carriers can lead to a decrease in the drain current with increasing drain voltage. By performing a loop measurement of the drain current versus the drain voltage at low temperatures, where the NDR effect is observed, we can determine whether we lose carriers with increasing drain voltage or not. The measurement, shown in figure 6, starts off at zero drain voltage, which is swept up to 5 V, then without stopping down to 0 V and then back up to 5 V. As can be seen in figure 6, there is a difference in the measured current for the three sweeps, proving that indeed some of the carriers are lost, possibly due to charge trapping at the germanium/oxide interfaces. Nevertheless, whether this is the reason for the observed NDR effect or not is not something that can readily be extracted from this measurement and further investigation of the effect based on *C*–*V* measurements is in progress to determine the interface trap density.

4. Conclusions

In conclusion, back-gated ultrathin GeOI FETs have been fabricated on Si substrates. Current transport measurements have been performed in order to characterize the material quality and test the device performance at room and cryogenic temperatures. These devices show ambipolar FET operation with symmetrical current drive in the *N*- and *P*-channel characteristics. At low temperatures the drain circuit of *N*-channel devices exhibits NDR, which becomes stronger for lower temperatures. Capacitance measurements at low and high frequencies are currently being conducted for a more thorough characterization of the material structure and the interface state density.

Various circuit applications have been proposed for NDR devices, such as oscillators, multi-valued logic circuits and static memory cells. An all-epitaxial GeOI technology that could combine ambipolar Ge FETs with NDR devices (and possibly optoelectronic Ge-based devices), all on the same Si substrate, would be of great interest, provided the quality of the Ge channels is improved.

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