Tunneling field-effect transistor with epitaxial junction in thin germanium-on-insulator

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We report on the fabrication and electrical characterization at room and low temperatures of a tunneling field-effect transistor (TFET). The devices are fabricated in thin germanium-on-insulator and consist of a heavily p^+-doped, epitaxially grown source, a heavily n^+-doped ion implanted drain, and a standard high-κ (HfO_2) gate stack with an effective gate length L_{eff} of 60 nm, obtained by trimming. The TFETs are fabricated using an ultralarge-scale integration compatible process flow. The devices exhibit an ambipolar behavior, reasonable on/off current ratio, and improved on current compared to silicon-on-insulator TFETs. © *2009 American Institute of Physics*.
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For the past decades silicon technology has relied almost completely on downscaling metal-oxide-semiconductor field-effect transistors (MOSFETs).[1] However, there is great need for both unconventional materials and devices, to extend the complementary metal-oxide-semiconductor (CMOS) technology to the end of the roadmap and beyond. The move from bulk CMOS to silicon-on-insulator (SOI) has so far enhanced the performance of the devices,[2] while the replacement of the standard polycrystalline silicon/SiO_2 gate stack with metal/high-κ dielectric gate stacks is already a reality.[3,4] Moreover using channel materials other than silicon to enhance or better match the electron and hole mobilities is being considered. At the same time, even in an ideal MOSFET, the diffusion subthreshold current can only change at a maximum rate of $S=2.3(kT/q) \sim 60$ mV/decade at room temperature.[5] This ideal subthreshold slope is further degraded in practical devices, due to short-channel effects and interface imperfections. A sharp subthreshold slope is necessary in order to scale down the supply voltage and maintain at the same time a high I_{ON}/I_{OFF} current ratio and a high I_{ON} current. However, even with the ideal slope, an ultimate transistor would need a supply voltage of about 0.5 V. In order to further lower the supply voltage, a device based on an alternative principle of operation is necessary. One such device is the proposed interband tunneling FET (TFET), whose subthreshold current is not due to source-drain diffusion. In a TFET the gate voltage controls the interband tunneling between source and drain. The fundamental idea dates back to a proposal by Shockley and Hooper[6] of a gated *pn* junction operated in avalanche mode and is now of interest because simulations show that the TFET can exhibit sharper turn-off characteristics than ideal CMOS transistors.[7,8] Recently, Choi *et al.*[9] and Mayer *et al.*[10] have experimentally demonstrated SOI TFETs with 53 and 42 mV/decade slopes, respectively. Earlier, TFETs were demonstrated in III-V,[11] and later in bulk silicon[12,13] and SOI.[14,15] However, whether SOI or bulk, Si TFETs suffer from low I_{ON} currents.[9,15] Interband tunneling depends largely on the semiconductor bandgap E_G and the maximum electric field E_{max} at the junction;[16] this is the main reason why Si interband tunneling devices are characterized by low currents (Si $E_G \sim 1.1$ eV).

A TFET capable of meeting the I_{ON} requirements of the roadmap[1] would benefit from a narrower bandgap than that of Si. Germanium is a very promising candidate, with a bandgap of ~ 0.66 eV, as well as higher mobilities than Si. Due to the cost and scalability limitations of bulk Ge substrates, the most interesting Ge-based FETs are in germanium-on-insulator (GeOI),[17–19] so integrating TFETs in such a platform would be ideal. In this letter, we report on the design, fabrication and characterization of a TFET based on thin GeOI of ~ 60 nm. The Ge TFET shows I_{ON} currents comparable[9] or higher[10] than recently reported Si TFETs.

A schematic cross section of the device is shown in Fig. 1(a). The GeOI channel of 60 nm thickness obtained by condensation[18] is lightly p^--doped. The heavily p^+-type source of the transistor is formed with selective epitaxial

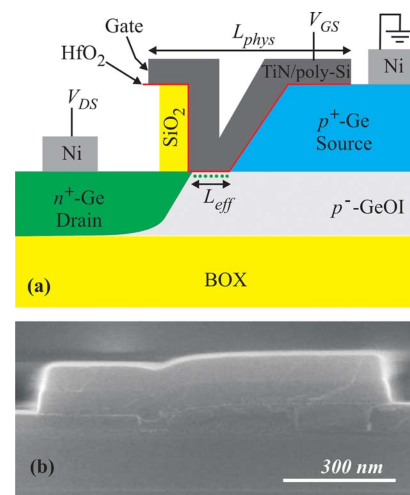

FIG. 1. (Color online) (a) Schematic cross section of the GeOI TFETs with the epitaxial *pn* junction at the source/channel interface and effective gate length of 60 nm and (b) SEM cross section, where the angled, epitaxial source can clearly be seen.

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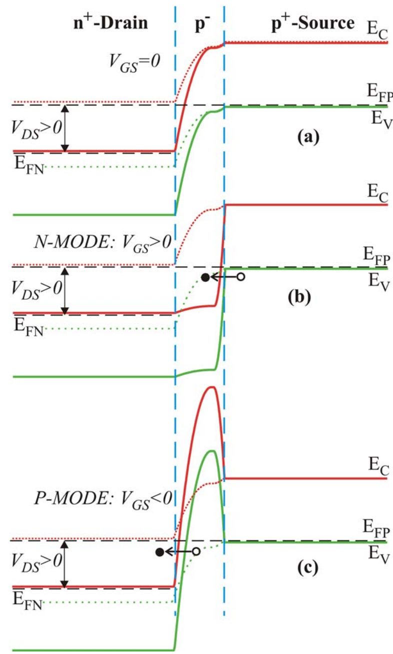

FIG. 2. (Color online) Band diagrams illustrating the electron interband tunneling in a TFET for various gate voltages and $V_{DS}>0$. Dashed lines show the bands for $V_{DS}=V_{GS}=0$. (a) For $V_{GS}=0$ the barrier for interband tunneling is large. (b) For $V_{GS}>0$ (N-mode) electrons tunnel from the valence band in the p^+-source into the conduction band in the channel. (c) For $V_{GS}<0$ (P-mode) electrons tunnel from the valence band in the channel to the conduction band in the n^+-drain.

growth (80 nm *in situ* boron-doped Ge) in half of the active area, while the rest of it is covered by an oxide mask. The epitaxial source is grown at an angled facet (~35° from the normal), as shown in Fig. 1. The oxide is then trimmed by 60 nm to produce the desired effective channel length. Subsequently, a standard high-κ (6 nm HfO_2) dielectric with a TiN/polycrystalline silicon electrode gate stack is fabricated. Optical lithography is used to pattern the gates with physical lengths L_{phys} down to 400 nm. The oxide mask is then removed at the drain side with controlled overetching under the gate and the highly doped drain is formed by n^+-type As implantation at a high 55° tilt angle, followed by annealing at 600 °C for 1 min. To save processing steps, instead of a full back-end process, these prototype TFETs had Ni contacts (60 nm) deposited by evaporation/lift-off and annealed in forming gas at 355 °C for 20 min. The devices are passivated with 200 nm of plasma-deposited SiO_2, which also serves as a dielectric for bonding pad fabrication. A scanning electron microscope (SEM) cross section of a typical TFET right after gate stack fabrication is shown in Fig. 1(b). The epitaxially grown, angled source of the transistor can clearly be seen in the image.

Similarly to other TFETs,[10,13] our GeOI TFETs are ambipolar devices and can operate in two modes (P-mode and N-mode) depending on the gate bias, as explained using schematic band diagrams in Fig. 2. When the gate voltage is low ($V_{GS}\sim 0$), there is no inversion channel formed, nor is there accumulation of holes, and therefore the barrier for tunneling is large, as shown in Fig. 2(a) for a positive drain bias. For positive $V_{GS}>0$, channel inversion occurs and a narrow tunneling barrier now exists at the p^+-source and inverted channel interface, with electrons tunneling from the valence band in the source to the conduction band in the

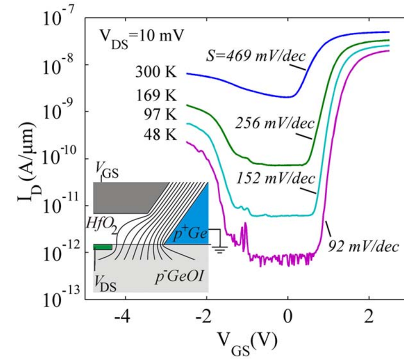

FIG. 3. (Color online) Measured $I_D(V_{GS})$ characteristics of a TFET with $W=10$ μm and $L_{eff}=60$ nm for $V_{DS}=10$ mV at $T=48-300$ K for both N- and P-modes of operation. Subthreshold slopes for N-mode operation are listed. Simulated equipotential lines at the corner source/channel junction are shown in the inset for a configuration analogous to the TFET, with $V_{GS}=V_{DS}=1$ V and the source grounded. The channel is assumed to be an equipotential at V_{DS}. The lines are denser in the vicinity of the junction, where the electric field is maximum.

inverted channel, as shown in Fig. 2(b) (N-mode operation). For negative $V_{GS}<0$, holes are accumulated in the channel under the gate and the tunneling barrier now exists at the drain side, as illustrated in Fig. 2(c) (P-mode operation), with electrons tunneling to the conduction band in the n^+-drain. The asymmetric geometry of the TFET (epitaxial source versus implanted drain and the corner source/channel junction) makes its performance better for N-mode operation ($V_{GS}>0$).

Figure 3 shows the measured ambipolar transfer characteristics of a TFET at a low drain voltage $V_{DS}=10$ mV at various temperatures between 48 and 300 K. It is clear from the measurement that the current is increased when the tunneling occurs at the epitaxial source/inverted channel interface, compared to the case when tunneling occurs at the implanted drain/channel interface. The difference in the I_{ON} currents is more than a decade at room temperature. As the temperature is lowered, the I_{OFF} current is significantly improved, while in the range of 50–300 K, the I_{ON} current is only decreased by half a decade for the N-mode operation and about two decades for the P-mode one. This decrease in the I_{ON} current is primarily due to the Ge bandgap increase as the temperature is reduced[16] (the bandgap at 48 K is 76 meV larger than at 300 K). This is verified by temperature simulations of the tunneling probability, which has an exponential dependence on $-E_G^{3/2}$.[16] The subthreshold slope is improved as the temperature is decreased (from 469 mV/decade at room temperature to 92 mV/decade at 48 K), combined with an increase in threshold voltage by about 0.5 V. Since the tunneling current does not depend on temperature as the subthreshold current in a standard MOSFET does, one would not expect an improvement in the subthreshold slope with decreasing temperature. However, there is a component in the I_{OFF} due to the thermally generated reverse leakage current flowing from the p^+-source through the p^--Ge body into the n^+-drain, which is temperature-dependent and is suppressed at cryogenic temperatures. This I_{OFF} current suppression appears as an improved subthreshold slope.

Figure 4 shows the room temperature $I_D(V_{GS})$ of the TFET for $V_{DS}=10$ mV, 100 mV and 500 mV. It is clear from this measurement how a higher drain bias (lateral electric field) increases the tunneling current by adding to the maxi-

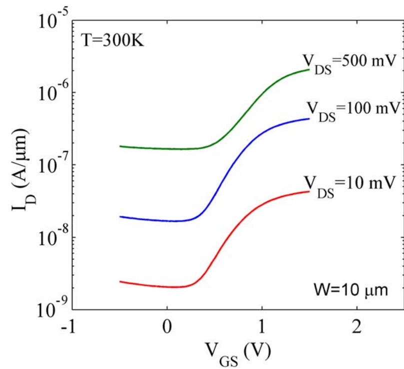

FIG. 4. (Color online) Measured room temperature $I_D(V_{GS})$ characteristics of the TFET in N-mode operation ($V_{GS}>0$) for $V_{DS}=10$, 100, and 500 mV.

mum electric field at the junction. Both the I_{ON} and I_{OFF} currents are increased with increasing drain bias.

The geometry of our TFET has advantages over the standard counter-doped implanted TFETs.[9,10,15] First, the highly p^+-doped source epitaxially grown on the lightly p^--doped Ge layer can provide a more abrupt pn tunneling junction than can be produced by standard implantation. Also, since the epitaxial source is grown at an angle, the pn junction where tunneling will occur in N-mode operation is located at a corner, where the electric field E is concentrated[20] and therefore the gate controlled tunneling current is further increased. Simulated equipotential lines in the vicinity of the source/channel junction, in a geometry analogous to the TFET are shown in the inset of Fig. 3. The Poisson equation was solved for $V_{GS}=V_{DS}=1$ V, while the source was grounded. For this qualitative simulation, the channel potential was assumed to be an equipotential at V_{DS} with respect to the source. It is clear that very close to the corner junction the density of the equipotential lines and therefore the electric field E is large.

However, the performance of the fabricated Ge TFET is far from ideal and the turn-on of the tunneling I_{ON} is not as sharp as expected for a tunneling transistor. The subthreshold slope for 300 K (N-mode operation) is 469 mV/decade, as shown in Fig. 3. The reason for the degraded turn-on characteristic is twofold. On one hand, it is a result of the well-known difficulty in achieving high n-type doping in Ge, due to the low dopant solubility in Ge and fast dopant diffusion during activation. On the other hand, it is due to the large buildup of negative charge at acceptorlike states at the HfO_2/GeOI interface.[21] Both of these reasons contribute to the degraded performance of n-channel devices in Ge compared to p-channel ones.[17] In the case of the TFET, this problem mainly leads to the degraded performance for P-mode operation, where tunneling occurs at the drain side. When the ambipolar behavior is undesirable, this issue can actually be an advantage, as the current in the P-mode will be suppressed. Another issue with the fabrication of the TFET is also related to the n-type implantation that is done at a high angle. Ideally the physical gate length L_{phys} should be slightly larger than L_{eff}, in order for the n-type dopants to reach the edge of the gate (see Fig. 1). Unfortunately in the present work, lithography limitations on $L_{phys}>350$ nm kept it larger than L_{eff}, which results in a p^- region between the n^+-drain and the gated part of the channel, corresponding to increased series resistance and therefore degraded I_{ON} currents. This limitation is not a fundamental one.

In conclusion, TFETs have been fabricated in thin GeOI with an epitaxially grown p^+-source that creates a more abrupt junction compared to a typical implanted one. The way the source is selectively grown at an angle helps concentrate the maximum electric field at the tunneling junction and therefore increases the performance of the transistor. The devices with effective channel lengths of 60 nm can work in two modes, for different gate biases and exhibit improved I_{ON} currents compared to reported silicon TFETs. This device is a potential candidate for future low-power, room temperature applications.

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