# Markov Chain Analysis of Thermally Induced Soft Errors in Subthreshold Nanoscale CMOS Circuits

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***Abstract*—The development of future nanoscale CMOS circuits, characterized by lower supply voltages and smaller dimensions, raises the question of logic stability of such devices with respect to electrical noise. This paper presents a theoretical framework that can be used to investigate the thermal noise probability distributions for equilibrium and nonequilibrium logic states of CMOS flip-flops operated at subthreshold voltages. Representing the investigated system as a 2-D queue, a symbolic solution is proposed for the moments of the probability density function for large queues where Monte Carlo and eigenvector methods cannot be used. The theoretical results are used to calculate the mean time to failure of flip-flops built in a current 45-nm silicon-on-insulator technology modeled in the subthreshold regime including parasitics. As a predictive tool, the framework is used to investigate the reliability of flip-flops built in a future technology described in the International Technology Roadmap for Semiconductors. Monte Carlo simulations and explicit symbolic calculations are used to validate the theoretical model and its predictions.**

***Index Terms*—CMOSFET logic devices, Laplace transform, Markov process, Monte Carlo method, Poisson distribution, reliability.**

## I. Introduction

DURING the last decades, advance in silicon technology has been driven by continuous downscaling of CMOS transistors, with predicted trends presented in the International Technology Roadmap for Semiconductors (ITRS) roadmap [1]. While the scaling of the supply voltage $V_{\rm dd}$ has been considerably slower than the transistor size scaling, there is a strong incentive to further reduce $V_{\rm dd}$ in order to limit the overall power dissipation. By 2015, CMOS device dimensions are expected to reach gate lengths $L_{\rm G} \approx 10$ nm while the $V_{\rm dd}$ of low-power CMOS is predicted to reach 0.5 V by 2016, then stay at that level for the next years. Lower voltages $V_{\rm dd} \approx 0.3$ V have also been predicted for later years [2].

If, for a specific application, power reduction takes precedence over performance, the option of further reducing $V_{\rm dd}$ into the subthreshold regime could prove useful. Computing circuits such as biomedical implants, environmental monitoring devices, space systems, or other battery-operated mobile applications are required to function under considerable energy constraints in order to increase their operation life. The quadratic dependence of dynamic energy on the supply voltage suggests that an efficient technique for low-power digital electronics is supply voltage scaling. It has been shown that the minimum energy is typically achieved when $V_{\rm dd}$ enters the subthreshold region [3].

An increasing number of papers have been published on ultralow-voltage digital circuits, as means of minimizing the overall energy consumption [4], [5] and exploring the challenges of ultralow-voltage memory design [6], [7]. A functional sub-200-mV 8-b processor for use in ultralow-energy sensor systems has recently been reported [8]. However, by operating the devices at ultralow $V_{\rm dd}$, the noise margins are reduced and reliability becomes a concern.

Reliability analysis is usually performed using simulation in a Monte Carlo framework. When applied to large circuits, this method requires considerable computational resources or is inefficient [9]. For the system considered in this paper, in a flip-flop circuit, the inefficiency of the Monte Carlo method stems from the exponential dependence of the computational time on the number of electrons stored in the node capacitances of the flip-flop. Therefore, an analytical method is needed to assess the logic stability of such devices, as designers will try to balance the constraints of performance, power dissipation and reliability.

This paper outlines the limitations of the Monte Carlo simulations for predicting the reliability of a CMOS flip-flop and presents a theoretical framework that can predict the soft error rates for given device dimensions, noise source, and $V_{\rm dd}$. The proposed framework is applied to calculate the failure rates due to thermal noise of flip-flops built in a cutting edge silicon-on-insulator (SOI) technology operated at subthreshold $V_{\rm dd}$. The theoretical results are also used to investigate the reliability of flip-flops built in an ultimate (2022), low operating power CMOS technology, as predicted by the ITRS roadmap [1].

Previous work on soft error analysis has mostly been confined to two frameworks. The first one is the analysis of soft errors through simulation of the effect of charge bursts on circuit models [10]. The second approach is to propagate discrete probabilities through logic networks using transition matrices

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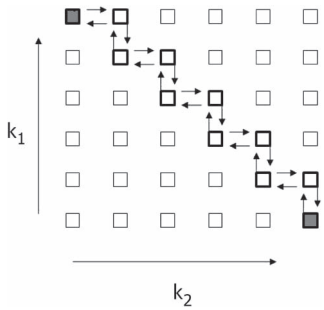


Fig. 1. Two-dimensional queue with the available states for CMOS flip-flop. The full queue can be reduced with a good approximation to a 1-D diagonal queue [13] with $k_1$ and $k_2$ electron populations on the two inverters. The filled squares depict the stable states of the flip-flop.

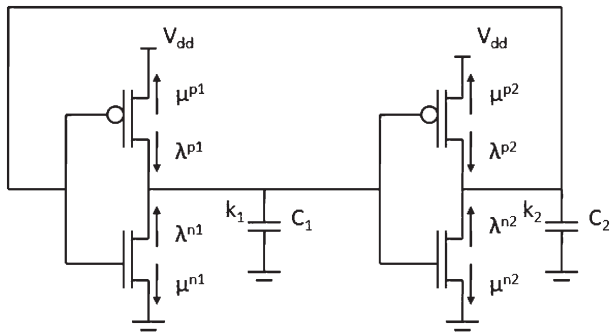


Fig. 2. Modeled flip-flop circuit. Capacitors $C_1$ and $C_2$ represent the node capacitances associated with each inverter. For each transistor, the charging and discharging rates $\lambda$ and $\mu$ determine the electron populations on the node capacitances.

or other propagation methods [11]. Compared with these approaches, the analytic framework introduced in [12] and [13] and extended in this paper allows for analysis of error probability over vast intervals of time not achievable through simulation, and has the ability to capture dynamic circuit behavior not possible through discrete probability propagation.

An important reference for the work presented here is the paper by Sarpeshkar *et al.* [14] on Poisson-noise modeling in subthreshold MOS transistors. It has been shown in the referenced paper that the subthreshold drain current noise fluctuations are equivalent to the difference between a forward and reverse drain current, each of which is characterized by pure shot noise.

In [12], a model was introduced for the distribution of shot noise as a Poisson process with independent distributions for the arrival and departure of carriers at a drain or source node. In [13], this model was extended by application of queuing theory to represent the storage of charge on the flip-flop gates or other parasitic capacitances. The capacitance of a node is modeled as a queue where the CMOS drain current fluctuations are considered to be random arrival and departure events. This type of queue is known as a birth–death queue and can be modeled as a Markov chain [15]. The result is a 2-D queue that contains all the available states for the system considered in terms of the number of electrons $k_1$, $k_2$ on the two inverters nodes. When applied to a flip-flop, the 2-D queue can be reduced with a good approximation to a 1-D queue represented by the step diagonal of the full queue, as shown in Fig. 1.

The 1-D queue is solved under the assumption that the transitions between available states represent independent Poisson processes. The arrival and departure of electrons at node capacitances can be modeled as Poisson processes only in subthreshold regime [14]. In MOS operation above threshold, there are sufficient carriers in the channel that electromagnetic interaction between them cannot be neglected. Their collective modulation of the surface potential alters the current–voltage relationship in the device and dielectric relaxation partially masks the effects of intrachannel scattering [16]. As a result, our model can only evaluate the reliability of logic devices operated at subthreshold voltages.

Within the theoretical framework outlined in [13], this paper extends the analysis to flip-flop devices with parasitics and presents the expressions of the probability density function moments that characterize the 1-D queue: mean, variance, skewness, and kurtosis. This moments, in turn, make it possible to evaluate the average and cumulative failure rates of flip-flop-based circuits.

The novelty of the proposed framework comes from the use of Markov chain and queuing theory to describe the thermal fluctuations of electron populations in a flip-flop. The complete solution for the diagonal queue approximation allows for a rapid calculation of error rates regardless of the number of electrons stored in the node capacitances.

The rest of this paper is organized as follows. Section II presents the flip-flop circuit model, its representation as a 2-D queue, and the limitations of Monte Carlo simulations. In Section III, the 2-D queue is reduced to a 1-D queue and the solution for the 1-D diagonal queue is presented. Section IV presents the mean time to failure for a flip-flop built in a modern fully depleted (FD) SOI technology as a function of $V_{\rm dd}$. Section V presents the mean time to failure for a flip-flop built in an ultimate ITRS roadmap predicted technology. Finally, Section VI presents the conclusions.

## II. Flip-Flop Circuit Model

The logic circuit to be modeled is a bistable flip-flop, consisting of two cross-coupled inverters (see Fig. 2) [13]. The two inverters are connected with positive feedback enabling the flip-flop to reside in either of two stable operation points ($V_{\rm in} = \text{logic } 0, V_{\rm out} = \text{logic } 1$) or vice versa. The logic state of the flip-flop is fully characterized by the number of electrons on the two load capacitors $C_1$ and $C_2$. The presence of thermal noise induces variations of the electron populations that cause the flip-flop to stray from the stable operating points. Large fluctuations of the number of electrons are exponentially rare. However, if a fluctuation is large enough, the flip-flop input and output voltages pass a critical threshold that results in the system being driven spontaneously to the other stable configuration, resulting in a logic error.

An example is shown in Fig. 3, where the Monte Carlo simulation for a model system with 25 electrons is presented. The model flip-flop was operated at $V_{\rm dd} = 0.2$ V and at a temperature of 100 °C. It can be seen that the electron populations on the two inverters present thermally induced fluctuations that do not change the logic level except in the rare case of a very

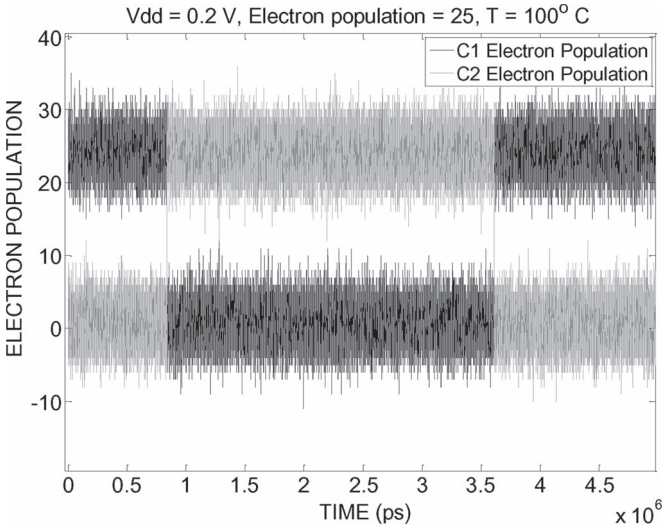


Fig. 3. Monte Carlo simulations for a model system with a low number of electrons (introduced in [13]). For large fluctuations in electron population beyond the midpoint, the system is driven spontaneously to the other stable state.

large fluctuation that drives the flip-flop to the other stable configuration. As explained later in this paper, an appropriate time scale for the Monte Carlo simulation of electrons leaving and arriving at node capacitances is a picosecond. For the small model system shown in Fig. 3, such very large fluctuations occur roughly every $\approx 10^6$ ps. For systems of real interest with a larger number of electrons, Monte Carlo simulations cannot observe such large fluctuations because the number of time intervals that must be considered exceeds the capability of commonly available computational resources.

In [12], an older bulk 65-nm CMOS technology from Intel [17] was used to model the effects of ultralow supply voltage on the subthreshold noise characteristics of a CMOS inverter operated at $V_{\rm dd} = 0.2$ V. The drain current $I_{\rm D}$, in the subthreshold regime, can be described by the diffusion dominated expression, including the drain-induced barrier lowering (DIBL) threshold shift

$$I_{\rm D} = i_0 \frac{W}{L_{\rm G}} \left(\frac{kT}{q}\right)^2 \exp\frac{q(V_{\rm GS}-V_{\rm T}+\sigma V_{\rm DS})}{nkT} \left(1 - e^{-\frac{qV_{\rm DS}}{kT}}\right) \quad (1)$$

where $W$ is the channel width, $L_{\rm G}$ is the channel length, $i_0$ is a prefactor that depends on channel mobility, $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the elementary charge, $n$ is the subthreshold slope factor, $\sigma$ the DIBL parameter, $V_{\rm T}$ is the transistor threshold voltage, $V_{\rm GS}$ is the gate voltage, and $V_{\rm DS}$ is the drain voltage.

Due to the coupling of the inverters, the charging and discharging rates for a particular inverter will depend on the electron populations on both capacitors $C_1$ and $C_2$, denoted $k_1$ and $k_2$, as shown in Fig. 2. It can be seen that $V_{\rm GS}$ and $V_{\rm DS}$ voltages for each of the four transistors can be rewritten as a function of $k_1$, $k_2$. The number of electrons stored in one node capacitance, when the bias voltage equals $V_{\rm dd}$, is denoted by $m$. The charging rates are denoted by $\lambda^{p_i}_{k_1k_2}$ or $\lambda^{n_i}_{k_1k_2}$, where $i$ refers to one of the two inverters and $p$ and $n$ denote the NMOS and PMOS transistors, respectively, that make up the inverter. Similarly, the notation for the discharging rates is $\mu^{p_i}_{k_1k_2}$ and $\mu^{n_i}_{k_1k_2}$.

Defining $u_{\rm T} = q \cdot V_{\rm dd}/k \cdot T$ to be the ratio of logic energy to thermal energy, the rates for the PMOS device in the first inverter are given, for example, by

$$\lambda^{p_1}_{k_2} = I_0 \cdot e^{\frac{u_t}{n}\frac{m-k_2}{m}} \quad (2)$$

$$\mu^{p_1}_{k_1k_2} = I_0 \cdot e^{\frac{u_t}{n}\frac{m-k_2}{m}} e^{\frac{-u_t}{n}\frac{m-k_1}{m}} \quad (3)$$

where $I_0$ accounts for the channel mobility prefactor $i_0$, width over channel length ratio, and $(kt/q)^2$.

Expressing the transition rates as a function of electron populations on the two node capacitances, Monte Carlo simulation can be used to investigate mean time to failure of model flip-flops.

### A. Monte Carlo Simulations

The flip-flop CMOS transistors are represented as two Poisson sources to portray the charging and discharging currents. One source is the reverse current and the other is the forward current. The fundamental assumption underlying a Poisson process is that events are rare and that the probability of an event in an interval $dt$ is given by $\lambda dt$, where $\lambda$ is a rate constant.

In the model for our flip-flop, such possible events are the departure or arrival of electrons at node capacitances. In order to meet the requirement that these events are rare, the time interval $dt$ must be appropriately sized [13]. Both for the 65-nm transistors [17] and for the SOI transistors [18] considered in this paper, the charging and discharging currents range from nanoamperes to microamperes, depending on $k_1$ and $k_2$. Accounting for the electron charge, it is imperative to set the time interval to picoseconds (ps) or less in order to have a low probability for an arrival or departure to occur during $dt$. Such a small time sampling, from the start, sets a limit on the total time over which the thermal fluctuation in electron populations can be evaluated.

Using the Monte Carlo simulation, the system is free to be in any of the available states. The simulations have been performed for a flip-flop model built with 65-nm transistors [17] and operated at a fixed subthreshold voltage $V_{\rm dd} = 0.2$ V. The number of electrons $m$, stored in one node capacitance when the bias voltage equals $V_{\rm dd}$, was the variable parameter. The mean time to failure was found to scale exponentially with $m$. The flip-flop with the largest electron population for which a failure could be observed by Monte Carlo, had only 30 electrons. For smaller dimensions, a sufficient number of simulations (i.e., 10 000) were performed to calculate a reliable mean failure time for a flip-flop with up to 23 electrons.

For flip-flop circuits of real interest with a larger number of electrons, it is clear that Monte Carlo simulations cannot be run long enough to observe a logic failure. Even assuming a short mean time to fail due to thermal noise on the order of a few days, this would translate to $\approx 10^{17}$ ps. The Monte Carlo simulation would have to go through the same number of iterations to observe, on average, one logic error. Considering

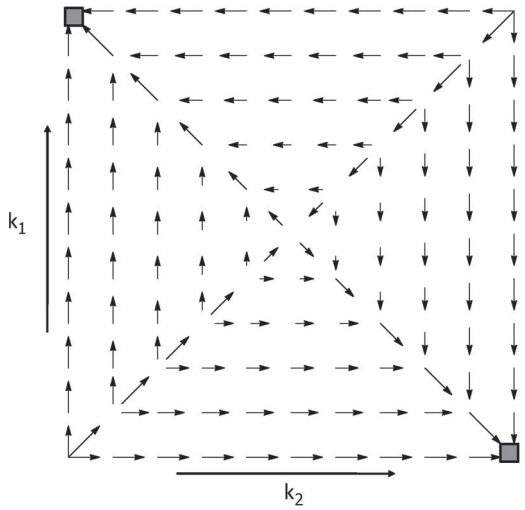


Fig. 4. For any given state in the 2-D queue, the rates of transition to neighboring states can be calculated. Plotting for each state, the transition associated with the highest rate results in a flow graph with the most probable paths in the 2-D queue.

that one iteration requires about ten floating point operations, this means that about $10^{18}$ floating point operations would be needed to be evaluated for a flip-flop that fails within days.

The failure of Monte Carlo simulations to resolve flip-flops with error rates that would present a reliability concern, highlights the importance of an analytic method that can calculate the failure rates of flip-flops built in different device technologies.

Although inappropriate for ultimately solving systems of real interest, the results of Monte Carlo simulations are important in assessing one important assumption that the theoretical framework proposed in this paper is based upon: That within the rectangular 2-D queue representation of the system, transitions can be restricted to be only along the diagonal path. A valid estimate of the failure time can be obtained by considering transitions along the 1-D queue. The comparison between 1-D failure times and Monte Carlo results will be presented in the following section.

### *B. 2-D Queue Representation of the Flip-Flop Circuit*

As previously mentioned, the possible configurations for the flip-flop in terms of the electron populations $k_1$, $k_2$ on the two load capacitors $C_1$, $C_2$ can be represented as a rectangular 2-D queue, as shown in Fig. 1.

A given state from the 2-D queue can be denoted as $(k_1, k_2)$ and is surrounded by four states denoted by $(k_1 \pm 1, k_2)$ and $(k_1, k_2 \pm 1)$. Each state is fully characterized by the electron populations and the transitions rates to each of the neighboring states can be computed. Representing the largest transition rate with a vector and accounting for its varying magnitude for different states, results in a flow chart of the most probable paths that the system can follow in the 2-D queue, which is shown in Fig. 4.

The two logically stable states are indicated by two rectangles in opposite corners of the graph. As expected, Fig. 4 shows that there is an unstable equilibrium point for $k_1 = m/2$, $k_2 = m/2$, where $m$ is the size of the 2-D queue. For a state on the main diagonal $k_i + k_j = m$ the most probable path is along the main diagonal in the direction of increasing $k_{\max}$. For a state on the second diagonal $k_i = k_j$, the most probable path is along the second diagonal toward the unstable midpoint. For a given state $(k_i, k_j)$ with $i \neq j$ and $(k_i > k_j)$, the most probable path results in increasing $k_i$ or decreasing $k_j$ depending on the position of state in the 2-D queue.

The probability offset map can be built using the difference in the transition rates along the most probable paths and taking the cumulative offset when moving from one state to another. The probability offset map has a saddle configuration with two stable states, for logic 1 and 0, and a saddle point for the middle of the queue. Fig. 5 shows the probability offset map for a 250-electron flip-flop. It is obvious from this map that the most probable path for transition between the two stable states is a diagonal one and that large deviations from the main diagonal between the stable states are unlikely.

## III. 1-D Queue Model

As argued in the preceeding section and shown in Fig. 5, the original 2-D queue representing the available states for the flip-flop can be reduced to a 1-D birth–death queue along the main diagonal. The states $(k_1, k_2)$ contained in the main step diagonal are given by $k_1 + k_2 = m$ and $k_1 + k_2 = m + 1$. Transitions between neighboring states are driven by two types of Poisson processes: the charging and discharging of the two load capacitors. The time interval $dt$ is chosen to be small enough to insure that the probability of jumping two or more states along the 1-D queue can be ignored. If $k_1 + k_2 = m$, from $(k_1, k_2)$, the system can move only to $(k_1 + 1, k_2)$ or $(k_1, k_2 + 1)$. If $k_1 + k_2 = m + 1$, from $(k_1, k_2)$, the system can move only to $(k_1 - 1, k_2)$ or $(k_1, k_2 - 1)$. This restricted movement is shown in Fig. 1.

Considering that $(k_1 = m, k_2 = 0)$ is the initial logic state, the rate of transition from $(k_1, k_2)$ toward $(k_1, k_2 + 1)$ or $(k_1 - 1, k_2)$ represents the charging rate, and it is denoted by $\lambda_i$, where $i$ is the index of the state in the 1-D queue. Similarly, the rate of transition toward $(k_1, k_2 - 1)$ or $(k_1 + 1, k_2)$ represents the discharging rate, and it is denoted by $\mu_i$.

If at time $t = 0$ the system is known to be in state $i$, the probability that it is still in state $i$ some time later is $e^{-(\lambda_i + \mu_i)t}$. The probability density for transitions out of this state to $i + 1$ or $i - 1$ is

$$p_i(t) = (\lambda_i + \mu_i)e^{-(\lambda_i + \mu_i)t}. \tag{4}$$

The residence time for state $i$ is given by the first moment of the transition probability density

$$\tau_i = \int_0^\infty t \cdot p_i(t)dt = \frac{1}{\lambda_i + \mu_i}. \tag{5}$$

Denoting the rates connecting two states by $r_{\mathrm{iq}}$, the probability density for transitions out of state $i$ to $q$ is given by $r_{\mathrm{iq}}p_i(t)/(\lambda_i + \mu_i)$. The factor $r_{\mathrm{iq}}/(\lambda_i + \mu_i)$ is the probability that when the system leaves state $i$, it goes to state $q$.

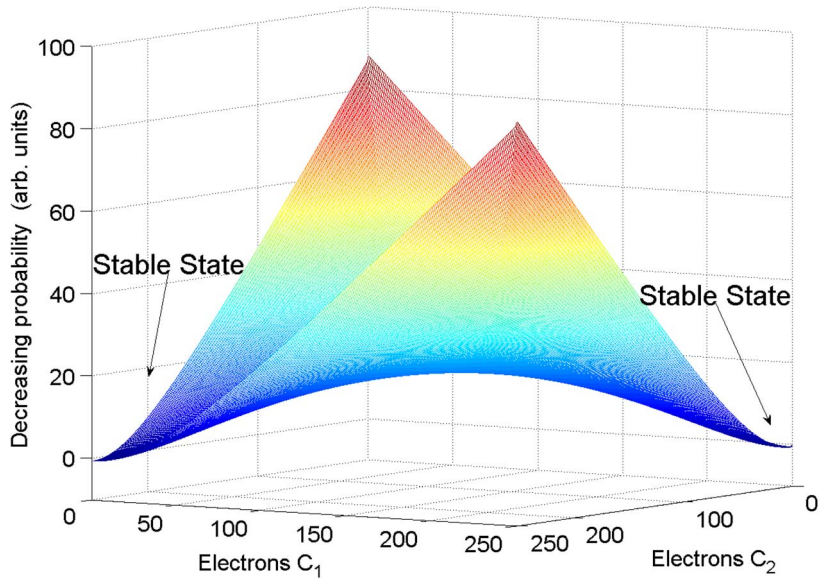


Fig. 5. Considering the most probable paths in the 2-D queue shown in Fig. 4, it is possible to plot the probability offset map for a 250-electron flip-flop built in 65-nm CMOS technology from Intel [17] and operated at subthreshold voltage $V_{\rm dd} = 0.2$ V $< V_{\rm T} = 0.28$ V. It illustrates the probability barrier that the system has to overcome to travel from one stable state to another. It is obvious that the path with the lowest probability barrier is a diagonal path. This justifies the approximation that the 2-D queue can be reduced to a diagonal 1-D queue.

Poisson process-induced transitions along the 1-D queue, can be analyzed using Laplace transforms.

### A. Linear System of Laplace Transforms

Laplace analysis can be used to calculate the moments of the probability density function in the context of queuing theory [13], [19]. Consider the special case when the queue leaves state $i$ and enters state $k$ at time $t_k$. The probability density for the time of reaching state $q$ via state $k$ is given by

$$p_{i\to k\to q}(t) = \frac{r_{ik}}{\lambda_i + \mu_i} \int_0^t p_i(t_k) p_{kq}(t - t_k) dt_k. \tag{6}$$

The Laplace transform of such a convolution is a simple product

$$L\left(p_{i\to k\to q}(t)\right) = \frac{r_{ik}}{\lambda_i + \mu_i} L\left(p_i(t)\right) L\left(p_{kq}(t)\right). \tag{7}$$

Considering the expression for $p_i$, (4) yields

$$L\left(p_i(t)\right) = \int_0^\infty p_i(t) e^{-st} dt = \frac{\lambda_i + \mu_i}{s + \lambda_i + \mu_i}. \tag{8}$$

From an initial state $i$, the system may have to move through a number of intermediate states to reach state $q$. Therefore, the probability density to reach $q$ must be the sum of all possible densities through the different intermediate states $k$

$$L\left(p_{i,q}(t)\right) = \sum_{k\neq q} \frac{r_{i,k}}{s + \lambda_i + \mu_i} L\left(p_{k,q}(t)\right) + \frac{r_{i,q}}{s + \lambda_i + \mu_i}. \tag{9}$$

Considering that in the model used, only transitions between consecutive states are allowed, $r_{i,k}$ can be written as

$$r_{i,k} = \begin{cases} \lambda_i & \text{if } k = i + 1 \\ \mu_i & \text{if } k = i - 1 \\ 0 & \text{if } |k - i| > 1. \end{cases} \tag{10}$$

Because $r_{i,k} \neq 0$ only for neighboring states, the Laplace transform for transition between the intermediate states in the 1-D queue, and the final state $f$ can be written as

$$L\left(p_{i,f}(t)\right) = \frac{\lambda i \cdot L\left(p_{i+1,f}(t)\right)}{s + \lambda_i + \mu_i} + \frac{\mu_i \cdot L\left(p_{i-1,f}(t)\right)}{s + \lambda_i + \mu_i}. \tag{11}$$

The probability density function $p_{i,f}(t)$ requires solving for the Laplace transform associated with the transition between the initial and final states. The Laplace transform is used to calculate the moments of the probability density function. The $n$th order moment is given by

$$M_n = lim_{s\to 0} \frac{d^n}{ds^n} L_{i,f}(-s). \tag{12}$$

For a 2-D queue of dimension $m$, the number of states in the 1-D queue is $2m$. The Laplace transform linear system of equations for the 1-D queue, due to memory limitations on commonly available computational resources, can only be solved explicitly in Mathematica [20] for up to a 70-state 1-D queue representing a 35-electron system. Once the Laplace transform is known, the probability density function can be calculated by taking the inverse Laplace transform. The probability density function is used to calculate the mean time and the variance of the process. The results for the 1-D queue obtained by explicitly computing the probability density function are in good agreement with the Monte Carlo results for the full 2-D queue,

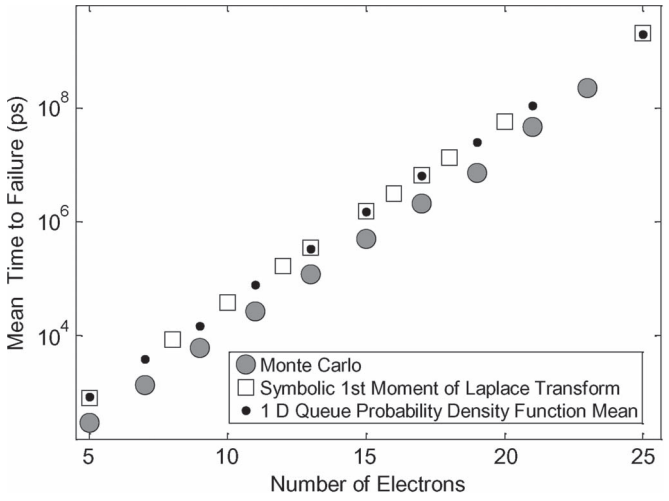


Fig. 6. For the model system with low number of electrons introduced in [13], the mean time was calculated using Monte Carlo simulations. Using the 1-D queue approximation, the system of Laplace transforms was explicitly solved in Mathematica, and the mean time to failure was computed from the probability density function. These results indicate that the full queue can be approximated by a 1-D diagonal queue and obtain reliable estimates of the error times. Using the symbolic expressions for moments of the probability density function that describes the 1-D queue, numerical results are obtained that agree with results calculated by exactly solving the system of Laplace transforms.

as shown in Fig. 6. As a result, the 1-D approximation becomes a viable strategy to deal with larger systems.

### *B. Symbolic Pattern of Laplace Transform Coefficients*

For the 2-D queues that represent flip-flops built in a realistic technology [17], [18] that have around 250 electrons at subthreshold voltages, it is impossible to solve explicitly the system of Laplace transforms. The theoretical framework proposed in this paper aims to calculate the coefficients of the Laplace transform directly by identifying the functional pattern of dependence on the transition rates. As presented later in this paper, the coefficients can be used to calculate the moments of the probability distribution function. While it is possible to calculate all the coefficients of the Laplace transform, only the first few coefficients are needed to describe the relevant quantities such as the average time and cumulative probability of failure. The structure and relevance of the first four coefficients are detailed in this paper.

The Laplace transform can be written in the most general form as

$$L_{i,j}(s) = \frac{1}{1 + f_1 s + f_2 s^2 + f_3 s^3 + \cdots + f_m s^m}. \quad (13)$$

Using (12), the expressions for the first four moments of the probability density function, as a function of Laplace transform coefficients $f_i$, are given by

$$\begin{aligned} M_1 &= f_1 \\ M_2 &= 2f_1^2 - 2f_2 \\ M_3 &= 6f_1^3 - 12 f_1 f_2 + 6 f_3 \\ M_4 &= 24 f_1^4 - 72 f_1^2 f_2 + 24 f_2^2 + 48 f_1 f_3 - 24 f_4. \end{aligned} \quad (14)$$

The first moment $M_1$ represents the mean time of transition between the first and last state of the queue. Moments about the origin of order two through four, are related to the variance, skewness, and kurtosis of the probability density function via the corresponding moments about the mean, denoted here by $\Upsilon_i$ [21], [22]

$$\begin{aligned} \Upsilon_2 &= M_2 - M_1^2 \\ \Upsilon_3 &= M_3 - 3M_1 M_2 + 2M_1^3 \\ \Upsilon_4 &= M_4 - 4M_1 M_3 + 6M_1^2 M_2 - 3M_1^4. \end{aligned} \quad (15)$$

The second moment about the mean $\Upsilon_2$ represents the variance. The skewness is given by $\Upsilon_3/\Upsilon_2^{3/2}$ while the kurtosis is given by $\Upsilon_4/\Upsilon_2^2$. It can be seen from (14) and (15) that the mean, variance, skewness, and kurtosis can be related to the first four coefficients of the Laplace transform [21], [22]

$$\text{Variance} = f_1^2 - 2f_2 \quad (16)$$

$$\text{Skewness} = \frac{2f_1^3 - 6f_1 f_2 + 6f_3}{\left(f_1^2 - 2f_2\right)^{3/2}} \quad (17)$$

$$\text{Kurtosis} = \frac{9f_1^4 - 36 f_1^2 f_2 + 24 f_2^2 + 24 f_1 f_3 - 24 f_4}{\left(f_1^2 - 2f_2\right)^2}. \quad (18)$$

The coefficients $f_i$ are functions of the charging and discharging rates for the states along the 1-D path, $\lambda_i$ and $\mu_i$. For queues with a small number of electrons $m$ and states 0 to $n = 2m - 1$, it is possible to solve explicitly for the Laplace transform and analyze its formula. The first coefficient has been determined to be a linear combination of terms with the following structure:

$$\begin{aligned} f_1 = &\frac{1}{\lambda_0} + \frac{1}{\lambda_1} + \frac{1}{\lambda_2} + \frac{1}{\lambda_3} + \ldots + \frac{\mu_1}{\lambda_0 \lambda_1} + \frac{\mu_2}{\lambda_1 \lambda_2} + \frac{\mu_3}{\lambda_2 \lambda_3} \\ &+ \ldots + \ldots + \frac{\mu_1 \ldots \mu_{n-1}}{\lambda_0 \ldots \lambda_{n-1}} + \frac{\mu_2 \ldots \mu_n}{\lambda_1 \ldots \lambda_n} + \frac{\mu_1 \mu_2 \ldots \mu_n}{\lambda_0 \lambda_1 \ldots \lambda_n}. \end{aligned} \quad (19)$$

All the terms that appear in the sum have consecutive indices for $\mu_i$ and $\lambda_i$. The set given by

$$\left\{ \frac{\mu_i, \ldots, \mu_{i+j}}{\lambda_{i-1}\lambda_i, \ldots, \lambda_{i+j}}, j = 0, n-1; i = 1, n; i + j \le n \right\} \quad (20)$$

is the base set from which all coefficients $f_i$ can be constructed. The first coefficient $f_1$ can be expressed in a closed form as

$$f_1 = \sum_{k=0}^{n} \sum_{i=1}^{n-k+1} \frac{1}{\lambda_{i-1}} \prod_{j=i}^{i+k-1} \frac{\mu_j}{\lambda_j}. \quad (21)$$

In (21), $i - 1$ gives the lowest order factor $1/\lambda_{i-1}$ that appears in a given term. The index $k$ gives the number of $\mu_j/\lambda_j$ factors that are multiplied to generate the current term. The values for $k$ range from 0, giving $1/\lambda_i$, to $n$, giving $\mu_1, \ldots, \mu_n/(\lambda_0 \lambda_1, \ldots, \lambda_n)$.

For a 1-D queue with states from 0 to $n$, the total number of terms in the base set that need to be added to calculate the $f_1$ coefficient is $(n + 1) \cdot (n + 2)/2$. For a 250-electron flip-flop, the 1-D queue contains 500 states which means that less than

$10^6$ terms must be evaluated. Significantly, larger systems can also be evaluated within the proposed framework.

For the 1-D queue, the magnitude of the terms in the base set can differ by orders of magnitude depending on the indices $i$: $\mu_i > \lambda_i$ for $i < n/2$ and $\mu_i < \lambda_i$ for $i > n/2$. Therefore, the ratio $\mu_i/\lambda_i$ can be larger or smaller than one depending on $i$. For an $n$-state 1-D queue, the maximum and minimum terms in the base set have the following structure:

$$\text{maximum term} = \frac{\mu_1 \ldots \mu_{n/2}}{\lambda_0 \lambda_1 \ldots \lambda_{n/2}} \tag{22}$$

$$\text{minimum term} = \frac{\mu_{n/2} \cdots \mu_n}{\lambda_{(n/2)-1} \lambda_{n/2} \ldots \lambda_n}. \tag{23}$$

For a 500-state 1-D queue describing the FD-SOI flip-flop, the unit $\mu_i/\lambda_i$ ratio, has a typical value of 1.1 or 0.9 depending on $i$. Using (22) and (23), the minimum term can be estimated to be $0.9^{250} \approx 10^{-12}$ and the largest term to be $1.1^{250} \approx 10^{10}$.

The vast difference in magnitude between the largest and smallest terms outlines the difficulty in solving the given 2-D queue using the eigenvector method [15], [19]. The transition and generating matrices are too ill conditioned to be numerically tractable. Within the proposed theoretical framework, such numerical difficulty is bypassed and the only concern is the round-off error which can be controlled by ordering the set first and starting to add up from the smallest terms.

The validity of the assumption that the system can be considered to mostly move along the diagonal path of the 2-D queue is shown in Fig. 6. The mean time results given by the Monte Carlo simulations are in good agreement with the ones obtained by explicitly solving the linear system of Laplace transforms and retrieving the mean time to failure. The validity of the symbolic solution for the moments of the Laplace transform is demonstrated by the perfect agreement between the symbolic predictions and the exact Mathematica results.

The difference between the mean failure time obtained for the 1-D diagonal queue and the mean time given by Monte Carlo simulations stems from the assumptions that the approximation is based upon: only diagonal states are considered, and only transitions between consecutive states are allowed. Possible trajectories that include transitions along the main diagonal between states that are not consecutive have a lower passage time, but they are not considered in the 1-D approximation.

### C. Higher Order Coefficients

It is of interest to know not only the mean time to failure but also the probability that the flip-flop will fail within a given time. This requires the calculation of the probability density function by taking the inverse of the Laplace transform that has higher order coefficients in its formula, as shown in (13). Ideally, all the coefficients of the Laplace transform should be taken into account. For the 1-D queue that is the subject of this analysis, it was found that considering coefficients of order higher than four does not result in a significant difference. However, the general structure of a coefficient of arbitrary order is presented.

The structure of the $f_2$ coefficient contains terms that can be rewritten as pairwise products of the factors that appear in $f_1$, with the restriction that no index $i$ can appear twice; e.g., terms like

$$\frac{1}{\lambda_0 \lambda_4} = \frac{1}{\lambda_0} \cdot \frac{1}{\lambda_4} \tag{24}$$

$$\frac{\mu_1 \mu_2 \mu_6 \mu_7}{\lambda_0 \lambda_1 \lambda_2 \lambda_5 \lambda_6 \lambda_7} = \frac{\mu_1 \mu_2}{\lambda_0 \lambda_1 \lambda_2} \cdot \frac{\mu_6 \mu_7}{\lambda_5 \lambda_6 \lambda_7}. \tag{25}$$

The second coefficient $f_2$ can be written in a closed form using the expression for $f_1$

$$f_2 = \sum_{k=0}^{n-1} \sum_{i=1}^{n-k+1} \frac{1}{\lambda_{i-1}} \prod_{j=i}^{i+k-1} \frac{\mu_j}{\lambda_j} \cdot \sum_{y=0}^{n-(i+k)} \sum_{x=i+k+1}^{n-y+1} \frac{1}{\lambda_{x-1}} \prod_{z=x}^{x+y-1} \frac{\mu_z}{\lambda_z}. \tag{26}$$

The index $k$ gives the number of $\mu_j/\lambda_j$ factors that are multiplied to generate the first term in the pairwise product that is present in the sum. In this case, the values for $k$ range from zero to $n-1$ restricting the term $\mu_1, \ldots, \mu_n/(\lambda_0 \lambda_1, \ldots, \lambda_n)$ that cannot be paired with any other term from the base set because of overlapping indices.

The higher order coefficients have been found to follow the same pattern. A coefficient of order $p$ can be calculated by taking the sum of all possible products of $p$ terms from the base set with the restriction that no indices appear twice. For example, a term appearing in $f_3$ can be rewritten as

$$\frac{\mu_1 \mu_3 \mu_4}{\lambda_0 \lambda_1 \lambda_2 \lambda_3 \lambda_4 \lambda_7} = \frac{\mu_1}{\lambda_0 \lambda_1} \cdot \frac{\mu_3 \mu_4}{\lambda_2 \lambda_3 \lambda_4} \cdot \frac{1}{\lambda_7}. \tag{27}$$

Closed formulas for $f_3$, $f_4$ and higher coefficients can be extrapolated from (26) along the guidelines presented above.

Using (17) and (18), for all the flip-flops considered in this paper, the skewness was calculated to be two and the kurtosis to be nine. The distribution function with these parameters is the exponential distribution which describes the times between events in a Poisson process [21], [22].

## IV. SOI Technology Flip-Flop

In order to apply our modeling to a real-world technology, we have chosen a recently published FD SOI transistor technology available at the 32-nm node [18]. The transistor has an effective gate length of $L_G = 25$ nm. The buried oxide (BOX) thickness is 146 nm, and the SOI layer is 10 nm thick. The equivalent gate oxide thickness is taken to be 1 nm. The gate material (TiN) work function is assumed to be roughly mid-gap for Si and undoped channels were used in the fabrication of the transistors.

The first step in the analysis is to simulate these FD-SOI transistors (drain current, inversion and parasitic charges, temperature, and threshold variations) particularly in the subthreshold regime.

The current–voltage characteristics of the transistors built in this FD SOI technology, cannot be modeled with the subthreshold $I_D$ expression from (1) used so far, which is valid only for

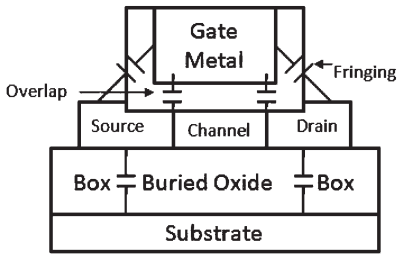


Fig. 7. Schematic of an FD-SOI MOSFET with the most important parasitic capacitances taken into account in the simulations: overlap, fringing, and BOX capacitances.

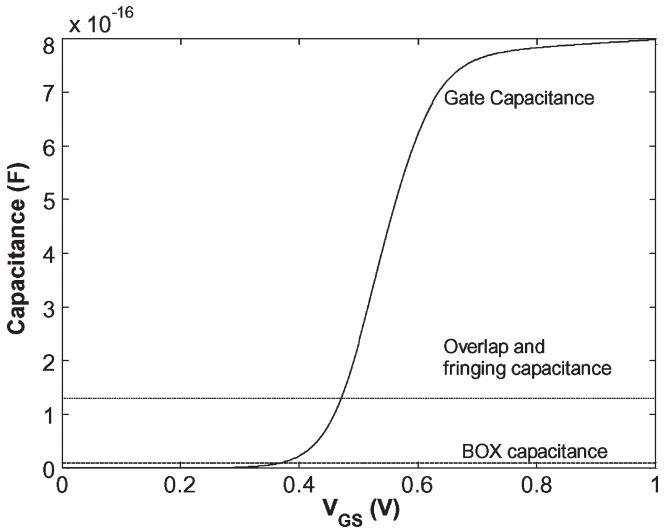


Fig. 8. Overlap, fringing, and BOX capacitances for an NMOS transistor.

bulk devices [12], [13]. Instead a model [23] has been used that is valid and analytic from weak to strong inversion and effects such as the DIBL, mobility reduction and velocity saturation are taken into account. The inversion charge at the drain and source sides of the channel are computed and from those, both the total inversion charge and the drain current can be found.

Unlike our earlier models [12] of idealized flip-flops, we have included parasitics of the SOI flip-flop in our analysis. Parasitic charges become very important in low-voltage operation of the transistors, where the inversion charge is significantly less than in strong inversion, and the gate capacitance is comparable to parasitic ones. Fig. 7 shows a schematic of an FD-SOI transistor with the parasitic capacitances taken into account, namely, the overlap, fringing, and BOX capacitances. As this is an ultra-thin FD-SOI technology, junction capacitances are negligible. The various capacitances of an NMOS device are shown in Figs. 7 and 8.

For our simulations, we consider the 32-nm FD-SOI, $L_{\rm G} =$ 25 nm transistors to be operated in subthreshold regime, and the total charge is found by integrating the total capacitance $Q = \int C(V)dV$, where capacitance $C$ is a function of voltage. Operating at $V_{\rm dd}$ values of 0.2–0.3 V results in 200–300 electrons being stored in a node capacitance.

All the technology and model parameters that were not given in [18], were extracted by fitting the published data with the model, as shown in Fig. 9. After the extraction of the full parameter set, the model can be used to simulate a similar

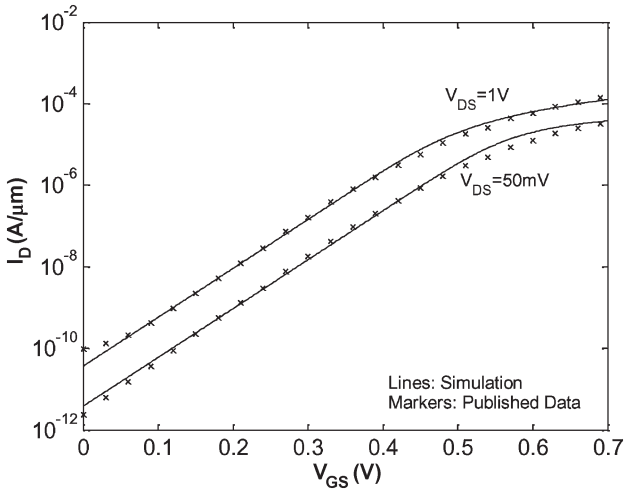


Fig. 9. $I_{\rm D}-V_{\rm GS}$ characteristics for an SOI NMOS transistor. Simulation and published data [18]. The model used for simulations [23] is valid and analytic from weak to strong inversion and effects such as the DIBL, mobility reduction, and velocity saturation are taken into account.

transistor of any width at any drain/gate voltages and any temperature. In addition, in order to investigate the effect of the mismatch between NMOS and PMOS devices on the noise of a flip-flop, an arbitrary threshold shift due to process variations can be added to any transistor.

### A. Mean Time to Failure

The theoretical results outlined above were used to calculate the mean error time for flip-flops built with transistors with no threshold variation. Operated at room temperature at a subthreshold voltage $V_{\rm dd} = 0.2$ V with an electron population of ≈200, the mean time to failure was found to be greater than $10^{40}$ s. However, this apparent stability arises from assuming perfectly matched current drive of the NMOS and PMOS transistors in the CMOS inverter. In a realistic CMOS inverter, this is not the case and a mismatch in current drive is usually present due to process variations.

The rapid scaling of CMOS technology inevitably leads to increased process variations [1]. These variations manifest themselves as fluctuations in the transistor parameters, such as $L_{\rm G}$, $V_{\rm T}$ and parasitic source/drain resistance. The effect of transistor threshold voltage shift $\delta V_{\rm T}$ is particularly critical, as it affects the current drive exponentially, with $I_{\rm D} \approx \exp(-\delta V_{\rm T})$. If the threshold values of NMOS and PMOS devices in an inverter are shifted in opposite directions by the same $\delta V_{\rm T}$, the asymmetrical charging and discharging rates shift the gate threshold and lower one of the input margins. When threshold shifts are of opposite sign in the two inverters, they produce a worst case scenario in which one state of the flip-flop is less stable and subject more to thermal upset.

Considering a 15% threshold shift, the mean time to failure was calculated for flip-flops operated both at room temperature and 100 °C, as shown in Figs. 10 and 11, respectively. As shown in the figures, both the operating temperature and $V_{\rm dd}$ influence the number of electrons on the node capacitance. For a given $V_{\rm dd}$, the number of electrons stored in a node capacitance increases with temperature. At higher temperatures,

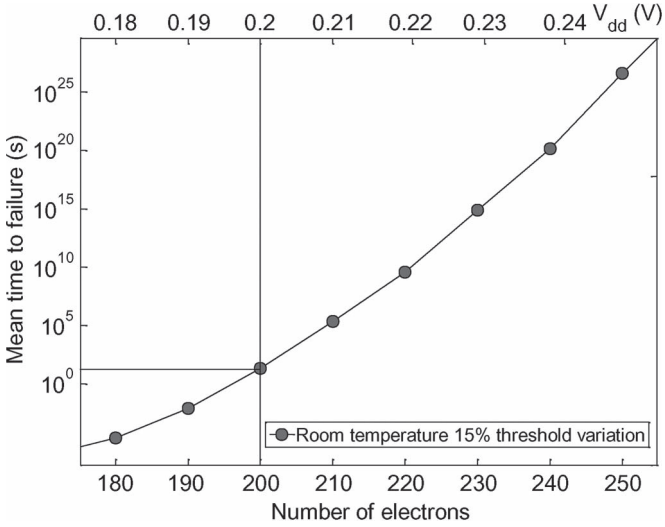


Fig. 10. Mean time to failure for the worst case scenario when threshold shifts of 15% are of opposite sign in the two inverters operated at room temperature.

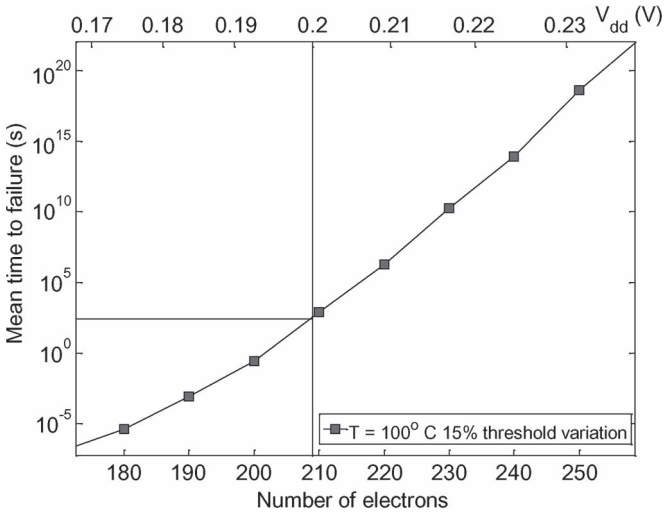


Fig. 11. Mean time to failure for the worst case scenario when threshold shifts of 15% are of opposite sign in the two inverters operated at 100 °C.

greater thermal noise and larger number of electrons have an opposite effect on the failure rate. While increased thermal noise results in larger oscillations in electron populations (as shown in Fig. 3), a larger number of electrons stored in a node capacitance requires the flip-flop to stray to a greater extent from the stable operating points in order for a logic error to occur. At both temperatures, considering an operating voltage $V_{\rm dd} = 0.2$ V, it is shown in Figs. 10 and 11 that the mean failure time for a device is less than $10^4$ s.

The mean time to failure increases exponentially with the operating voltage $V_{\rm dd}$. However, even at higher operating voltages, the reliability still remains a concern if we consider the large number of devices in integrated circuits. For a 240-electron flip-flop with 15% threshold variation at 100 °C and $V_{\rm dd} = 0.225$ V, the cumulative distribution function is shown in Fig. 12. For a single device, the mean time to flip is $\approx 10^{14}$ s. Such a long time may seem not to pose any logic stability problems for this technology. However, considering that modern integrated circuit is approaching $10^9$ devices on

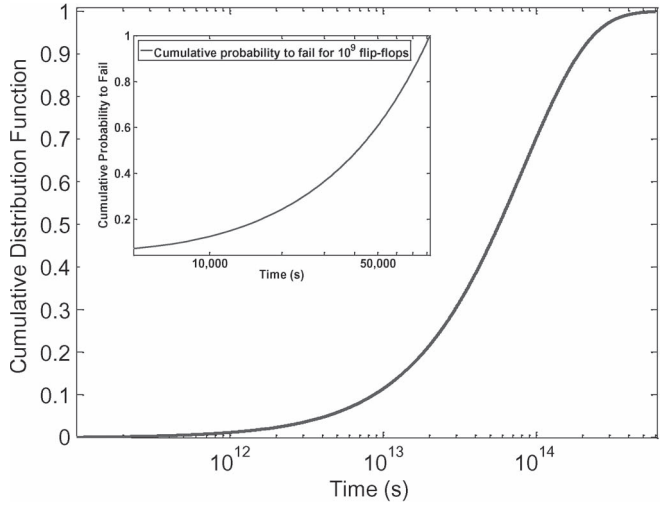


Fig. 12. Cumulative distribution function for 240-electron flip-flop at 100 °C with 15% threshold variation. Inset: cumulative distribution function for an integrated circuit with $10^9$ devices. For such an integrated circuit, the mean time for a logic error to occur is on the order of days.

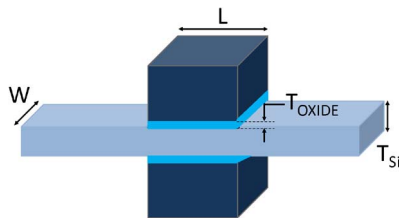


Fig. 13. Symmetrical DG FET predicted by ITRS roadmap for year 2022.

a chip, the average mean time for a logic error on the chip is $10^5$ s. The inset of Fig. 12 shows the cumulative probability for such a logic error to occur within a given time. It can be seen that such an integrated circuit with $10^9$ devices will suffer logic errors within days.

## V. Ultimate ITRS Predicted Technology

To investigate the reliability of future logic devices, a symmetrical double-gate field-effect transistor (DG FET), predicted by the ITRS for the year 2022, has been selected. The transistor is schematically shown in Fig. 13. The parameters outlined by the ITRS for this transistor are the following: physical gate length $L_{\rm G} = 6$ nm, equivalent oxide thickness 6 Å (10 Å including quantum–mechanical effects), power supply voltage 0.45 V, threshold voltage 0.2 V, Si channel thickness of 3.7 nm, and channel doping of $10^{17}$ cm$^{-3}$.

Simulations using the MASTAR software [24] predict a 20% overlap of source/drain under the gate and the total fringing capacitance for an inverter to be $1.9 \cdot 10^{-16}$ F/$\mu$m. The framework presented allows for rigorous calculation of error rates at subthreshold voltages, but we expect that it can be reasonably applied to voltages slightly above threshold. For near-threshold voltage $V_{\rm dd} = 0.25$ V, the CMOS inverter total charge including parasitics (overlap, fringing, Miller) consists of 36 electrons. In the simulations, the NMOS and PMOS devices were considered to be perfectly matched, and PMOS has half the current but double the width for identical current drive.

TABLE I
MEAN FAILURE TIME FOR AN ULTIMATE (2022) ITRS ROADMAP LOW OPERATING POWER SYMMETRICAL DG FET WITH 6-nm CHANNEL LENGTH

| T ($^o$ C) | $V_{dd}$ (V) | Charge (electrons) | Mean Time (s) |
|---|---|---|---|
| 27 | 0.25 | 36 | $4.4 \cdot 10^{10}$ |
| 100 | 0.25 | 36 | $4.7 \cdot 10^{5}$ |
| 127 | 0.25 | 36 | $1.7 \cdot 10^{4}$ |
| 177 | 0.25 | 36 | $9 \cdot 10^{1}$ |

Using the symbolic solution for the first moment of the probability density function, the mean failure time at different temperatures was calculated, as shown in Table I. It can be seen from the table that at realistic operating temperatures, such devices suffer very frequent errors. Increasing $V_{\rm dd}$ is expected to result in an exponential increase in the meantime to failure. Nevertheless, accounting for possible threshold variations and the very large number of devices in integrated circuits, our simulations suggest that such ITRS end of the roadmap devices may be susceptible to logic errors even operated at $V_{\rm dd}$ values close to the predicted supply voltage. However, the theoretical framework presented in this paper can only be used to investigate the reliability of devices operated at subthreshold voltages. For a comprehensive analysis of such future devices, a new analytic framework is needed that considers the effect of thermal and other sources of noise at voltages above threshold.

## VI. CONCLUSION

This paper presents a queuing theory analysis of thermally induced errors in subthreshold nanoscale CMOS flip-flops. It was shown that, within the full 2-D queue of available states, the flip-flop system mainly resides on the states along the main diagonal. Thus, the 2-D queue can be reduced to a 1-D queue to a good approximation. A theoretical framework has been proposed for computing the mean, variance, skewness, kurtosis, and higher moments of the probability density function that describes the transition process along a 1-D queue. The proposed framework was validated by comparing its predictions with the results obtained by exactly solving the linear system of Laplace transforms. Using these theoretical results, the reliability of two classes of devices was evaluated. While the focus was on an advanced SOI technology where device characteristics are available, the framework is also applicable in investigating the stability of future logic devices as outlined by the ITRS.

The results for FD-SOI technology show that, considering the very large number of devices in integrated circuits, thermal errors can become a concern for the worst case scenario of up to 15% threshold shifts of opposite sign in the two inverters operated at subthreshold $V_{\rm dd}$. For the presented future technology, the thermal errors, for perfectly matched NMOS and PMOS flip-flops, occur on a time scale that ranges from seconds to years, depending on the operating temperature. These results highlight the importance of the theoretical framework presented in this paper as a predictive tool to investigate the reliability of logic devices based on different technologies.

Considering the possible threshold variations and the very large number of devices in integrated circuits, the failure times for flip-flops built with ITRS predicted transistors suggest that such a new technology may suffer logic errors even at $V_{\rm dd}$ values close to the nominal operating voltage. To quantitatively investigate this scenario, the analytic framework presented in this paper is to be extended in our future work to devices operated at voltages above threshold. This would allow for complete reliability analysis of current and ITRS predicted logic devices.

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