Low-frequency noise behavior of tunneling field effect transistors

J. Wan,[1,a)] C. Le Royer,[2] A. Zaslavsky,[1,3] and S. Cristoloveanu[1]
[1]*IMEP-LAHC, INP-Grenoble, MINATEC, 3 Parvis Louis Neel, BP 257, 38016 Grenoble, France*
[2]*CEA-LETI, MINATEC, 17 Avenue des Martyrs, 38054 Grenoble Cedex 9, France*
[3]*School of Engineering, Brown University, Providence, Rhode Island 02912, USA*

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We report on the low-frequency noise (LFN) properties of tunneling field effect transistors (TFETs) fabricated on silicon-on-insulator substrate. Unlike conventional large FETs, where LFN obeys a $1/f$ frequency dependence, in large TFETs the LFN is dominated by random telegraph signal (RTS) noise characterized by $1/f^2$ slope. We explain this unique LFN behavior by the local junction control of the tunneling drain current, which involves few traps in a small area. The origin of RTS noise is corroborated by the gate length independence of the I_D-V_{GS} characteristics of TFETs. The relatively high amplitude of RTS noise in TFETs will have circuit design implications. © *2010 American Institute of Physics*. [doi:10.1063/1.3526722]

The downscaling of conventional complementary metal-oxide-semiconductor (CMOS) devices has yielded faster and cheaper circuits over the past decades. One of the impediments to further downscaling is the emergence of short-channel effects (SCEs) that increase the subthreshold slope (S) and transistor off current (I_{off}). The fully depleted (FD) and multigate MOS field effect transistors (MOSFETs) based on silicon-on-insulator (SOI) substrates have been implemented to enhance gate controllability, thus mitigating the SCEs. However, the S in standard MOSFETs cannot reach below $2.3(kT/q)$. As a result, alternative devices based on conventional semiconductor materials and processes are of interest. Among these, the tunneling field effect transistor[1] (TFET) is interesting due to its promise of low I_{off} and S, which could potentially reduce the supply voltage and hence the power consumption below the standard MOSFET limits. TFETs with $S < 60$ mV/decade at room temperature have been demonstrated experimentally, albeit with relatively low on currents (I_{on}).[2–5] Recently, most of the studies on TFETs have concentrated on enhancing the I_{on} using low-bandgap materials such as germanium (Ge),[6,7] III–V compounds,[8] carbon nanotubes,[9] and even graphene.[10,11] Other important aspects of TFETs, such as noise, have received less attention.

In this letter, we present low-frequency noise (LFN) measurements on TFETs fabricated in parallel with MOSFETs on FD SOI substrates using an advanced CMOS process. We observed random telegraph signal (RTS) noise with $1/f^2$ slope even in large TFETs. The RTS current noise in TFETs also shows amplitude as high as 5% and large device to device variability. This is different from large MOSFETs in which the $1/f$ noise is dominant. We attribute the strikingly different LFN properties of TFETs and similarly sized MOSFETs to the extremely small section of gate overlapping the narrow tunneling junction that actually controls the current in TFETs.

The LFN of standard MOSFETs is an important limiting factor in analog and digital circuits.[12,13] Since the LFN-generating mechanism is the trapping at the channel-gate dielectric interface, MOSFET LFN measurements are also used to extract the density and energy distribution of the interface traps.[14–19] As TFET technology matures, LFN properties of TFETs will also impact circuit functionality. But even at the single device level, the $1/f^2$ LFN dependence in TFETs provides a useful experimental signature distinguishing the tunneling current mechanism from standard MOSFET current.

The fabrication process flows of TFETs and FD-SOI MOSFETs are totally compatible, as illustrated in Fig. 1. The process started from a SOI substrate with 140 nm buried oxide and 20 nm active Si layer. The isolated device active areas (mesa structures) are formed by photolithography and dry etching, followed by the definition and etching of the gate stack consisting of a 6 nm SiO_2 gate oxide, a 10 nm TiN metal gate, and 50 nm of polysilicon. The first spacer is formed by the deposition of 10 nm Si_3N_4. The lightly doped drain (LDD) is formed for the MOSFETs and TFETs in different ways by altering the lithographic mask. For N-type LDD implantation, the window is opened on both the source and drain sides of NMOSFETs and only on the drain side of TFETs, and then implanted with As at 9 keV with a dose of 1×10^{15} cm^{-2}. For P-type LDD implantation, the window is opened on both the source and drain sides of PMOSFETs and only at the source side of TFETs, and implanted with BF_2 at 7 keV with a dose of 1×10^{15} cm^{-2}. Then, a second spacer of 15 or 30 nm and a Si layer of 20 nm were deposited

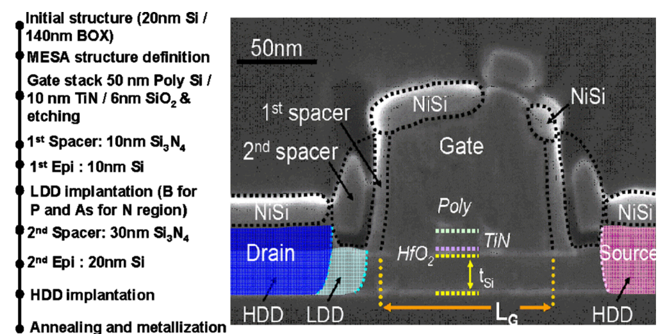

FIG. 1. (Color online) Fabrication process flow and SEM cross-section of the FD-SOI TFETs. The fabrication follows the standard MOSFET process with double spacers to lower the parasitic capacitance and raised source/drain to reduce the series resistance.

[a)]Author to whom correspondence should be addressed. Electronic mail: wanj@minatec.inpg.fr.

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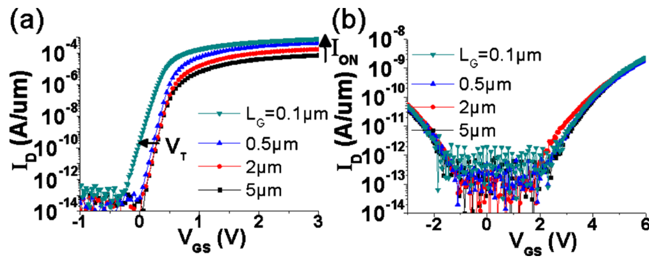

FIG. 2. (Color online) Measured I_D-V_{GS} characteristics ($V_{DS}=1$ V) of (a) MOSFETs and (b) TFETs with L_G decreasing from 5 μm to 100 nm. The I_{on} of MOSFETs tends to increase as L_G decreases and V_T decreases due to short-channel effects. The I_D of TFETs remains stable even when L_G decreases to 100 nm.

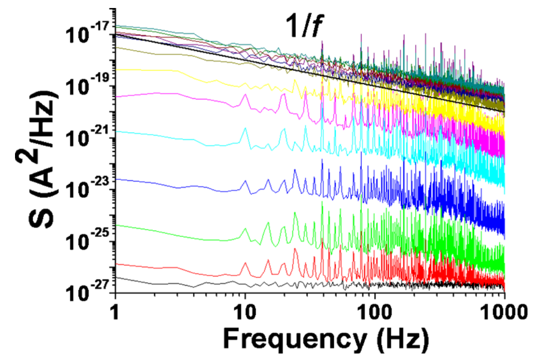

FIG. 3. (Color online) LFN spectra of NMOS ($L_G=350$ nm, $W=10$ μm, $V_{DS}=50$ mV, and $V_{GS}=0.1-1.5$ V).

(raised source and drain for reduced series resistance). The heavily doped drain (HDD) implantation followed the same process as LDD except that the As dose and energy for NHDD implantation were 2×10^{15} cm^{-2} and 20 keV, respectively, whereas for BF_2 PHDD implantation these values were 3×10^{15} cm^{-2} and 5 keV. Rapid thermal annealing was used to activate the dopants, followed by the back-end process.

The structure of our TFETs is analogous to that of a MOSFET with double spacers and raised source/drain regions, as shown in Fig. 1, with the only structural difference lying in the opposite doping of the TFET source and drain.

Figure 2 compares the I_D-V_{GS} characteristics of NMOSFETs and NTFETs with different gate lengths (L_G) from 5 μm to 100 nm. The I_{on} of TFETs is almost 5–6 decades lower than that of MOSFETs due to the large bandgap of silicon and the insufficiently abrupt tunnel junction. As can be seen from Fig. 2(a), in MOSFETs the I_{on} increases as L_G decreases due to larger channel conductance. As L_G decreases to 100 nm, the threshold voltage (V_T) of the NMOSFET tends to decrease due to the drain induced barrier lowering (DIBL). In TFETs, neither the I_{on} nor V_T changes as L_G decreases from 5 μm to 100 nm. This indicates that the current in TFETs is not controlled by channel conductance as in MOSFETs, but by interband tunneling at the source-channel junction, which is also confirmed by the weak temperature dependence of I_D.[20] Therefore, the characteristics of TFETs are independent of L_G,[21] at least for the low I_{on} levels demonstrated thus far.

In MOSFETs, the LFN is mainly caused by the fluctuation of the channel carrier density due to the trapping-detrapping process at the channel-dielectric interface. A single trapping-detrapping event causes RTS noise with Lorentzian spectrum characterized by $1/f^2$ slope.[14,16] For MOSFETs with large gate area, the superposition of many trapping-detrapping events produces $1/f$ noise, see Fig. 3. As the gate area of MOSFETs decreases below 1 μm^2, only one or a few near-interface oxide traps exist in the entire device, leading to RTS current noise.

Figure 4 shows the spectrum of two NTFETs with the same 6 nm SiO_2 gate oxide presenting totally different spectral behavior. In the NMOSFET of Fig. 3 with a gate area of 3.5 μm^2 ($L_G=350$ nm) the LFN is $1/f$, whereas in the NTFETs the noise spectrum is Lorentzian with $1/f^2$ slope despite the much larger 25 μm^2 gate area ($L_G=5$ μm). The lower images in Fig. 4 show the output voltage of the amplifier used for detecting the fluctuation in I_D. The sensitivity of the amplifier is 1×10^{-8} A/V which indicates that the maximum fluctuation in I_D is ~5% in the TFET of Fig. 4(a).

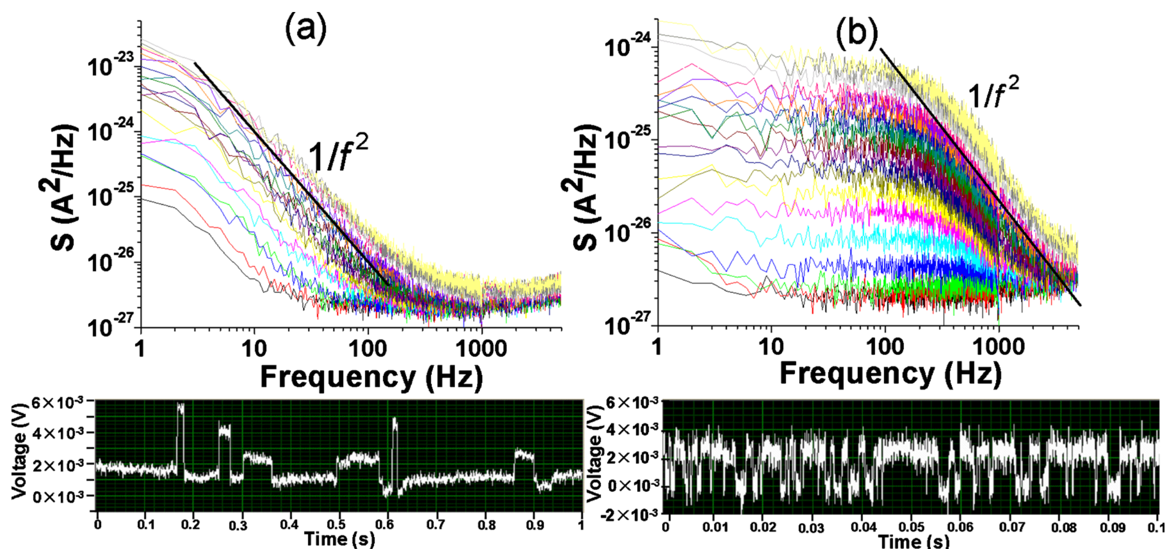

FIG. 4. (Color online) [(a) and (b)] LFN spectra of two NTFETs with the same structure and bias ($L_G=5$ μm, $W=5$ μm, $V_{DS}=1$ V, and $V_{GS}=3-5$ V). The lower images show the time variation of the output voltage from the amplifier used to capture the LFN signal in the NTFET. The RTS noise can be clearly observed with an amplitude of ~0.003 V (output voltage)$\times10^{-8}$ A/V (amplifier sensitivity)$=3\times10^{-11}$ A for the NTFET in (a). RTS of lower amplitude and higher characteristic frequency is observed in (b), indicating large variability due to single-trap events.

In TFETs, the same trapping-detrapping process occurs at the $Si-SiO_2$ interface as in MOSFETs. However, the impact of this process depends on the location of the traps. First, the trapping can modulate the channel conductance, just as in a MOSFET, but as we have discussed already, the fluctuations in the channel conductance have a negligible effect on I_D. Second, the trapping-detrapping events near the tunneling junction can change the maximum junction electric field F_{max}, causing fluctuations in the interband tunneling rate which is exponentially dependent on F_{max}.[1,2,22] The corresponding area is determined by the detailed structure and gate/drain bias of TFET, but it is generally very narrow (<10 nm).[21] Hence, the effective LFN-generating area of the TFET is very small ($<0.05\ \mu m^2$ for device width $W=5\ \mu m$), including only discrete numbers of traps, just as in a very small MOSFET. This is why the RTS noise is observed in TFETs even if the gate area is nominally large.

As in small MOSFETs,[16] the RTS noise in TFETs is characterized by a large variability. The TFET in Fig. 4(a) exhibits RTS caused by two or three traps that cause different I_D jumps at different trapping rates. The TFET in Fig. 4(b), which has nominally the same structure and dimension, includes a single RTS-generating trap with lower RTS amplitude. The trapping-detrapping process is also faster, resulting in a much higher characteristic frequency.

Due to its extremely small effective gate length (<10 nm), the amplitude of RTS noise in our TFETs is comparable to that in very small MOSFETs,[15] even though the transconductance is much lower. However, as TFET performance is enhanced by the introduction of alternative low-bandgap materials (Ge) and more effective electrostatic modulation of tunneling junction electric field, we can expect that RTS noise will become a major issue for the TFET-based circuits of the future.

In conclusion, we have measured the LFN characteristics of TFETs fabricated in parallel with FD-SOI MOSFETs on the same wafer. By comparing the I_D-V_{GS} and noise characteristics of TFETs and MOSFETs, we confirm that the current in TFETs is controlled by the tunneling junction and is independent of L_G. Our LFN measurements reveal that, unlike in MOSFETs, the RTS noise with $1/f^2$ frequency dependence and large amplitude variability is dominant in TFETs even though the nominal gate area is large because the relevant area where the interband tunneling takes place is much smaller than the physical L_G.

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