SOI TFETs: Suppression of Ambipolar Leakage and Low-Frequency Noise Behavior

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***Abstract*—We report on the thin-body tunneling field-effect transistors (TFETs) built on SOI substrates with both SiO_2 and HfO_2 gate dielectrics. The source-drain leakage current is suppressed by the introduction of intrinsic regions adjacent to the drain side, reducing the electric field at the tunnel junction. We also investigate the temperature dependence of the TFET characteristics, as well as the low frequency noise (LFN) behavior. Unlike conventional MOSFETs, the TFET LFN behaves as $1/f^2$ even for large gate areas, indicating less trapping due to its much smaller effective gate length.**

I. INTRODUCTION

As the scaling of conventional CMOS devices is suffering from short-channel effects (SCEs), silicon-compatible devices based on different principles are being studied for their unique properties. In particular, the tunneling field effect transistor (TFET) [1] is of interest due to its complete semiconductor process compatibility and similarity of device layout with the Si MOSFET. The current in TFETs is induced by band-to-band tunneling (BTBT), which makes it theoretically possible to reach extremely low OFF (I_{OFF}) currents as well as an ultra-low subthreshold slope (S) below the ideal MOSFET value of 60 mV/dec at room temperature. A number of studies have focused on power consumption in TFETs, reporting a theoretical advantage over standard MOSFETs [2-3]. In order to enhance the ON current (I_{ON}), multigate [4] and lower bandgap semiconductors, such as Ge and SiGe, have been reported [5-7].

At the same time, experimentally realized TFETs have typically suffered from difficulties in simultaneously achieving low S and high I_{ON}, as well as from high leakage current (I_{LEAK}) due to ambipolar conduction, especially for low bandgap semiconductors.

In this work, we focus on several aspects of Si TFETs. First, compare TFETs with SiO_2 and HfO_2 gate dielectrics to demonstrate lower S and higher I_{ON} values in devices with thinner equivalent oxide thickness (EOT). Second, an asymmetrical TFET layout with an intrinsic region (L_{IN}) is demonstrated to effectively suppress I_{LEAK} while retaining the same I_{ON} level. These experimental results are confirmed using device and process simulations based on Silvaco TCAD. Further, temperature variation tests are performed to examine the validity of Kane's model [8] of the BTBT process. Finally, we present the first low-frequency noise (LFN) measurements on TFETs and qualitatively explain the different LFN properties of TFETs compared to standard MOSFETs (where LFN measurements are widely used to extract trap properties [9-10]).

II. FABRICATION AND DEVICE STRUCTURE

A. Device fabrication

The fabrication of TFETs started from an SOI substrate with 140 nm BOX and 20 nm active Si layer. The MESA process was employed to define isolated device active areas followed by the definition of gate stack which is composed of three layers, as illustrated in Fig. 1. Two different gate oxides were formed for comparison: either a 6 nm SiO_2 grown by dry oxidation or a 3 nm HfO_2 deposited by ALD. After the deposition of a metal gate (10 nm TiN), 50 nm thick poly silicon is deposited. The 1st spacer was formed by the deposition of 10 nm Si_3N_4, then a 10 nm Si layer was epitaxially grown, followed by NLDD and PLDD implantation. The 2nd spacer and Si layer are formed at the same way. Before the implantation of NHDD and PHDD, a Si_3N_4 layer was formed to protect the intrinsic region L_{IN}. Rapid thermal annealing (RTA) was used to activate the dopants, followed by the metallization.

B. Device structure and bias polarity

The structure of the fabricated TFETs is quite similar to that of MOSFET with two exceptions. Firstly, the dopant types in source and drain are different. Secondly, the structure of our TFETs was rendered asymmetrical by the intrinsic regions L_{IN} separating the drain contact from the channel.

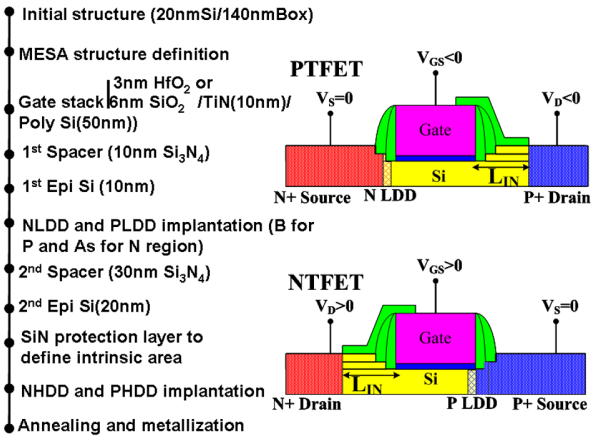

Fig. 1. Fabrication process flow and bias polarity of TFETs. In PTFET, the gate is negatively biased and the BTBT occurs at the n+ doped source. Conversely, in NTFET, the gate is positively biased and the BTBT occurs at the p+ doped source.

For simplicity, the N+ region in a PTFET is defined as source while the P+ region is defined as drain. This definition is opposite in an NTFET, as can be observed in Fig. 1. The source of both PTFETs and NTFETs is always grounded, while the drain is negatively biased in PTFETs and positively biased in NTFETs. For I_{ON} to flow by tunneling at the source-channel junction, $V_{GS} < 0$ for PTFETs and $V_{GS} > 0$ for NTFETs.

III. Electrical Characterization and Analysis

The fabricated devices were systematically characterized. From C-V measurements, the EOT values of TFETs with 6 nm SiO_2 and 3 nm HfO_2 gate oxides were 6 nm and 2.2 nm, respectively. The gate width of all TFETs was 10 µm, the gate length L_G varied from 100 nm to 400 nm, and L_{IN} accounting for the spacer varied from 20 nm to 100 nm.

A. Impact of gate oxide on characteristics

A comparison of I_D-V_{GS} curves of NTFETs and PTFETs with different gate oxides and L_G = 400 nm and $|V_{DS}|$ = 1 V is shown in Fig. 2. Since there exists no unambiguous definition of threshold voltage V_T and S is not a constant value in TFETs, for comparison purposes, we define the V_T as the voltage when drain current starts to surpass 2×10^{-10} A/µm and extract the S value when drain current reaches 2×10^{-12} A/µm, ranging over two decades in drain current. As can be easily observed in Fig. 2, TFETs based on HfO_2 have smaller V_T and higher I_{ON} than those based on SiO_2. The S values are also largely reduced.

The results on devices with different L_G = 100–400 nm show that V_T and S are independent of L_G, as expected in TFETs [11]. This due to the fact the tunneling current is determined by the maximum electric field at the tunneling junction and unaffected by the carrier transport in the channel. The results show that V_T is 4.5V for both NTFETs and PTFETs with SiO_2, whereas V_T is 2.3V for those with HfO_2 gate oxide. As for the S value, both NTFETs and PTFETs with SiO_2 have S value of 1.1 V/dec, which is reduced to 0.33 V/dec in devices with HfO_2. We can note that a formal study has been performed [5]. Here, we discuss only TFETs with comparable characteristics for both types of oxides.

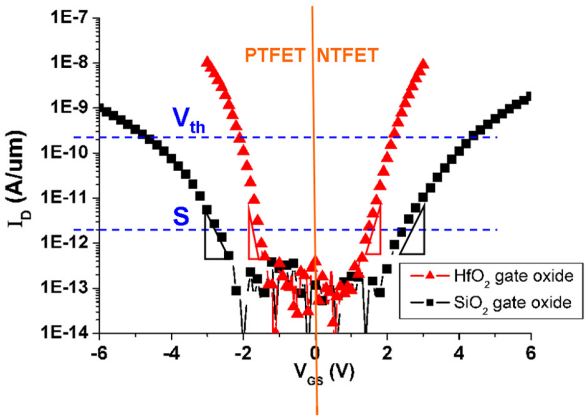

Fig. 2. Measured I_D-V_{GS} curves of both NTFETs and PTFETs based on different gate oxides (L_G =400 nm, $|V_{DS}|$ = 1 V). The inset symbols show the definitions of V_T and S.

The comparison reveals that thinner EOT can lead to lower V_T and S values due to the better electrostatic controllability from the gate. The theoretically achievable S < 60 mV/dec value in TFETs requires excellent electrostatic control of the maximum junction field, which requires minimizing gate EOT and sharpening the S/D lateral doping profile. As a result, few experimental reports of low S have been published thus far [5, 7, 12].

B. Impact of device architecture on characteristics

A potential problem of symmetrical TFETs is the large I_{LEAK} under opposite gate bias, because interband tunneling possible occurs at either the source-channel or the drain-channel junction depending on the sign of V_{GS}. This ambipolar I_{LEAK} can be much more severe for TFETs based on low band-gap semiconductors such as Ge. The solution is to introduce an asymmetrical architecture, such as unequal source/drain doping [7, 13], intrinsic regions and even lateral heterojunctions [7].

In our case, we introduce an intrinsic area to make the device asymmetrical, hence to suppress the ambipolar tunneling current. This method has been proposed from simulation work [7, 14] and experimental data have been presented in [5]. Here, we make a systematic study by the combination of simulation and experiment and also show the possibility to completely suppress the ambipolar I_{LEAK}. Figure 3 shows a NTFET with intrinsic area under different V_{GS} and its corresponding simulated maximum electric field (E_{max}) at source and drain sides. Under positive gate bias, the TFET is in ON state and the tunneling occurs at source side. The E_{max} at the source side is almost constant as L_{IN} increases, shown as the rectangular curve in Fig. 3, which thanks to the negligible potential drop on L_{IN} region.

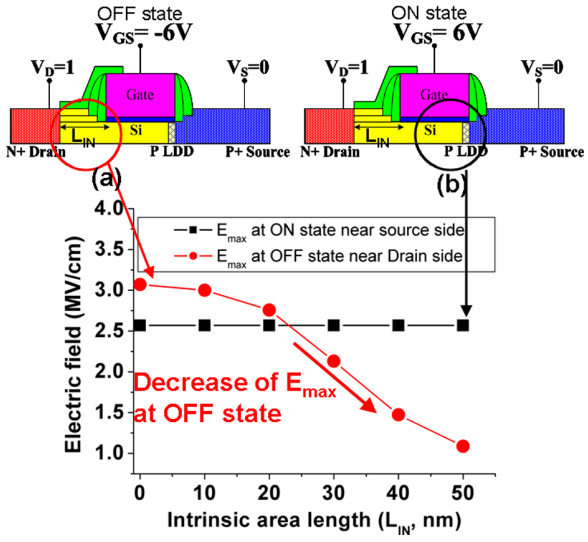

Fig. 3. The maximum electric field (E_{max}) at the tunneling junction of a NTFET with different L_{IN} under positive gate bias and negative gate bias.

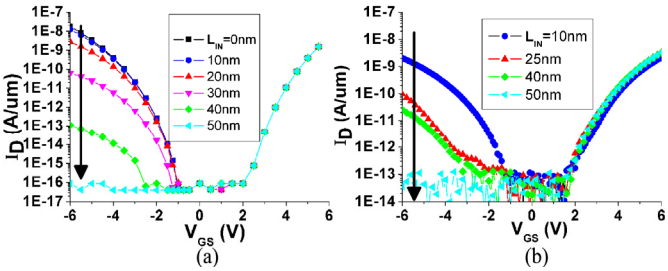

Fig. 4 I_D-V_{GS} curve of NTFETs with different L_{IN} from (a) simulation and (b) experimental results (L_G = 400 nm, V_{DS} = 1 V).

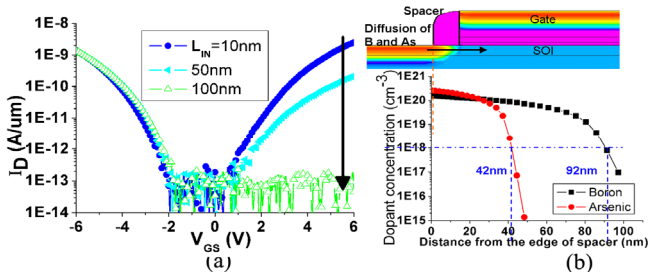

Fig. 5. (a) I_D-V_{GS} curve of PTFETs with different L_{IN} and (b) the simulation about the diffusion length of boron and arsenic.

In contrast, as the gate is negatively biased, the TFET is in OFF state and the tunneling occurs at drain side where the intrinsic area is located. For the TFET with L_{IN} smaller than 20 nm, the E_{max} at OFF state is even slightly larger than that at ON state, see Fig. 3. This due to the fact that the V_{GD} = 7 V at OFF state which is 1 V higher than that of V_{GS} in the ON state. However, as L_{IN} increases larger than 20 nm, the E_{max} at the drain side drops apparently. Since the BTBT rate is directly determined by E_{max}, it can be largely reduced at the drain side due to the increase of L_{IN}. However, at the source side, the E_{max} does not change which means a constant tunneling rate at ON state.

A comparison of the simulated and experimental results for an NTFET with different values of L_{IN} is shown in Fig. 4, where the simulated tunneling current in Fig. 4(a) is obtained from Kane's model as discussed below. The simulated I_{LEAK} of the NTFET with L_{IN} smaller than 20 nm is even slightly higher than the I_{ON} due to the larger E_{max}. As L_{IN} increases from 20 nm to 50 nm, the I_{LEAK} is largely suppressed, whereas I_{ON} is unaffected. Figure 4(b) shows the experimental results for NTFETs with four different L_{IN} from 0 to 50 nm. In agreement with the simulation, the I_{LEAK} of the TFETs without L_{IN} is comparable to I_{ON}, but can be effectively suppressed by increasing L_{IN} to 50 nm.

In PTFETs, the I_{ON} is also unaffected by L_{IN}, as can be seen in Fig. 5(a). However, the full suppression of I_{LEAK} in PTFETs requires a larger L_{IN} = 100 nm. We attribute this difference to the different diffusion coefficients of boron (B) and arsenic (As) in Si. Figure 5(b) shows the simulated doping profiles of implanted B and As after the activation anneal. All parameters in simulation were adjusted according to the fabrication process. As previous work indicates [8], a doping concentration which is lower than 1×10^{18} cm^{-3} can be used to effectively suppress the tunneling. In our case, the I_{LEAK} results from the tunneling at drain side which is doped by As and B in NTFETs and PTFETs, respectively. The characteristic diffusion distance from the edge of spacer to the 10^{18} cm^{-3} value point is 42 nm for As and 92 nm for B, as shown in Fig. 5(b), qualitatively explaining our experimental observations.

C. *Impact of temperature on characteristics*

Fig. 6(a) shows the I_D-V_{GS} of a NTFET with HfO_2 gate oxide, L_G = 400 nm and L_{IN} = 10 nm at temperatures ranging from 77 K to 300 K. The temperature dependence of the TFET I_D can be qualitatively explained by Kane's model in device level as [8]:

$$I_D = A\cdot V_{GS}^{\ 2}\cdot\exp(-\frac{B}{V_{GS}});\ \ A\propto E_G^{\ -0.5};\ \ B\propto E_G^{\ \frac{3}{2}} \tag{1}$$

The dominant temperature effect on the TFETs performance comes from the temperature variation of bandgap E_G, which enters in the exponential of (1). The E_G has weakly negative temperature dependence [15]:

$$E_G(T) = E(0) - \frac{\alpha\cdot T^2}{T+\beta} \tag{2}$$

As temperature increases, the E_G decreases, leading to a corresponding decrease in parameter B and hence an increasing tunneling current.

The validity of Kane's model can be examined by rewriting (1) as:

$$\log(\frac{I_D}{V_{GS}^{\ 2}}) = \log(A) - \frac{B}{V_{GS}} \tag{3}$$

The relation between $\log(I_D/V_{GS}^2)$ and $1/V_{GS}$ is quite linear over the entire temperature range, as shown in Fig. 6(b).

Since the behavior of the TFET at various temperature in our work is quite similar to that reported previously [5] and agree with (1), we can conclude that the weakly positive temperature dependence of the TFET I_D can be used as confirmation of BTBT in the device and that the Kane's model is at least qualitatively effective in describing the BTBT process in Si TFETs.

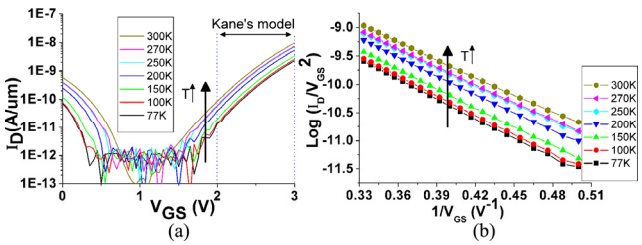

Fig. 6. Relation between (a) I_D-V_{GS} and (b) $\log(I_D/V_{GS}^2)$-$1/V_{GS}$ of an NTFET at various temperatures (L_G = 400nm, V_{DS} = 1 V).

D. Low frequency noise (LFN) characteristics

The LFN caused by the trapping-detrapping process at the channel-dielectric interface has a 1/*f* signature in MOSFETs. As the area of MOSFET decreases below 1 μm^2, only a few interface traps exist in the entire device, leading to a random telegraph signal (RTS) current noise that produces a Lorentzian spectrum whose slope is almost 1/*f*^{2} [9].

Figure 7 compares the LFN of NMOS and NTFETs with the same 6 nm SiO_2 gate oxides showing totally different spectral behavior. In the NMOS with a gate area of 3.5 μm^2 (L_G = 350 nm) the LFN is 1/*f*, whereas in the NTFET, the spectrum of the noise is Lorentzian even though it is much larger (area =25μm^2, L_G = 5 μm).

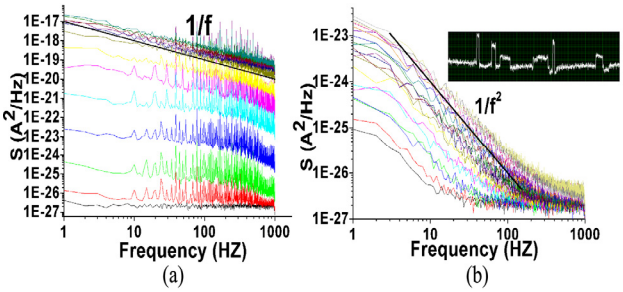

Fig. 7. Comparison of LFN spectrum between (a) NMOS (L_G = 350 nm, V_{DS} = 50 mV, V_{GS} = 0.1-1.5V) and (b) NTFET (L_G = 5 μm, V_{DS} = 1V, V_{GS} = 3-5V). The inset image shows the RTS signal in NTFET.

For TFET, the current is only determined by the tunneling rate, while the channel provides a way for carrier transport. The trapping of carriers at the Si/SiO_2 interface above the channel can only cause the fluctuation of the channel conductance, whereas the tunneling rate at the tunneling junction stays stable. The tunneling rate can only be affected by the trapping process at the Si/SiO_2 interface above the tunneling junction which is very narrow (around 10 nm). Hence, the effective LFN-generating area of the TFET is very small (0.05 μm^2), including only a discrete numbers of traps, just as in a very small MOSFET. This is why the RTS noise is observed in TFET even though its gate area is nominally large.

IV. CONCLUSION

In this paper, we report on the various aspects of Si TFET performance. We demonstrate that the use of HfO_2 gate oxide with smaller EOT leads to a lower threshold V_T and subthreshold slope S than identically processed SiO_2 oxide TFETs, with S decreasing by a factor of ~3. We show that the introduction of an intrinsic region between the channel and the drain in both types of TFETs can largely suppress the I_{LEAK} without impacting I_{ON}: I_{LEAK} decreases from 2×10^{-9} A/μm to sub 1×10^{-13} A/μm as L_{IN} is increased to 50 nm (NTFET) and 100 nm (PTFETs). The difference in the L_{IN} required to suppress the ambipolar I_{LEAK} is explained by the different diffusion profiles of B and As, as confirmed by TCAD simulations. Finally, LFN characterizations are performed on MOSFET and TFETs. The results reveal that, unlike in MOSFETs, the RTS noise is dominant in TFETs even though the nominal gate area is large, because the relevant area where the interband tunneling takes place is much smaller than the physical L_G.

ACKNOWLEDGMENTS

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