Numerical Queue Solution of Thermal Noise-Induced Soft Errors in Subthreshold CMOS Devices

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ABSTRACT

Power consumption requirements drive CMOS scaling to ever lower supply voltages, reducing the stability margin with respect to thermal noise and raising the probability for thermally-induced soft errors. Given the long time scale of noise-induced soft errors, conventional Monte Carlo simulations cannot be used to predict error rates and alternative approaches are needed. In this paper, the analysis of thermal fluctuations in a CMOS flip-flop is performed using a 2D queue that maps the available configurations for the flip-flop in terms of electron populations on the two inverters, with the two stable logic states at the opposite corners of the 2D matrix. Trial simulations for model systems show that the thermally-induced logic transitions involve only a limited number of states immediately above and below the main diagonal of the full 2D queue. We present a numerical solution based on variable precision arithmetic for a truncated 2D queue consisting of a variable number of near-diagonal states. It is shown that increasing the width of the near-diagonal queue, an accurate solution for the error rate is asymptotically obtained without the need to consider the full 2D queue. Our approach is used to calculate the mean time to failure of flip-flops built in a 45-nm fully-depleted silicon-on-insulator (FD-SOI) technology modeled in the subthreshold regime, including parasitics. As a predictive tool, the framework can be used to investigate the thermal stability of devices built in future technologies and as a measure of device reliability in VLSI design.

Categories and Subject Descriptors

B.3 [**Memory Structures**]: General; B.3.4 [**Reliability, Testing, Fault Tolerance**]: Diagnostics; B.6 [**Logic Design**]: General

General Terms

Reliability, Theory

Keywords

Reliability, CMOS logic devices, Markov process, Poisson distribution, Laplace transform, Monte Carlo method

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1. INTRODUCTION

Noise margins represent a reliability concern for digital circuits and the nature of the noise has been traditionally dominated by factors such as supply voltage fluctuations and capacitive cross-coupling. However, with the miniaturization process, CMOS devices continue to scale down in both physical dimension and operating voltage V_{dd}, giving rise to other noise sources, such as thermal noise, electromagnetic coupling, and hot-electron effects [1][2]. The relatively wider process-related spread of gate threshold voltages will also further reduce the operational noise margins.

In advanced CMOS transistors, noise measurements are widely used to characterize processing quality at the device level, but have had little impact to date on higher-level circuit design because, at the current stage of semiconductor technology, the number of electrons flowing across the channel of a MOS transistor is sufficiently large to render the current fluctuations negligible. However, as operating voltages and transistor gate lengths are scaled down, current fluctuations due to a few electrons will become more significant, thereby increasing the likelihood of soft errors.

Interest in ultra-low-voltage digital circuits has been growing in the past years, prompted by the need to reduce the overall energy consumption[3][4]. If power reduction requirement is particularly stringent in some specific application, such as biomedical implants, environmental monitoring devices or space systems, the option of further reducing V_{dd} into the subthreshold regime could prove useful [5][6]. This reduction in the operating voltage raises the need for probabilistic frameworks capable of analyzing the effect of noise sources on low V_{dd} devices. The error rate estimates arising from such models can serve as a guideline for the design of logic circuits operated at ultra-low or subthreshold voltages.

In previous work [7], a theoretical framework was introduced for calculating the soft-error rates due to thermal noise in a flip-flop operated at subthreshold voltages. Representing the flip-flop as a 2D queue, simulations on small scale models indicated that the error-inducing thermal fluctuations are dominated by the transitions along the diagonal of the queue. A symbolic solution was derived for 1D diagonal approximation of the full queue which allowed for the estimation of error rates in real devices. While the symbolic solution has the advantage that it evaluates directly the terms that are present in the transition time expression, it is difficult to extend the symbolic solution to larger near-diagonal 2D queues. In this paper, a numerical solution for truncated 2D queue approximations of the full queue, consisting of a variable number of near-diagonal states is

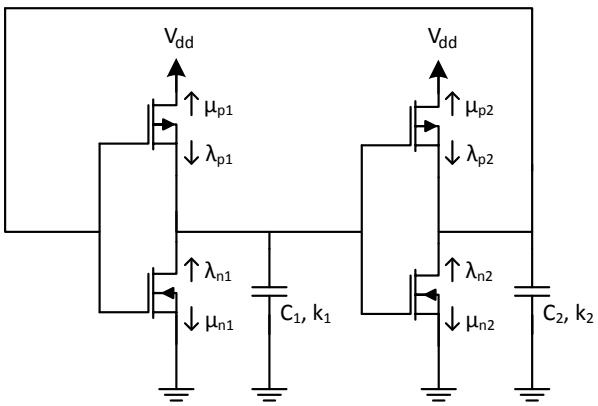

Figure 1: The modeled flip-flop circuit. Capacitors C_1 and C_2 represent the node capacitances associated with each inverter. For each transistor, the charging and discharging rates λ and μ determine the electron populations on the node capacitances.

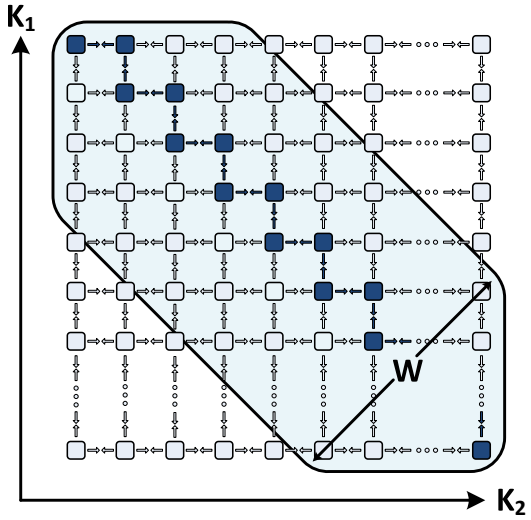

Figure 2: Two dimensional queue of available states for CMOS flip-flop with k_1 and k_2 representing the electron populations on the two inverters. The solution for the 1D diagonal approximation, represented here with filled square, was derived in [7]. In this paper the analysis extended to a truncated 2D queue that is solved numerically using a variable number of near-diagonal states. The variable parameter in successive approximations is W, the width of the band of near-diagonal states considered in the simulations.

presented. It is shown that increasing the width of the near-diagonal queue, an accurate solution for the error rate is asymptotically obtained without the need to consider the full 2D queue.

2. THE 2D QUEUE REPRESENTATION

As described in [7], the possible configurations for the flip-flop, Fig. 1, in terms of the electron populations k_1, k_2 on the two load capacitors C_1, C_2 can be represented as a square 2D queue, as shown in Fig. 2. A given state from the 2D queue can be denoted as (k_1, k_2) and is surrounded by four states denoted by $(k_1 \pm 1, k_2 \pm 1)$. Each state is fully characterized by the electron populations and the transition rates to each of the neighboring states can be computed from the published or theoretically predicted device characteristics [8].

If at time $t = 0$ the system is known to be in state labeled i, the probability that it is still in state i some time later is $e^{-(\Sigma r_i)t}$, where Σr_i is sum of the outward rates from state i in four directions (or less if state i is an edge or a corner state). The probability density for transitions out of this state to any neighboring state is:

$$p_i(t) = (\Sigma r_i)e^{-(\Sigma r_i)t} \tag{1}$$

The residence time for state i is given by the first moment of the transition probability density:

$$\tau_i = \int_0^\infty t \cdot p_i(t)dt = (\Sigma r_i)^{-1} \tag{2}$$

Denoting the rates connecting two states labeled i and q by r_{iq}, the probability density for transitions out of state i to a neighboring state q is given by $r_{iq}p_i(t)/\Sigma r_i$. The factor $r_{iq}/\Sigma r_i$ is the probability that when the system leaves state i, it goes to state q.

The moments of the probability density function in the context of queuing theory [9][10] can be calculated using the Laplace transform. The probability density for the time of reaching state q via state k if staring in state i is given by:

$$p_{i\to k\to q}(t) = \frac{r_{i,k}}{\Sigma r_i}\int_0^t p_i(t_k)p_{k,q}(t-t_k)dt_k \tag{3}$$

The Laplace transform of such a convolution is a simple product:

$$L(p_{i\to k\to q}(t)) = \frac{r_{i,k}}{\Sigma r_i}L(p_i(t))L(p_{k,q}(t)) \tag{4}$$

Considering the expression for $p_i(t)$, Eq. (1) yields

$$L(p_i(t)) = \int_0^\infty p_i(t)e^{-st}dt = \frac{\Sigma r_i}{s+\Sigma r_i} \tag{5}$$

From an initial state i, the system may have to move through a number of intermediate states to reach state q. Therefore the probability density to reach q must be the sum of all possible densities through the different intermediate neighboring states k:

$$L(p_{i,q}(t)) = \sum_{k\neq q}\frac{r_{i,k}}{s+\Sigma r_i}L(p_{k,q}(t))). \tag{6}$$

If state q is the sink for which all the outward rates are zero, then Eq. (6) modifies to

$$L(p_{i,q}(t)) = \sum_{k\neq q}\frac{r_{i,k}}{s+\Sigma r_i}L(p_{k,q}(t))) + \frac{r_{i,q}}{s+\Sigma r_i} \tag{7}$$

The probability density function $p_{i,f}(t)$ requires solving for the Laplace transform associated with the transition between the initial and final states. The Laplace transform is used to calculate the moments of the probability density

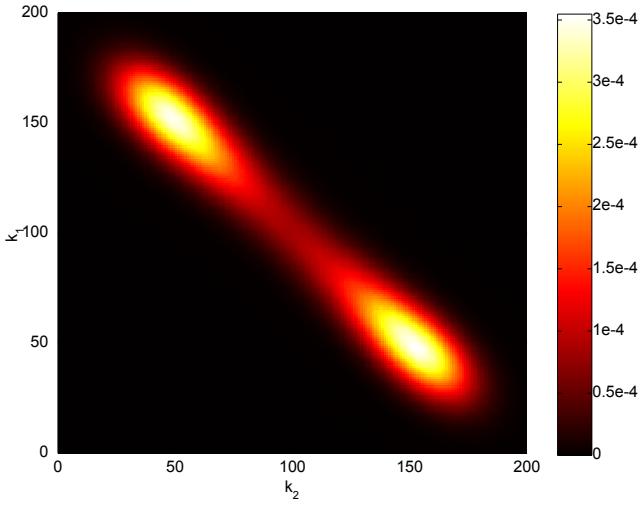

Figure 3: MC simulations run at room temperature for a model flip-flop with fixed capacitance described in [9] and driven at an artificially low voltage $V_{dd} = 0.075V$, show that the thermally-induced logic transitions involve only a limited number of states immediately above and below the main diagonal of the full 2D queue. The gray scale is exponential, illustrating the high occupation probability for the states within the 2D queue that are associated with the stable logic states, limited occupation for the near-diagonal states that participate in the transition and negligible presence in the off-diagonal states.

function. The n^{th} order moment is given by:

$$M_n = (-1)^n \lim_{s\to 0} \frac{d^n}{ds^n} L_{i,f}(s) \tag{8}$$

As described in [7], a symbolic solution was found for 1D diagonal approximation to the full 2D queue as illustrated in Fig. 2 with filled squares. The solution for the 1D diagonal approximation made it possible to estimate the error rates for flip-flops built in a 45-nm FD-SOI technology [11] as well as for devices built in a future technology described in the ITRS [1]. Comparison with Monte Carlo simulations for model flip-flops with a reduced number of electrons, confirmed that the 1D diagonal gives the order of magnitude of the mean time to a thermally-induced logic error.

The symbolic pattern for the simplest near-diagonal approximation, consisting of the main diagonal and the states immediately below it, increases exponentially in complexity with respect to the simple 1D diagonal path. The higher-order moments needed to fully describe the statistics of error rates present an even higher degree of pattern complexity, making the symbolic solution impractical.

Moving beyond the symbolic approach, the guideline for extending the analysis arises from Monte Carlo simulations of modeled flip-flops operated at artificially low voltages ($V_{dd} = 0.075V$), see Fig. 3. These simulations show that the thermal broadening of the occupied logic states occurs predominantly along the diagonal with a spread influenced by the ratio of the thermal and driving energy k_BT/qV_{dd}. It can be seen that the states within the 2D queue that are involved in transition are only the ones that lie near the main diagonal, while off-diagonal states are not relevant for the thermal transition process. Therefore, considering ever larger near-diagonal approximation with increasing W, Fig. 2, is expected to lead asymptotically to an accurate solution for the error rates, without the need to solve the complete 2D queue.

3. NUMERICAL APPROACH FOR SOLVING THE TRUNCATED 2D MARKOV CHAIN

3.1 Forming a system of equations for calculating the probability moments

The Laplace system of equations described in Eq. (6) can be written in matrix form

$$\mathbf{A}(s)\mathbf{x}(s) = \mathbf{b}(s) \tag{9}$$

where $\mathbf{A}(s)$ is a matrix of coefficients, $\mathbf{x}(s)$ is a vector of Laplace transforms of the time-dependent failure PDFs for the states and $\mathbf{b}(s)$ is the right hand side vector corresponding to the last term in Eq. (7).

According to Eq.(8), the different probability moments of the PDFs are equal in amplitude to the corresponding derivatives of the Laplace transforms, $\mathbf{x}(s)$, evaluated at $s = 0$. For example, to obtain the mean time to failure, one needs to evaluate $-\mathbf{x}'(s)\,|_{s=0}$. A systematic approach to solve for the first four moments will be presented in this section:

One may start by differentiating Eq. (9) with respect to s, four times to get

$$\mathbf{A}'\mathbf{x} + \mathbf{A}\mathbf{x}' = \mathbf{b}' \tag{10}$$

$$\mathbf{A}''\mathbf{x} + 2\mathbf{A}'\mathbf{x}' + \mathbf{A}\mathbf{x}'' = \mathbf{b}'' \tag{11}$$

$$\mathbf{A}^{(3)}\mathbf{x} + 3\mathbf{A}''\mathbf{x}' + 3\mathbf{A}'\mathbf{x}'' + \mathbf{A}\mathbf{x}^{(3)} = \mathbf{b}^{(3)} \tag{12}$$

$$\mathbf{A}^{(4)}\mathbf{x} + 4\mathbf{A}^{(3)}\mathbf{x}' + 6\mathbf{A}''\mathbf{x}'' + 4\mathbf{A}'\mathbf{x}^{(3)} + \mathbf{A}\mathbf{x}^{(4)} = \mathbf{b}^{(4)} \tag{13}$$

in which the s dependence is omitted for brevity. Solving for $\mathbf{x}'$, $\mathbf{x}''$, $\mathbf{x}^{(3)}$ and $\mathbf{x}^{(4)}$ from Eqs. (10)-(13) yields

$$\mathbf{x}' = \mathbf{A}^{-1}\left(\mathbf{b}' - \mathbf{A}'\mathbf{x}\right) \tag{14}$$

$$\mathbf{x}'' = \mathbf{A}^{-1}\left(\mathbf{b}'' - \mathbf{A}''\mathbf{x} - 2\mathbf{A}'\mathbf{x}'\right) \tag{15}$$

$$\mathbf{x}^{(3)} = \mathbf{A}^{-1}\left(\mathbf{b}^{(3)} - \mathbf{A}^{(3)}\mathbf{x} - 3\mathbf{A}''\mathbf{x}' - 3\mathbf{A}'\mathbf{x}''\right) \tag{16}$$

$$\mathbf{x}^{(4)} = \mathbf{A}^{-1}\left(\mathbf{b}^{(4)} - \mathbf{A}^{(4)}\mathbf{x} - 4\mathbf{A}^{(3)}\mathbf{x}' - 6\mathbf{A}''\mathbf{x}'' - 4\mathbf{A}'\mathbf{x}^{(3)}\right) \tag{17}$$

all evaluated at $s = 0$. The values for $\mathbf{x}$ and its derivatives at zero can be obtained by forward substitution in Eqs. (14)-(17). It should be noted that $\mathbf{x}(0) = \mathbf{1}$ by the definition of Laplace transform and that all PDFs are positive definite and normalized to unity.

From Eq. (6), all the elements of the matrix $\mathbf{A}(s)$ as well as those of the vector $\mathbf{b}(s)$ have the form

$$A_{ij}(s) = \frac{r_{ij}}{s + c_{ij}} \tag{18}$$

in which r_{ij} is the rate of flow from the state (i, j) to a specific neighboring state and c_{ij} is the sum of all rates exiting the state (i, j). The derivatives of (18) can be easily

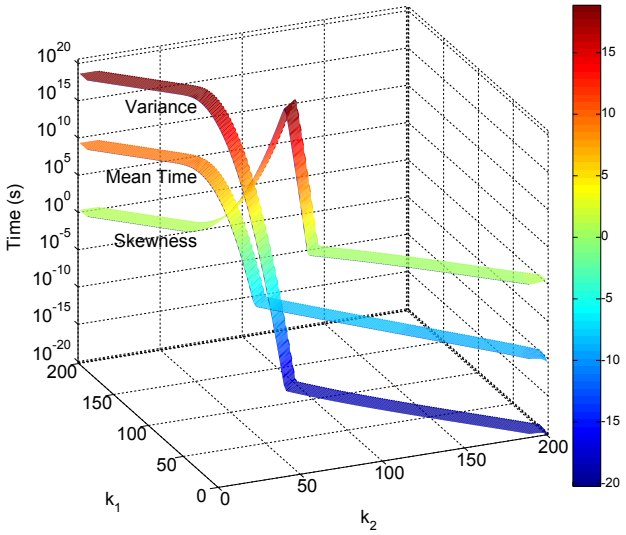

Figure 4: The first three moments of the probability density function give the mean time to failure (seconds), variance and skewness of the probability curve. The x and y axes map the 2D queue, while the z axis presents the numerical results for time to failure in a FD-SOI CMOS flip-flop operated at $V_{dd} = 0.2V$.

evaluated to any order at $s = 0$:

$$\left.\frac{d^n A_{ij}(s)}{ds^n}\right|_{s=0} = \left.\frac{d^n}{ds^n}\left(\frac{r_{ij}}{s + c_{ij}}\right)\right|_{s=0} = \frac{(-1)^n n! r_{ij}}{c_{ij}^{n+1}} \quad (19)$$

Using this equation, all the terms in Eqs. (14)-(17) can be written solely in terms of the rates, independent of the variable s and one can solve for $\mathbf{x}'$ through $\mathbf{x}^{(4)}$ by Gaussian elimination.

3.2 Near-diagonal approximation and multiple precision arithmetic

The 2D Markov queue for a flip-flop with maximum number of N electrons has N^2 possible states, therefore the matrix $\mathbf{A}$ will have N^4 elements. Taking a realistic device operated at the subthreshold voltage of $V_{dd} = 0.2V$, results in $N \approx 200$. The required memory for containing the non-sparse matrix $\mathbf{A}$ during the Gaussian elimination will be about 12GB, assuming 8-byte double-precision format for each element. The other computational burden is that for $N \geq 40$, the system shows signs of ill-conditioning to the point that at about $N \geq 50$ the final results are not valid.

The ill-conditioning problem can be addressed by using arbitrary/multiple precision arithmetic (MPA) [1] where more bits are allocated for storing each element than in conventional double-precision format. No matter how badly the system is ill-conditioned, it is only relative to the degree of precision used and one may always increase the precision to compensate for the numerical errors caused by high degrees of system sensitivity. However the use of MPA leads to even larger memory requirements and much lower processing speeds.

These constraints may be enormously relaxed by only considering the states on or near the diagonal connecting the

[1]The GMP free library was used for the simulations in this project

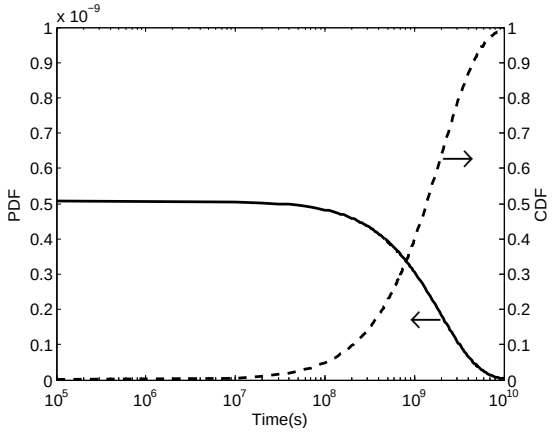

Figure 5: Normalized Probability Density Function and Cumulative Distribution Function for a flip-flop operated at $V_{dd} = 0.2V$ with $N \approx 200$

two stable states of the flip-flop. The memory required for the $N = 300$ system mentioned above drops down to 1.2GB when only taking into account the states within a $W = 20$ band around the diagonal. The processing time also reduces to an hour, on a 16 core workstation. [2]

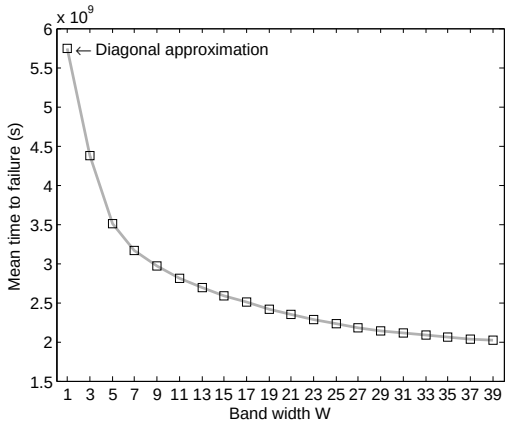

Figure 6: Increasing the width, W, of successive band diagonal queues results in an asymptotic refining of the accuracy in predicting the error rates. This confirms that only a limited number of states immediately above and below the main diagonal are relevant in the analysis of thermally-induced errors. Therefore to estimate the soft-error rates it is not necessary to solve the full 2D-queue, which reduces the computational complexity from N^2 to WN. This result is of particular relevance for a future analysis that will address logic devices operated at voltages above threshold where the number, N, of electrons is much larger.

The mean time to failure, variance and skewness for FD-SOI CMOS flip-flop are shown in Fig. 4. The device was biased at $V_{dd} = 0.2V$ considering a worst case scenario of 15%

[2]Four Quad-Core 2.3GHz AMD Optron 8356, 64GB physical memory

threshold variation among the p and n transistors and operated at room temperature. The mean time to failure for this single device is $\sim 10^9$ seconds which is equivalent to 30 years. This is a very high error rate on a practical basis: nowadays, a modern processor has about 8MBs of built-in SRAM cache, utilizing approximately on the order of 10^8 flip-flops running concurrently. Assuming independent errors, the mean time to failure drops down to about 30 seconds for such a system, assuming no error correction. Clearly, operating the system at higher voltages improves the stability exponentially. On the other hand, higher temperature, expected in future circuits will also reduce the noise margins. Our approach is capable of accounting for the variation in these technological and operational factors, to produce an estimate of error rates for subthreshold flip-flops.

As the Fig. 4 suggests, the variance is typically twice as large in orders of magnitude as the mean, therefore the standard deviation is the same order of magnitude as the mean, suggesting a very wide probability distribution [12]. The probability density function (PDF) and cumulative distribution function (CDF) for this system are calculated using the first three moments and shown in Fig. 5. From the shape of the probability distributions, it can be seen that the time scale in which the CDF reaches a value of 1% is two orders of magnitude less than the mean time to error.

The effect of different band widths, W, in calculating the mean time is shown in Fig. 6. Increasing the width, W of successive band diagonal queues results in an asymptotic refining of the accuracy in predicting the error rates. This confirms that only a limited number of states immediately above and below the main diagonal is relevant in the analysis of thermally-induced errors. The same asymptotic trend is observed in the calculations for the higher moments. Therefore, to obtain the statistics of the soft-error rates it is not necessary to solve the full 2D-queue, which reduces the computational complexity from N^2 to WN. This result is of particular relevance for devices operated at higher V_{dd}, where N is much larger.

3.3 Formulation of the steady-state thermal distribution

Interestingly, our numerical approach can also be used to derive the steady-state statistics of the thermally-induced logic transitions. Given an initial probability distribution for the states of the system, the continuity equation governs the dynamics of probability flow between the states:

$$-\alpha \frac{\partial P_{i,j}(t)}{\partial t} = \left(\nabla \cdot rP(t)\right)\big|_{i,j} \qquad (20)$$

in which α is a constant of proportionality and $rP(t)$ indicates the net probability flow out of the state (i,j). As $t \to \infty$ the system acquires a global steady state and the probabilities lose their time dependence, making the left hand side of Eq. (20) zero. In this condition, expanding the discrete divergence in the right hand side of the same equation reads

$$\begin{aligned}(u_{i,j} + d_{i,j} + r_{i,j} + l_{i,j})\, P_{i,j} = d_{i+1,j} P_{i+1,j} + \\ u_{i-1,j} P_{i-1,j} + l_{i,j+1} P_{i,j+1} + r_{i,j-1} P_{i,j-1}\end{aligned} \qquad (21)$$

Eq. (21) applied to all the states within a band around the diagonal produces a system of equations that can be solved using the same techniques described above. The thermal distribution for an FD-SOI CMOS flip-flop with 15% threshold variation is shown in Fig. 7. Because of the asymmetry in the device resulting from the threshold variation, it is $\sim 10^{37}$ times more likely to find the device in the stronger stable state than in the weaker stable state, if let the device run indefinitely without applying an input. More importantly, Fig. 7 shows the steady-state thermal broadening of both logic states similar to Fig. 3 but without recourse to Monte Carlo simulations.

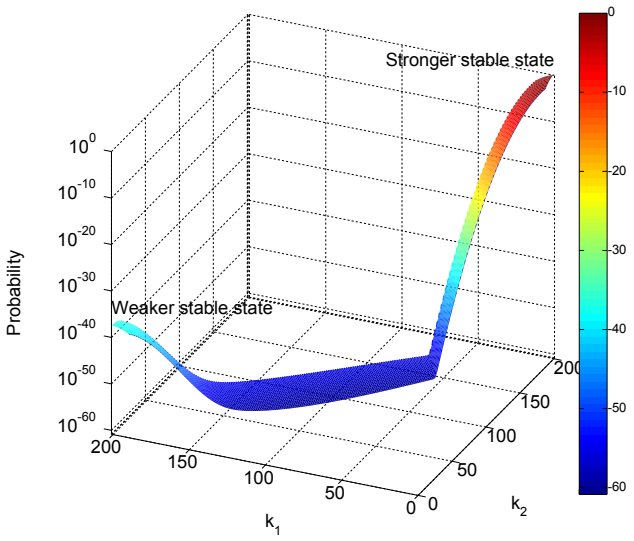

Figure 7: The process-induced threshold variations in the transistors that make up the flip-flop render a given logic state to be more stable than the other. Steady-state thermal broadening for an FD-SOI CMOS flip-flop operated at $V_{dd} = 0.2V$ illustrates the confining of the system within the well defined logic states and exponentially rare transitions. The x and y axes map the 2D queue, while the z axis presents the numerical results for the occupation probability of states in a near-diagonal queue.

4. IMPLICATIONS FOR VLSI DESIGN

The classical approach to noise analysis is based on computing the independent mean square current or voltage fluctuation in each device within the bandwidth of the circuit [13]. The underlying assumptions are that the noise statistics are stationary and the noise amplitude is sufficiently low so that the circuit behaves linearly. Under those assumptions, the noise energies are added at the output of the circuit to find a total mean square noise voltage. That limited information does not predict the time it would take to disturb the state of a flip-flop. Moreover, a flip-flop that has sufficient noise fluctuation to change state does not satisfy either classical assumption, because the noise current distributions change with the storage node potentials, as do the noise gains.

Given these limitations, it is impossible to compute these error rates using conventional electronic circuit simulators such as SPICE [14], engendering the need for probabilistic frameworks capable of analyzing the effect of thermal noise on low-power devices. Our approach provides such a technique and takes into account parameters such as supply voltage, temperature, physical dimensions of the logic device and process-related spread of threshold voltages.

5. CONCLUSIONS AND FUTURE WORK

This paper extends the analysis of the effect of thermal noise fluctuations on the logic stability of CMOS flip-flops within the 2D queue representation that was introduced in [7]. While MC simulations for systems of real interest fail to describe the transition process resulting in a logic error due to the long time scales involved, for model systems run at artificially low V_{dd}, such simulations offer valuable insight in the statistics of the process. It was shown that the logic transitions involve only a limited number of states immediately above and below the main diagonal of the full 2D queue.

A numerical solution based on variable precision arithmetic for a truncated 2D queue consisting of a variable number of near-diagonal states is presented in this paper. It is shown that increasing the width W of the band diagonal, an accurate solution for the error rate is asymptotically obtained without the need to consider the full 2D queue. The same asymptotic trend is observed in the calculations for the higher moments. Therefore, to obtain the statistics of the soft-error rates it is not necessary to solve the full 2D-queue which reduces the computational complexity from N^2 to WN. This result is of particular relevance for a future analysis that includes logic devices operated at higher voltage and into the above threshold region where the number of electrons N is much larger.

The numerical solution is used to calculate the mean time to failure of flip-flops built in a 45-nm FD-SOI technology modeled in the subthreshold regime. The error rates for individual devices built in this technology show that considering the very large number of devices in modern integrated circuits, thermal errors are a serious issue for the worst-case scenario of up to 15% threshold shifts of opposite sign in the two inverters operated at subthreshold V_{dd}. These results highlight the importance of the extended analytical framework presented in this paper as a predictive tool to investigate the reliability of a class of logic devices. In the future, we plan to extend our analysis to SRAM cells operated in subthreshold using current and ITRS predicted ultimate CMOS transistors. This can be done by expanding the queue to the higher dimensions to map the states introduced by the two pass-gate transistors in the SRAM. The same strategy can be applied to logic circuits of higher complexity provided they are operated at subthreshold.

6. ACKNOWLEDGMENTS

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