A tunneling field effect transistor model combining interband tunneling with channel transport

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We present a model for the tunneling field-effect transistor (TFET) comprising a series connection of a metal-oxide-semiconductor FET (MOSFET) with a gate-controllable tunneling diode. Through the introduction of MOSFET in the model, both operational regimes of TFET are handled correctly, with the tunneling diode dominating at low interband tunneling current and the MOSFET component dominating at high tunneling current. The comparison between our model, TCAD simulations and experimental data on TFETs with different gate oxide and channel thicknesses over the full range of gate and drain bias confirms the model's reliability and accuracy. At low tunneling current, the model further simplifies to a compact analytical model. With minor modifications, our model can also be applied to multi-gate TFET architectures. © *2011 American Institute of Physics*. [doi:10.1063/1.3658871]

I. INTRODUCTION

As a potential candidate to replace the metal-oxide-semiconductor field-effect transistor (MOSFET), the tunneling FET (TFET) has recently attracted much interest due to its low OFF current (I_{OFF}) and the possibility of reaching subthreshold slope (S) below the $2.3 \times (kT/q)$ limit of a standard MOSFET.[1–13] Tunneling FETs with S lower than 60 mV/decade at room temperature have been demonstrated experimentally, albeit with relatively low ON current (I_{ON}).[1–4] Recent research has concentrated on enhancing the I_{ON} by employing low bandgap materials such as germanium,[5,6] III-V compounds,[7] carbon nanotubes,[8] and even graphene.[9,10] With improving experimental performance, reliable models are urgently required to explain the results and optimize the structures.

In the past, technology computer-aided design (TCAD) simulation combining the local Kane's model[11] with numerically obtained potential distributions have been used for qualitative analysis and TFET performance predictions.[12–14] A more precise and complicated numerical method using non-equilibrium Green's function (NEGF) is also available.[15,16] On the other hand, an analytical model would be very useful to aid physical understanding and provide quick predictions, and indispensable for circuit-level simulation and modeling.

Several analytical TFET model have been published to date.[17–20] They are generally based on analytically solving the Poisson equation at the tunneling junction and then calculating the tunneling current by inserting the obtained electric field into Kane's model for interband tunneling. In Ref. 19, the channel was assumed to be always fully depleted, so that the effect of drain voltage (V_D) on tunneling junction is excluded. Even in models that include the effect of V_D, however, the channel is still assumed to be depleted, which is usually incorrect at high gate voltage (V_G) in a long-channel TFET.[20] None of the models published to date quantitatively captures the two working regimes in a long-channel TFET: the "saturation regime" in which the tunneling current is independent of V_D and the "linear regime" in which the current depends on both V_D and V_G. Furthermore, carrier transport along channel is typically ignored, even though the channel transport is expected to limit I_{ON} in TFETs with a sufficiently high tunneling rate.

In this paper, we propose an analytical model for the TFET regarded as series connection of a gate-controllable tunneling diode (GTD) with a MOSFET. The potential distribution around the tunneling junction is obtained by solving the Poisson equation with the pseudo-2D method,[17,20] including the influence of the channel potential that is determined by the series-connected MOSFET. Kane's model serves to derive the tunneling current, but using the average electric field along shortest tunneling width (E_{TW}) rather than the local maximum electric field (E_{max}).[19,21] By combining the current-voltage (I-V) equations of the tunneling diode and MOSFET, the channel potential is determined in both linear and saturation regimes, yielding the actual value of the drain current (I_D). Generally, the channel transport in the MOSFET must be solved numerically, but our model reduces to a compact and explicit analytic expression if the tunneling rate is relatively low.

The model was validated by comparing the predicted potential profile at the tunneling junction with TCAD simulations for various biasing values, gate oxide (T_{ox}) and channel (T_{Si}) thicknesses. Further, our model accurately predicts experimental I-V data over a wide range of biasing with interband tunneling parameters that agree with published results. Finally, the model can be easily extended to multi-gate structures and used to predict the performance of TFETs with different technological parameters (gate oxide thickness, channel thickness), device geometries, and alternative materials.

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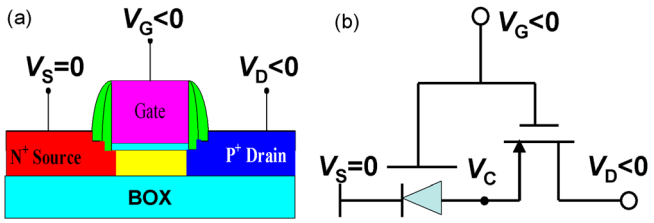

FIG. 1. (Color online) (a) Schematic view of a PTFET with gate and drain negatively biased. The schematic structure with raised source/drain and two spacers is the same as our measured devices. (b) The proposed model of the PTFET in which the channel and drain belong to a MOSFET in series with the gate-controllable tunneling diode located at source.

II. MODEL DERIVATION

A schematic view of a p-type TFET (PTFET) is shown in Fig. 1(a). At sufficiently negative V_G, a reverse-biased tunneling junction is formed at the source side. As illustrated in Fig. 1(b), we model this TFET as the series connection of a p-type MOSFET (PMOSFET) at the drain side with a GTD at the source. The PMOSFET has a well-defined drain voltage V_D, but its virtual source at the start of the channel coincides with the cathode of the GTD and is at a potential V_C determined by current continuity.

We have performed TCAD simulations using Silvaco Atlas (version 3.18.17.R) to analyze the TFET and MOSFET properties. Figure 2 compares the surface potential profiles of the MOSFET with two TFETs possessing either a normal or an exaggerated interband tunneling rate. The exaggerated tunneling rate is implemented by directly decreasing the exponential parameter B_K in Kane's model[11] from 21 MV/cm to 1 MV/cm, mimicking an optimized future TFET structure with higher tunneling (achievable, for example, by implementing the GTD in a lower bandgap material like Ge). For the TFET with normal Si junction tunneling rate, the potential drop in the channel is minimal, except for the pinched off depletion region near the drain. However, if the tunneling rate is large, the high I_{ON} of TFET induces a large potential

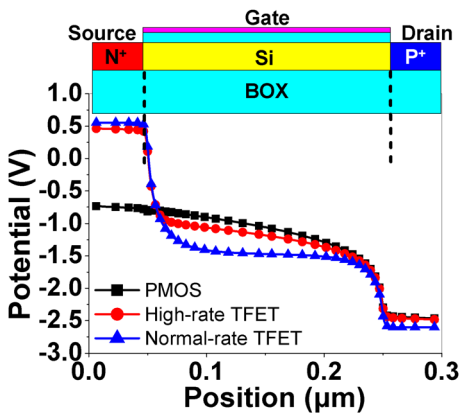

FIG. 2. (Color online) Comparison of TCAD-simulated surface potentials between three devices: TFET with normal Si interband tunneling rate; TFET with exaggerated tunneling rate; and a regular MOSFET without a tunneling junction at the source. The simplified structure of the simulated TFET is shown in the upper inset of Fig. 2. The simulated MOSFET is identical to the TFET, except that both source and drain are p^+ doped. The PTFET with exaggerated tunneling rate has the same potential profile as the MOSFET. The simulated device has $L_G = 200$ nm, $T_{si} = 20$ nm and $T_{ox} = 2$ nm with bias of $V_G = -1.5$ V and $V_D = -2$ V.

drop in channel. The surface potential of the TFET with exaggerated tunneling rate is almost the same as that of the MOSFET in the channel and drain regions except that there is an extra drop at the source junction due to the built-in junction potential, as shown in Fig. 2. As a result, if the tunneling rate is high enough, only a small potential drop is needed at tunneling junction to produce a high current; the current will be restricted by the carrier transport along the channel, so a TFET with high tunneling rate degenerates into a MOSFET.

A. Current continuity and *I-V* characteristic of the GTD

The TFET *I-V* characteristics can be obtained by using current continuity and setting the current $I_D(V_G, V_C)$ of the GTD equal to the $I_D(V_G, V_D - V_C)$ of the series connected MOSFET with its source at V_C. We need to combine the well-known *I-V* relations for MOSFET (Ref. 22) with a model incorporating the V_G and V_C dependence of the GTD current.

One possible approach is to solve the Poisson equation at the junction and then use the obtained maximum electric field (E_{max}) in the local Kane's model.[20] However, the use of E_{max} can greatly overestimate the tunneling current due to the non-uniformity of the electric field at tunneling junction. Instead, the use of the mean electric field (E_{TW}) along the shortest tunneling width (L_{TW}) in the WKB approximation of interband tunneling has been shown to be more accurate in planar Si *pn* tunnel junctions.[21]

A schematic view of a GTD on SOI substrate is shown in Fig. 3(a). Since the tunneling rate decreases exponentially with increasing tunneling width, the analytical model is still fairly accurate by only considering the shortest tunneling path. This significantly simplifies the analytical model. The surface potential along the tunneling direction can be determined by the electrostatic potentials of the gate ($\varphi_G = V_G - V_{FB}$), source ($\varphi_S = V_S + V_{biS}$), and channel ($\varphi_C = V_C + V_{biC}$), referenced to the midgap Fermi level E_i in the nominally undoped channel.[23] Note that the two terms in the channel potential (φ_C) consist of the channel voltage V_C induced by the current flow through the channel and drain junction and the channel built-in potential V_{biC} that reflects the change of the Fermi level in the channel induced by the V_G. Following the pseudo-2D method of Ref. 20, an equation describing the top surface potential of tunneling junction can be obtained as

$$\varphi_t(x) = C \times e^{\frac{x}{L_d}} + D \times e^{-\frac{x}{L_d}} + \varphi_G \quad \text{and} \quad L_d = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} \times T_{ox} \times T_{si}}, \tag{1}$$

where φ_t is the top surface potential, L_d is the characteristic decay length determined by the T_{ox} and active layer T_{si} thicknesses, and C and D are the coefficients determined by the boundary conditions of the channel region. After inserting the channel boundary conditions, one obtains

$$\varphi_t(x) = (\varphi_C - \varphi_G) \times cosh\left(\frac{x}{L_d}\right) + \varphi_G. \tag{2}$$

From Eq. (2), as x decreases toward zero, the potential decays from φ_S at source side to φ_C at channel with the

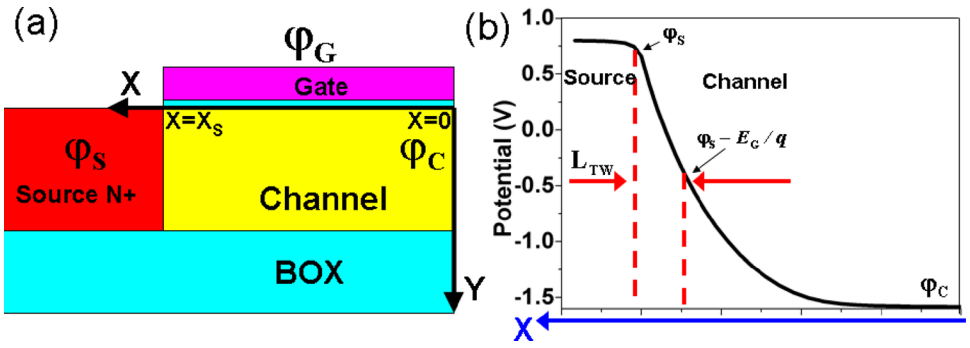

FIG. 3. (Color online) (a) Schematic view of the tunneling junction in which the potential distribution is determined by the potentials of the gate φ_G, source φ_S and channel φ_C. (b) Potential profile along the tunneling junction obtained from TCAD simulation showing the shortest tunneling width L_{TW} between the source at potential φ_S and the point where the surface potential equals $(\varphi_S - E_G/q)$.

decay length L_d, as shown in Fig. 3(b). This potential profile ensures that the shortest tunneling barrier width L_{TW} lies along the source-channel direction and is determined by the point where the surface potential falls by $\sim E_G/q$ below the source potential φ_S. From Eq. (2), we further obtain

$$x(\varphi_t) = L_d \times arccosh\left(\frac{\varphi_t - \varphi_G}{\varphi_C - \varphi_G}\right) \tag{3}$$

such that

$$L_{TW} = x(\varphi_S) - x\left(\varphi_S - \frac{E_G}{q}\right) = L_d \times \left[arccosh\left(\frac{\varphi_S - \varphi_G}{\varphi_C - \varphi_G}\right) - arccosh\left(\frac{\varphi_S - \frac{E_G}{q} - \varphi_G}{\varphi_C - \varphi_G}\right)\right]. \tag{4}$$

Equation (4) can be converted to a more straightforward form,

$$L_{TW} = L_d \times \ln\left[\frac{(\varphi_S - \varphi_G) + \sqrt{(\varphi_S - \varphi_G)^2 - (\varphi_C - \varphi_G)^2}}{\left(\varphi_S - \varphi_G - \frac{E_G}{q}\right) + \sqrt{\left(\varphi_S - \varphi_G - \frac{E_G}{q}\right)^2 - (\varphi_C - \varphi_G)^2}}\right]. \tag{5}$$

From Eq. (5), we can find the average electric field along the shortest tunneling barrier, $E_{TW} \sim E_G/qL_{TW}$, and then substitute E_{TW} into the Kane model expression for the interband tunneling current,[11] yielding

$$I_D = A_K \times E_{TW}^2 \times \exp\left(-\frac{B_K}{E_{TW}}\right) \quad \text{with} \quad E_{TW} = \frac{E_G}{q \times L_{TW}} = \frac{E_G}{q} \times \frac{1}{L_d \times \ln\left[\frac{(\varphi_S - \varphi_G) + \sqrt{(\varphi_S - \varphi_G)^2 - (\varphi_C - \varphi_G)^2}}{\left(\varphi_S - \varphi_G - \frac{E_G}{q}\right) + \sqrt{\left(\varphi_S - \varphi_G - \frac{E_G}{q}\right)^2 - (\varphi_C - \varphi_G)^2}}\right]}, \tag{6}$$

where A_K and B_K are tunneling parameters determined by the bandgap and mass of the channel carriers. The parameter A_K also includes the effective tunneling volume with unit channel width, but it is the B_K parameter in the exponential that dominates the predicted values of I_D.

B. Low current simplification and the two working regimes of a TFET

Combining Eq. (6) with the MOSFET equation, both the φ_C and I_D of TFET can be obtained. Due to the nonlinearity of the equations, in the general case they must be solved numerically. However, if the overall TFET current is much lower than that of its MOSFET component (the PMOSFET of Fig. 1(b) with $V_C = 0$), the channel potential φ_C can be simplified by ignoring the potential drop along the channel. In this case, the φ_C in both linear and saturation regimes of the MOSFET component can be expressed as

$$\varphi_C = V_D + V_{biC} \quad \text{if} \quad |V_D| < |V_G - V_{Th}| \text{ (linear region)}$$
$$\varphi_C = V_G - V_{Th} + V_{biC} \quad \text{if} \quad |V_D| > |V_G - V_{Th}| \text{ (saturation region)}, \tag{7}$$

where V_{biC} is the channel built-in potential and V_{Th} is the threshold voltage of the MOSFET component.[23] This assumption is reasonable for all experimental devices reported to date, since even the best experimental TFETs have I_{ON} about 3 decades lower than MOSFETs built in the same technology.[3] Substituting Eq. (7) into Eq. (6), an analytical expression for $I_D(V_G, V_D)$ in a TFET is obtained.

As indicated in Eq. (7), V_C increases linearly with V_D in the linear regime of the MOSFET and thus the I_D of the

GTD depends both on V_G and V_D, according to Eq. (6). In the saturation regime of the MOSFET, V_C only depends on V_G and thus the tunneling current is independent of V_D. Note that the $|V_{Tth}|$ of the MOSFET component in the model is slightly larger than the threshold voltage of a standalone MOSFET with $V_C = 0$ (grounded source). This is most easily seen by noting that the non-zero V_C is equivalent to an opposite back gate bias ($V_B = -V_C$) on MOSFET component, so that the interchannel coupling effect increases the $|V_{Tth}|$.[24]

In Sec. III, we will verify our model against both TCAD and experimental results measured on Si TFETs fabricated in an FD-SOI process.

III. MODEL VALIDATION

The reliability of the model proposed in Eqs. (6) and (7) is verified from two aspects. First, the potential expressed by Eq. (2) around the tunneling junction with φ_C determined by Eq. (7) is examined by tracking the surface potential via TCAD simulation. Next, the model is used to quantitatively fit the experimental results with extracted tunneling parameters.

A. Potential profile tracking

The surface potential is the basis for calculating tunneling current and should be determined as accurately as possible. For verifying the reliability of the potential, TCAD simulations are used to obtain the surface potential around tunneling junction and compared with the expression given by Eq. (2) for TFETs with a normal Si tunneling rate. Combining Eqs. (2) and (7) we obtain

$$\varphi_t(x) = (\varphi_C - \varphi_G) \times cosh\left(\frac{x}{L_d}\right) + \varphi_G \text{ with}$$
$$L_d = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} \times T_{ox} \times T_{si}} \text{ and}$$
$$\varphi_C = V_D + V_{biC} \quad \text{if} \quad |V_D| < |V_G - V_{Tth}|$$
$$\varphi_C = V_G - V_{Tth} + V_{biC} \quad \text{if} \quad |V_D| > |V_G - V_{Tth}|. \quad (8)$$

We verified the predicted potential profile of Eq. (8) with TCAD simulations on a simplified model PTFET structure with various T_{ox} and T_{si}. The source and drain have a doping concentration of 1×10^{21} cm^{-3} to avoid depletion. The channel is taken as intrinsic with a length of 200 nm. For simplicity, the channel built-in potential V_{biC} in Eq. (8) is taken as –0.6 V in all cases.

Figure 4 compares the surface potential profile of the tunneling junction from TCAD simulation (dots) to that described by Eq. (8) (curves) for TFETs under different biasing with several values of T_{ox} and T_{si}. Figure 4(a) shows the tracking results as V_D is fixed at –2 V with V_G swept from –1 to –4 V, from saturation to linear regime. This model device has an SOI structure with 1 nm SiO_2 and 5 nm thick Si channel, at the limits of modern fabrication.[25] The tracking by the model is accurate and reasonable. In the saturation region, as V_G decreases from –1 to –2 V, the channel potential follows the V_G. However, as V_G decreases below –3 V, the channel potential (φ_C) is pinned by the fixed V_D, because the device

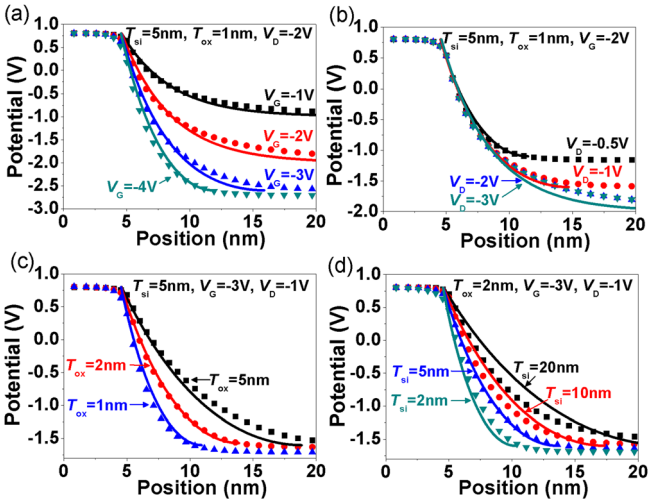

FIG. 4. (Color online) Comparison of the surface potential profile at tunneling junction between TCAD simulation (dots) and the model (curves). The simulated device has the same simplified structure as in Fig. 2. (a, b) The model TFETs have $T_{ox} = 1$ nm and $T_{si} = 5$ nm, with biasing (a) $V_D = -2$ V with V_G swept from –1 V to –4 V and (b) $V_G = -2$ V with V_D swept from –0.5 V to –3 V. (c, d) The TFETs are biased at $V_D = -1$ V and $V_G = -3$ V, with different structures: (c) $T_{si} = 5$ nm with T_{ox} varying from 5 nm to 1 nm and (d) $T_{ox} = 2$ nm with T_{si} varying from 20 nm to 2 nm. The model can explain the effect of T_{ox} and T_{si} reasonably well, except for relatively thick T_{si}.

is now in the linear regime. Similar results can be observed for the situation with fixed V_G and swept V_D, as shown in Fig. 4(b).

The structural parameters T_{ox} and T_{si} can strongly affect the potential profile through changing L_d in Eq. (8). As the T_{ox} decreases from 5 nm to 1 nm with a constant T_{si} of 5 nm, the surface potential decays faster, which is accurately reproduced by our model, as shown in Fig. 4(c) for simulations with biasing fixed at $V_D = -1$ V and $V_G = -3$ V. The influence of the T_{si} for fixed T_{ox} is also accurately reproduced until T_{Si} increases over 10 nm, at which point our model overestimates the change in the potential, see Fig. 4(d). This discrepancy is due to the polynomial approximation for the 2D potential becoming less reliable at large T_{si}.[19,26] Since the trend for SOI technology is toward thinner T_{si}, this is not a major problem for our model.

B. Quantitative fitting of experimental results

Having verified the model's ability of accurately track TCAD-simulated potential profiles in simplified TFET structures, we have further verified our model by quantitatively fitting the tunneling current from experimental results on TFETs fabricated in a standard FD-SOI process.[2,23] Two different gate oxides, HfO_2 and SiO_2, with equivalent gate oxide thickness (EOT) of 2.2 nm and 6 nm were used, with 140 nm buried oxide for all devices. The silicon channel thickness was $T_{si} = 20$ nm and gate length was 400 nm. For quantitative fitting of the experimental results, our model requires three parameters: V_{Tth} and the tunneling parameters, A_K and B_K.

In a TFET with low I_D, the threshold voltage V_{Tth} cannot be extracted from the I_D-V_G curve as in a MOSFET. Instead, we extract V_{Tth} from the I_D-V_D curves by considering the

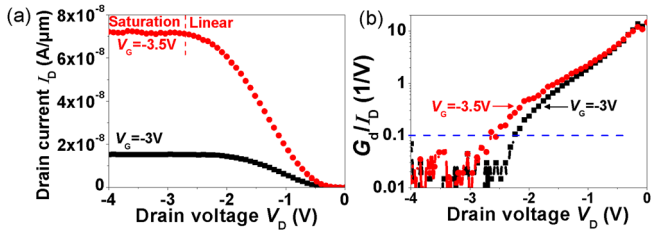

FIG. 5. (Color online) (a) Experimental I_D-V_D PTFET curves *vs.* V_G, showing two distinct working regimes. In the linear regime, I_D changes with V_D, whereas in the saturation regime I_D is unaffected by V_D. (b) The relative output conductance $G_{RD} \equiv G_d/I_D$ where G_d is the output conductance $\partial I_D/\partial V_D$. The constant value of $G_d/I_D = 0.1\,V^{-1}$ is taken as the criterion to extract/define the saturation threshold.

current saturation as a function of V_D. Figure 5(a) shows an experimental I_D-V_D curve of a PTFET with HfO_2 gate oxide. As V_D increases, the device transitions from linear to saturation regime, with I_D becoming independent of V_D. The extraction of V_{Tth} proceeds from the relative output conductance expressed by $G_{RD} = G_d/I_D$, where $G_d \equiv \partial I_D/\partial V_D$ is the output conductance. As V_D increases to $V_{Dsat} = V_G - V_{Tth}$, we extract V_{Tth} from the point where G_{RD} falls below 0.1, as shown in Fig. 5(b).

Next, the tunneling parameters, A_K and B_K, are extracted from the I_D-V_G curve under a fixed V_D. Figure 6(a) shows the I_D-V_G curves of two PTFETs with HfO_2 and SiO_2 gate oxides at $V_D = -2$ and -5 V, respectively. The HfO_2-based device has larger I_{ON} and smaller subthreshold swing (i.e., steeper slope) due to the stronger gate controllability. Taking the logarithm of Eq. (6),

$$\ln\left(I_D/E_{TW}^2\right) = \ln(A_K) - B_K/E_{TW} \tag{9}$$

A_K and B_K are extracted from the slope and intercept of the linear section of the curve shown in Fig. 6(b).

The extracted B_K values are around 23 MV/cm for both TFETs with different gate oxides, in agreement with other reports on interband tunneling in Si.[20,21] Substituting these values into Eqs. (6) and (7), the tunneling current under different V_G and V_D can be computed. Figure 7 shows the fit between our model (curves) and the experimental data (dots) from a HfO_2 TFET (similarly good fits of TFETs with SiO_2 gate oxide are obtained, see Ref. 23). The agreement between model and experimental results is good over a large V_G and V_D range. The model does slightly overestimate I_D in

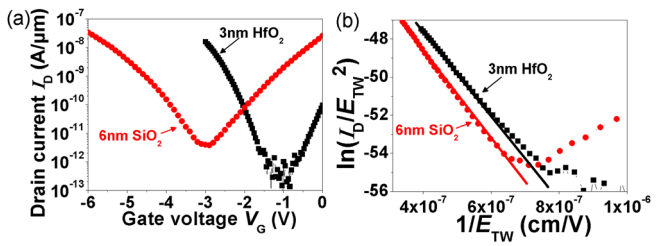

FIG. 6. (Color online) (a) I_D-V_D curves of SOI TFETs with different gate oxides of 3 nm HfO_2 and 6 nm SiO_2 biased at $V_D = -2$ V and -5 V, respectively. (b) The corresponding linear regions of $\ln(I_D/E_{TW}^2)$ *vs.* E_{TW}^{-1} curves. The tunneling parameters of A_K and B_K can be extracted from the slope and intercept for subsequent quantitative fitting.

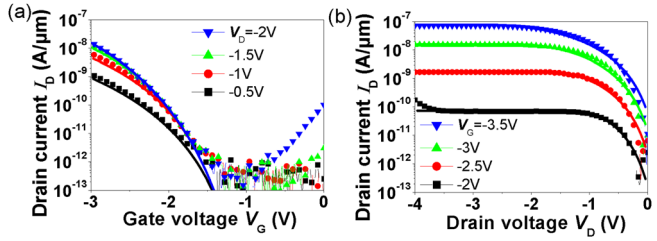

FIG. 7. (Color online) Quantitative model fits (curves) of the experimental results (dots) of (a) I_D-V_G and (b) I_D-V_D characteristics of SOI TFET with 3 nm HfO_2 gate oxides. The fits are accurate except for I_D-V_D curves at low V_D, where the model slightly overestimates the tunneling current.

the region of very small V_D and high V_G only, see Fig. 7(b). We attribute this to the fact that the tunneling model in Eq. (6) takes the parameter A_K and hence the tunneling volume to be a constant. For TFETs with small L_d, the electric field is very high under high V_G, but at low V_D the effective tunneling volume is small.

In Fig. 8, the same fitting method is used for a PTFET with the same HfO_2 gate oxide but $Si_{0.65}Ge_{0.35}$ channel material, resulting in higher I_D. The extracted B_K value is 19 MV/cm, which is almost 4 MV/cm lower than for a Si TFET. As shown in Fig. 8(a), the current is dominated by trap assisted tunneling (TAT) at low V_G, where the current increases slower than at high V_G,[27] but at higher V_G band-to-band tunneling (BTBT) takes over and the data can be well fit by the model (solid lines). The overestimation of the I_D at low V_D is somewhat worse than in Si TFETs due to the lower B_K value of $Si_{0.65}Ge_{0.35}$, as shown in Fig. 8(b).

IV. EXTENSION TO MULTI-GATE DEVICES AND PERFORMANCE PREDICTION

The model can be used for multi-gate devices with a slight change in the definition of the decay length L_d, which has the same meaning as the natural length in a MOSFET.[28] The expressions of L_d for Double-Gate (DG) and Gate-All-Around (GAA) structures have been derived as[29,30]

$$L_d = \sqrt{\frac{\varepsilon_{si}}{2 \times \varepsilon_{ox}} \times T_{ox} \times T_{si}} \quad \text{for} \quad \text{DG and}$$

$$L_d = \sqrt{\frac{2 \times \varepsilon_{si} \times T_{si}^2 \times \ln(1 + \frac{2 \times T_{ox}}{T_{si}}) + \varepsilon_{ox} \times T_{si}^2}{16 \times \varepsilon_{ox}}} \quad \text{for} \quad \text{GAA}. \tag{10}$$

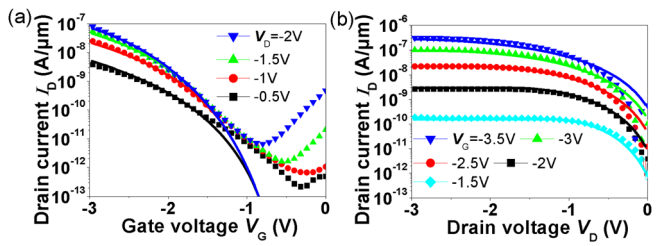

FIG. 8. (Color online) Quantitative model fits (plain lines) of experimental results (symbols) of (a) I_D-V_G and (b) I_D-V_D curves of $Si_{0.65}Ge_{0.35}$ TFETs with 3 nm HfO_2 gate oxide. The bandgap of $Si_{0.65}Ge_{0.35}$ is taken to be 0.98 eV, corresponding to unstrained SiGe. The overestimation of tunneling current is somewhat worse in the low V_D region compared to the SOI TFET.

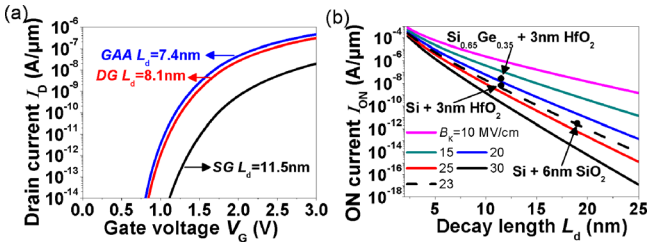

FIG. 9. (Color online) (a) The effect of using a multi-gate TFET structure predicted by the model. The SOI TFET has T_{ox} of 2.2 nm and T_{si} of 20 nm which is the same as the experimental device. The predicted enhancement of I_{ON} by using DG or gate-all-around (GAA) structure is apparent compared to the single gate (SG) TFET. (b) Prediction of the I_{ON} defined at $|V_D| = 1$ V and $|V_G| = 3$ V for TFETs with different L_d and B_K values. The three dots represent the experimental results showing good match in the prediction map.

Figure 9(a) compares the performance predicted by the model of TFETs with different gate configurations. The T_{ox}, T_{si}, and tunneling parameters are the same as in our experiments. The usage of multi-gate structure can effectively enhance the gate controllability, and thus decrease L_d, leading to a higher tunneling current and lower subthreshold swing.

The performance of TFETs depends on the device geometry (through L_d) and channel material parameters (dominated by the B_K tunneling parameter). Figure 9(b) shows the predicted I_{ON} extracted at $V_G = -3$ V and $V_D = -1$ V for TFETs with different L_d and B_K. As L_d decreases, which can be achieved by decreasing T_{ox} and T_{Si} or using multi-gate structures, the I_{ON} increases almost linearly. A lower B_K value, which indicates the use of a lower bandgap channel material, can also enhance the I_{ON}. The dots in Fig. 9(b) indicate the I_{ON} extracted from our experimental Si and $Si_{0.65}Ge_{0.35}$ PTFETs.

Even though our model quantitatively reproduces experimental results, there are still some problems requiring improvements. For simplicity, the model does not consider the doping depletion and profile in the source region, so that the shortest tunneling distance is assumed to lie along the channel length direction. This slightly overestimates the electric field and thus exaggerates the tunneling current. A simple introduction of a uniform depletion region along channel length direction is possible but results in a slightly more complicated expression.[20] However, in reality, the depletion in source region is much wider near the gate oxide than deep in the channel due to the vertical electric field from the gate, effectively tilting the tunneling direction. Since the technology of fabricating TFETs is moving towards higher source doping and sharper tunnel junctions, this relative weakness of our model is expected to become insignificant.

V. CONCLUSION

In this paper, we have developed a TFET model that includes a series-connected MOSFET limiting the current for TFETs with high interband tunneling rates. Further, for TFETs with low interband tunneling rate, like all experimentally reported devices to date, a compact analytical expression is derived by solving pseudo-2D Poisson equation with the boundary condition (φ_C) defined by the MOSFET component in linear and saturation regimes, respectively. The surface potential of TFETs with different T_{ox} and T_{si} can be well tracked by our model over a large range of V_G and V_D biasing. The tunneling parameter B_K values extracted from I_D-V_G experimental curves, 23 MV/cm and 19 MV/cm for silicon and $Si_{0.65}Ge_{0.35}$ channels, respectively, are in agreement with previously reported results and produce good quantitative match between our model and experimental I_D-V_D and I_D-V_G data. Finally, the model is extended to multi-gate structures by simply modifying the decay length value L_d and predictions are made for the I_{ON} of TFETs with different L_d and B_K. The proposed model is expected to not only quantitatively characterize the TFET with various materials and structures but also provide a guide for the improvement of performance.

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