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Gate-induced drain leakage in FD-SOI devices: What the TFET teaches us about the MOSFET

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ABSTRACT

This paper compares the gate-induced drain leakage (GIDL) in fully-depleted (FD) silicon-on-insulator (SOI) tunneling field effect transistor (TFET) and in standard metal-oxide-semiconductor FET (MOSFET) fabricated in the same process. The measurements show that the MOSFET GIDL current is lower than the GIDL in a TFET with the same junction doping, especially for devices with thick gate oxide and under low drain bias. A model describing lateral band-to-band tunneling (BTBT) is developed for GIDL in the FD-SOI TFET. By combining the model of gate-controllable tunneling diode in series with a field effect diode, we achieve an accurate picture of GIDL in FD-SOI MOSFETs.

1. Introduction

As the conventional MOSFET is scaled down, gate-induced drain leakage (GIDL) current is becoming a critical issue. The competing TFET device, which is of interest due to its potentially lower subthreshold slope and partial immunity to short-channel effects [1–5], also faces the problem of relatively high leakage current due to the parasitic tunneling [2,3].

In bulk MOSFETs, several models for GIDL based on both lateral and vertical BTBT have been proposed by combining the Kane's interband tunneling model with a calculated potential distribution [6–9]. However, there are few studies of GIDL in MOSFETs built in FD-SOI technology [10,11]. Moreover, the analysis and modeling of GIDL in TFETs is urgently required because in TFETs GIDL is often quite significant compared to the I_{ON}.

In this paper, a model considering lateral BTBT at the drain junction is developed for the GIDL in TFETs and then extended to FD-SOI MOSFETs. In the FD-SOI MOSFET model, the gate-controllable tunneling diode (GTD) at the drain is combined with the field effect diode (FED) at the source. Even with the same tunneling junction, the GIDL in MOSFETs is lower than that in TFETs due to the series-connected FED, especially under low drain voltage (V_D). The restriction by the FED component is less important in devices with thinner gate oxide. Moreover, the GIDL in FD-SOI MOSFET shows higher temperature sensitivity than that in TFETs due to the presence of the FED.

2. Device comparison

Fig. 1 compares the GIDL current flow in TFETs and MOSFETs built in the same FD-SOI process. In the TFET, the GIDL current generated by BTBT at the drain junction flows through the channel and into the source. Since the voltage drop in the channel is negligible as long as the BTBT current is low, the TFET can be treated as a single GTD at the drain junction.

In the FD-SOI MOSFET, by contrast, the accumulated channel forms a diode with the source. The BTBT-generated current must turn on this FED, inducing a voltage drop at the channel (V_C). This can reduce the voltage difference between the drain and channel, reducing the lateral BTBT rate at that drain junction accordingly.

We observe this effect experimentally by comparing the GIDL data in MOSFETs and TFETs fabricated in the same FD-SOI process [2,12]. Fig. 2(a) shows the full I_D–V_G curves of a NMOSFET, with GIDL current apparent in the $V_G < 0$ regime; whereas Fig. 2(b) compares the GIDL currents in the NMOSFET and TFET. Both devices have 6 nm SiO_2 gate oxide, gate length $L_G = 350$ nm, silicon body $T_{Si} = 20$ nm, a buried oxide (BOX) thickness of 140 nm, and identical drain implantation parameters. Even with the same GTD component at the drain junction, the GIDL of the TFET is consistently larger than that of the MOSFET, especially at low V_D and high V_G.

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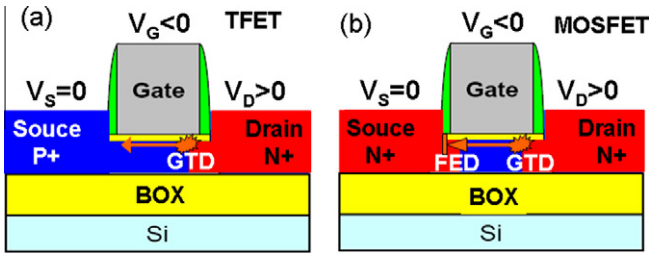

Fig. 1. Comparison of the flow of GIDL current between FD-SOI TFET (a) and MOSFET (b) from the same wafer (T_{Si} = 20 nm, L_G = 350 nm, 6 nm SiO_2 gate oxide).

Thus, the modeling of GIDL in the FD-MOSFET should consider both the effects of GTD and FED.

3. Model derivation

In this work, only lateral BTBT tunneling is discussed, since it explicitly includes the impact of the voltage drop V_C and also becomes physically dominant in FD-SOI devices with thin T_{Si}. A pseudo-2D method is used to derive the surface potential distribution at tunneling junction [10,13,14]. Then, the mean electric field along the shortest tunneling width (E_{TW}) is used in Kane's model [15,16], resulting in the following expression of the tunneling current in GTD [17,18]:

$$I_{GTD} = A_K \cdot E_{TW}^2 \cdot \exp\left(-\frac{B_K}{E_{TW}}\right) \quad \text{with } E_{TW} = \frac{E_G}{q}\frac{1}{L_d \cdot \ln\left[\frac{(\varphi_D-\varphi_G)+\sqrt{(\varphi_D-\varphi_G)^2-(\varphi_C-\varphi_G)^2}}{\left(\varphi_D-\varphi_G-\frac{E_G}{q}\right)+\sqrt{\left(\varphi_D-\varphi_G-\frac{E_G}{q}\right)^2-(\varphi_C-\varphi_G)^2}}\right]} \quad (1)$$

where the A_K and B_K are the tunneling parameters, E_G is the bandgap of the channel material, and $\varphi_G = V_G - V_{FB}$, $\varphi_D = V_D + V_{biD}$, and $\varphi_C = V_C + V_{biC}$ are the gate, drain and channel electrostatic potentials respectively (referenced to the midgap Fermi level E_i in the nominally undoped channel). The channel V_{biC} is determined by gate voltage and can be derived from a simple charge sheet approximation [19].

In FD-SOI MOSFETs, the modeling of GIDL needs to combine both the GTD and FED. In the first approximation, the FED can be modeled as an ideal short-base diode where the doping concentration on the channel side is controlled by the gate voltage [20].

$$I_{FED} = qT_{Si}(D_p n_p/L_E + D_n p_n/L_G)[\exp(qV_C/kT) - 1] \quad \text{with } n_p = n_i \exp(qV_{biC}/kT) \quad (2)$$

where D_p and D_n are the diffusion coefficient of holes and electrons in source and channel respectively, L_E is the effective hole diffusion length at the source, and kT is the temperature. The original minority carrier density in source (p_n) is determined by the source doping concentration, whereas the equivalent electron density in channel (n_p) is controlled by V_G through the change of V_{biC}.

4. Model verification

The validity of the model is examined by comparing with the experimental results. The tunneling parameters (A_K and B_K) in Eq. (1) are extracted from the I_D–V_G curve of the TFET at V_D = 1.5 V through the linear relation of $\ln(I_D/E_{TW}^2) \sim 1/E_{TW}$. The extracted B_K value is 21.1 MV/cm, which agrees with reported results on phonon-assisted BTBT in silicon [14,15]. Using these values as fitting parameters, we calculated the TFET GIDL current according to Eq. (1) and compared with the experimental results – see Fig. 3(a). The model agrees with experiment over a wide range of V_D and V_G.

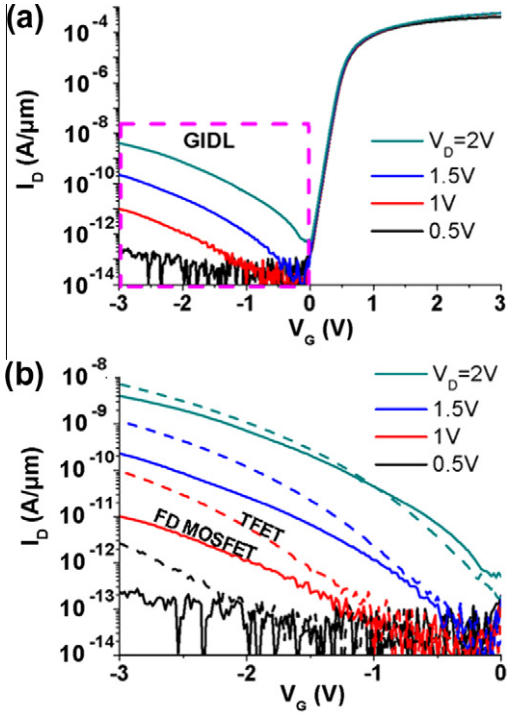

Fig. 2. (a) I_D–V_G curves of an N-type FD-SOI MOSFET under various V_D. (b) Comparison between the SOI TFET current (dashed lines) and the GIDL in MOSFET (solid lines). The devices are fabricated by the same FD-SOI process, and gate length L_G = 350 nm with 6 nm SiO_2 gate oxide.

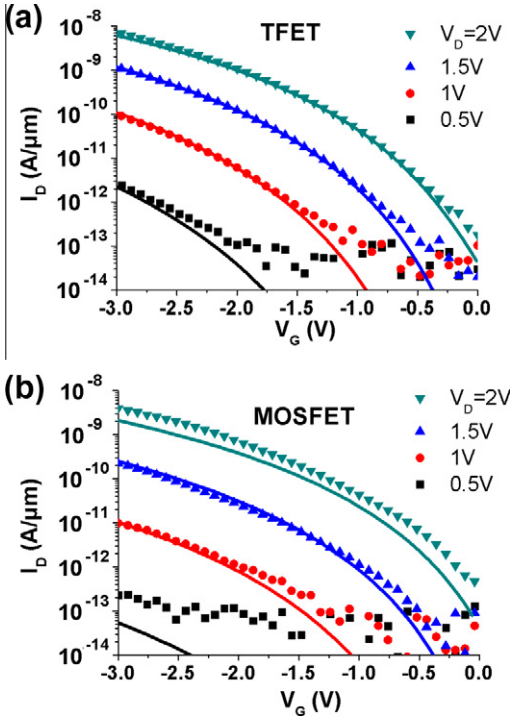

Fig. 3. (a) Fit between the model describing the GTD (lines) and the experimental TFET data (points). (b) Comparison between the proposed model (lines) combining GTD with FED mechanism and the experimental data (points) from the GIDL in FD-SOI MOSFET.

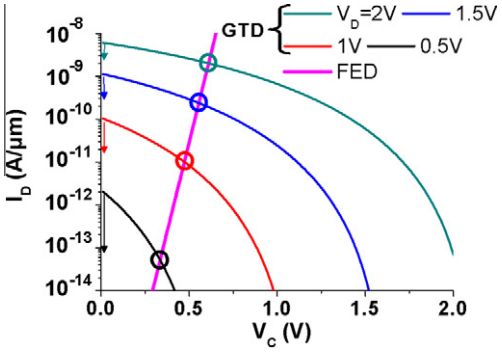

Fig. 4. I_D–V_C curves from GTD component of FD-SOI MOSFET as a function of V_D. Combining with the FED component, the current I_D in FD-SOI MOSFET is obtained at the crossing point. At lower V_D, the I_D decreases more rapidly as V_C increases and thus becomes much smaller than in a SOI TFET with the same fabrication parameters.

Using the tunneling parameters extracted from the TFET, the GIDL of an FD-SOI MOSFET is calculated by combining Eqs. (1) and (2) and solving them numerically. Fig. 3(b) compares the model (curves) with the experimental data (points), showing good agreement. The reduction of GIDL in a MOSFET compared to a TFET at low V_D bias can be straightforwardly explained by the graphical method illustrated in Fig. 4. The curves in Fig. 4 correspond to the GTD I_D–V_C curves as a function of V_D with fixed $V_G = -3$ V, the straight line corresponds to the I_D–V_C relation of the FED from Eq. (2), and the actual V_C and I_D values of the FD-SOI MOSFET are given by the intersection points, circled in Fig. 4. The GIDL current in the FD-SOI MOSFET is markedly reduced compared to its GTD component due to current continuity through the FED. The reduction occurs even at low V_D, because when V_D is low the I_{GTD} falls more rapidly with the increase in V_C.

The model is also used for analyzing devices fabricated with 3 nm HfO_2 gate oxide. Compared to the 6 nm SiO_2 devices, the GIDL current in MOSFETs is again lower than in TFETs, but the reduction is less pronounced. At $V_D = 2$ V, the GIDL current of the MOSFET is almost the same as the TFET, indicating that the FED has less effect in devices with thinner gate oxide. The fits of our model with the experimental results of the HfO_2 devices are shown in Fig. 5. The MOSFET GIDL current at $V_D = 0.5$ V is somewhat underestimated by the model. This may be due to the fact that the FED current at low I_D is dominated by the recombination component, ignored in Eq. (2), which decreases more slowly with V_C. This hypothesis is consistent with the experimental results, since the HfO_2 gate oxide introduces more traps than SiO_2 gate oxide, enhancing recombination.

5. Discussion

The effect of the FED component in FD-SOI MOSFETs can also impact the temperature dependence behavior of GIDL. Fig. 6 compares this temperature dependence in TFETs and MOSFETs based on the same FD-SOI substrate with 3 nm HfO_2 gate oxide. At room temperature, the MOSFET and TFET GIDL currents are similar, indicating negligible effect from the FED. As T decreases, the TFET current decreases slowly due to the weak temperature dependence of BTBT [2]. On the other hand, the MOSFET GIDL current decreases more rapidly, especially at lower temperature, as shown by the points in Fig. 6. This sensitivity to temperature arises from the stronger temperature dependence of the FED component, which effectively restricts the current flow at low T. A more quantitative analysis of the impact of FED will require an additional examination of both the vertical BTBT tunneling, which is more

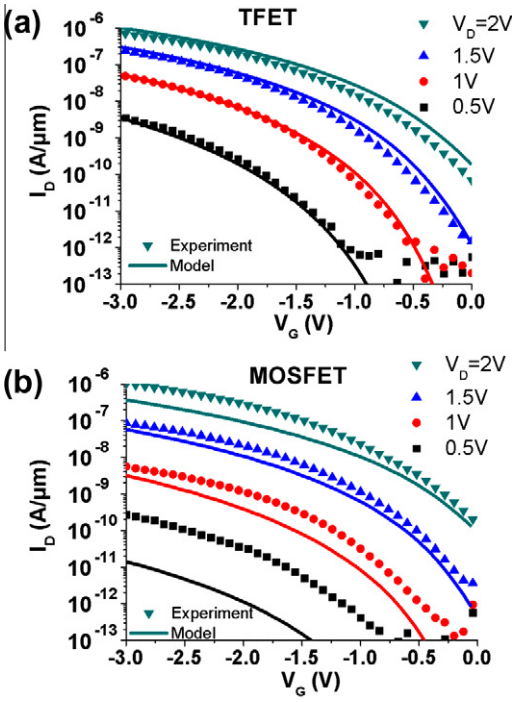

Fig. 5. Fit between model (lines) and the experimental results (points) from (a) SOI TFET and (b) SOI MOSFET with 3 nm HfO_2 gate oxide.

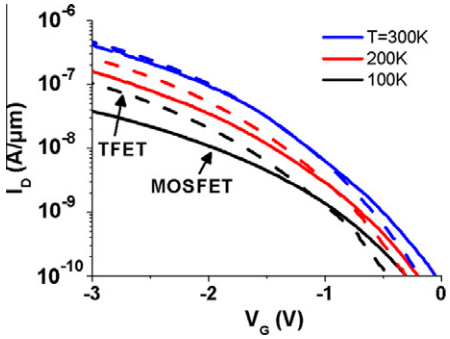

Fig. 6. GIDL current of SOI TFET (dashed lines) and SOI MOSFET (solid lines) with 3 nm HfO_2 gate oxide vs. temperature. The GIDL of TFET is less sensitive to temperature compared to that of FD-MOSFET.

complicated because it is not explicitly determined by the channel potential [6–9], and of the trap-assisted tunneling which is another main source of GIDL [21].

The existence of the FED provides some extra guidelines for reducing GIDL in MOSFETs. The doping concentration in source should be high enough to reduce the minority carrier density and thus the FED current, which argues against using an LDD region in the source. Furthermore, the effective hole diffusion length L_E in the source is determined by the distance between source electrode and the source doping boundary. Normally, it is minimized to reduce the series resistance, but as we have seen it can also enhance the FED current and hence increase the GIDL. Further, the density of traps should be minimized, as they increase not only the tunneling current at drain junction but also the recombination component of I_{FED} at source junction.

6. Conclusion

An analytical model considering the GTD at drain junction is developed for the GIDL in TFETs. Compared with the TFET, we find

that the FD-SOI MOSFET fabricated in the same technology experiences a significant voltage drop on the series diode at source junction, which reduces the voltage drop on the drain junction and hence significantly reduces its GIDL current, especially at low V_D. By combining the expressions of GTD and FED, a composite model is proposed for the GIDL in FD-SOI MOSFETs. Both the models for TFET and MOSFET show good agreement with the experimental results from devices with different gate oxides. Finally, the low temperature test is performed to confirm the current restriction effect of the FED.

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