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Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling

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ABSTRACT

We report on thin-body tunneling field-effect transistors (TFETs) built on SOI substrates with both SiO_2 and HfO_2 gate dielectrics. The source–drain leakage current is suppressed by the introduction of an intrinsic region adjacent to the drain, reducing the electric field at the tunnel junction in the off state. We also investigate the temperature dependence of the TFET characteristics and demonstrate that the temperature-induced change in the Si bandgap is the main mechanism that determines the tunneling barrier and hence the drain current I_D. We present a model of the TFET as a combination of a gated diode and a MOSFET, which can be solved analytically and can predict the experimentally measured I_D over a wide range of drain and gate bias. Finally we report on the low frequency noise (LFN) behavior of TFETs, which unlike conventional MOSFETs exhibits $1/f^2$ frequency dependence even for large gate areas. This dependence indicates less trapping due to the much smaller effective gate length over the tunneling junction.

1. Introduction

As the scaling of conventional CMOS devices is hampered by short-channel effects (SCEs), silicon-compatible devices based on different principles are being studied for their unique properties. In particular, the tunneling field effect transistor (TFET) [1] is of interest due to its complete semiconductor process compatibility and similarity of device layout with the Si MOSFET. The current in TFETs is carried by band-to-band tunneling (BTBT), which makes it theoretically possible to reach extremely low off-state currents (I_{OFF}) as well as an ultra-low subthreshold slope (S) below the ideal MOSFET value of 60 mV/decade at room temperature. A number of studies have focused on power consumption in TFETs, reporting a theoretical advantage over standard MOSFETs [2,3]. In order to enhance the on-state current (I_{ON}), multigate [4] and lower bandgap semiconductors, such as Ge and SiGe, have been reported [5–9]. At the same time, experimentally realized TFETs have typically suffered from difficulties in simultaneously achieving low S and high I_{ON}, as well as from high source–drain leakage current (I_{LEAK}) due to ambipolar conduction, especially for low bandgap semiconductors.

In addition to experimental demonstrations, analytical TFET models are important for understanding device physics (including BTBT and leakage effects) and quick prediction of device performance [10–12]. In previously reported models, the channel was assumed to be fully depleted, which suppresses [11] or minimizes [12] the effect of drain voltage V_D on the tunneling junction, especially at high gate voltage V_{GS} in long-channel TFETs. Furthermore, ignoring the carrier transport in the channel also removes the current saturation mechanism of future TFETs with higher I_{ON}.

In this work, we focus on several aspects of Si TFETs. First, we compare TFETs with SiO_2 and HfO_2 gate dielectrics to demonstrate lower S and higher I_{ON} in devices with thinner equivalent oxide thickness (EOT). Second, an asymmetrical TFET layout with an intrinsic region (L_{IN}) at drain side is demonstrated to effectively suppress I_{LEAK} while retaining the same I_{ON}. These experimental results are confirmed using device and process simulations based on Silvaco TCAD. Third, temperature variation tests are performed to examine the validity of Kane's model [13] of the BTBT process. Further, an analytical model of TFET including a MOSFET channel component is proposed. While this model requires numerical evaluation over the entire range of bias and current, it reduces to a compact and convenient form for our experimental TFETs with relatively low I_{ON}. Finally, we present low-frequency noise (LFN) measurements on TFETs and qualitatively explain the different LFN properties of TFETs compared to standard MOSFETs (where LFN measurements are widely used to extract trap properties [14,15]).

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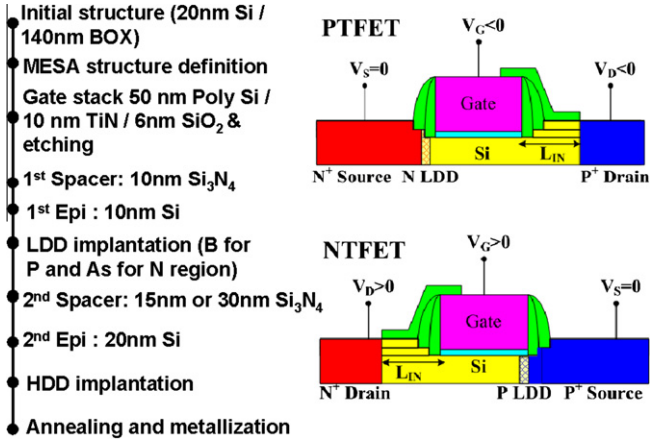

Fig. 1. Fabrication process flow and bias polarity of TFETs. In PTFET, the gate is negatively biased and the BTBT occurs at the n+ doped source. Conversely, in NTFET, the gate is positively biased and the BTBT occurs at the p+ doped source.

2. Fabrication and device structure

2.1. Fabrication process

Our TFET fabrication sequence is completely compatible with fully depleted SOI CMOS process flow. The process started from an SOI Unibond substrate with 140 nm BOX and 20 nm active Si layer. The isolated device active areas (mesa structure) were formed by photolithography and dry etching, followed by the definition of gate stack which is composed of three layers, as illustrated in Fig. 1. Two different gate oxides were formed for comparison: either a 6 nm SiO_2 grown by dry oxidation or a 3 nm ALD-deposited HfO_2. After the deposition of a metal gate (10 nm TiN), 50 nm thick polysilicon was deposited for silicidation. The first spacer was formed by the deposition of 10 nm Si_3N_4 in LPCVD, then a 10 nm Si layer was epitaxially grown by CVD process. The N-type LDD was formed by implantation of As with dose of 1×10^{15} cm^{-2} and energy of 9 keV, while BF_2 implantation with dose of 1×10^{15} cm^{-2} and energy of 7 keV was used for formation of P-type LDD. Then, a second spacer of 15 or 30 nm and a Si layer of 20 nm were deposited. Before the implantation of N-HDD and P-HDD regions, a Si_3N_4 layer was formed to protect the intrinsic region L_{IN}. The dose and energy of As for NHDD implantation were 2×10^{15} cm^{-2} and 20 keV, respectively, whereas, for PHDD implantation, these values were 3×10^{15} cm^{-2} and 5 keV. Rapid thermal annealing (RTA) was used to activate the dopants, followed by the metallization.

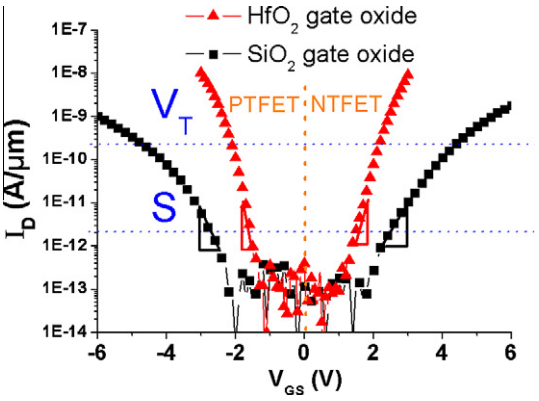

Fig. 3. Measured I_D–V_{GS} curves of both NTFETs and PTFETs based on different gate oxides (L_G = 400 nm, $|V_{DS}|$ = 1 V). The inset symbols show the definitions of V_T and S.

2.2. Device structure

The structure of the fabricated TFETs is quite similar to that of a MOSFET with double spacers and raised S/D, shown in Fig. 2a. The only structural difference between TFETs and MOSFETs lies in the opposite doping of the TFET source and drain. Furthermore, for suppressing the ambipolar current, the structure of some TFETs was rendered asymmetrical by adding an intrinsic region L_{IN} separating the drain contact from the channel as shown in Fig. 2b.

For simplicity, the N+ region in a PTFET is defined as source while the P+ region is defined as drain. The opposite definition applies to NTFETs, as shown in Fig. 1. The source of both PTFETs and NTFETs is always grounded, while the drain is negatively biased in PTFETs and positively biased in NTFETs. The I_{ON} is produced by tunneling at the source-channel junction at $V_{GS} < 0$ for PTFETs and $V_{GS} > 0$ for NTFETs.

3. Electrical characterization and analysis

The fabricated devices were systematically characterized. From C–V measurements, the EOT values of TFETs with 6 nm SiO_2 and 3 nm HfO_2 gate oxides were 6 nm and 2.2 nm, respectively. The gate width of all TFETs was 10 μm, the gate length L_G varied from 100 to 400 nm, and the intrinsic region length L_{IN} varied from 0 to 100 nm.

3.1. Impact of gate oxide on characteristics

A comparison of I_D–V_{GS} curves of NTFETs and PTFETs with different gate oxides and L_G = 400 nm and $|V_D|$ = 1 V is shown in

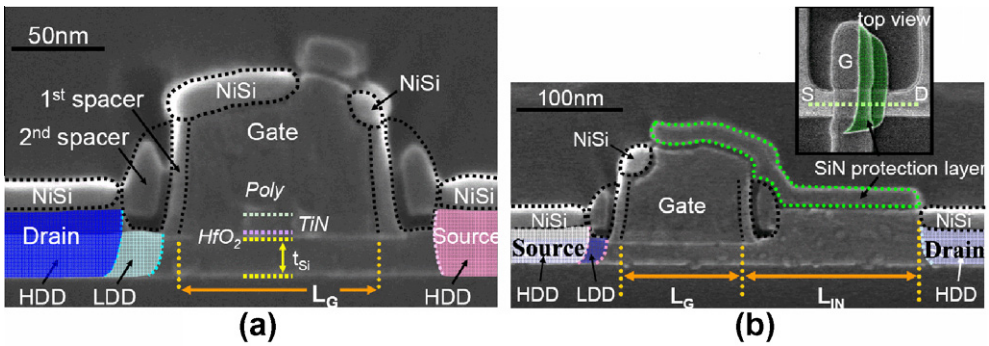

Fig. 2. SEM images of fabricated conventional (a) and asymmetric (b) TFETs.

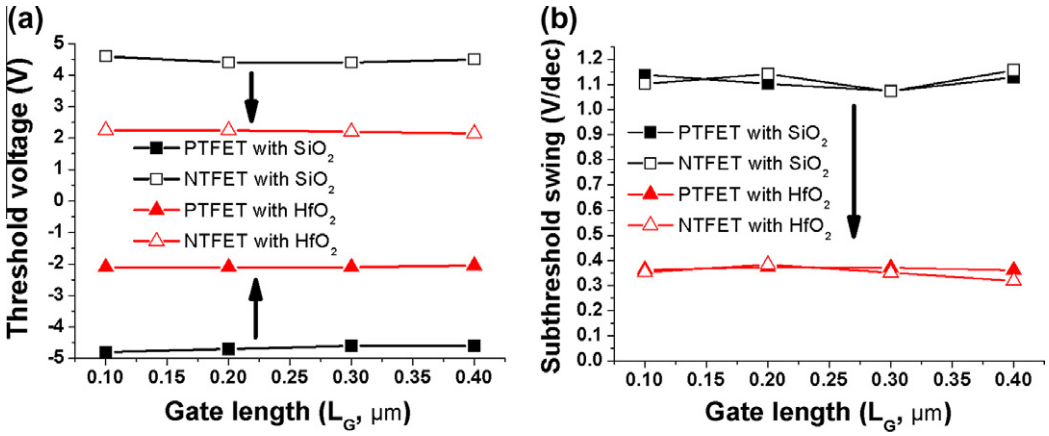

Fig. 4. Comparison of V_T (a) and S (b) values of the TFETs with different gate oxide and gate length.

Fig. 3. In TFETs, there exists no unambiguous definition of threshold voltage V_T and S is not a constant value. For comparison purposes, we define the V_T as the voltage when I_D equals 2×10^{-10} A/μm and extract the S value when I_D reaches 2×10^{-12} A/μm, ranging over two decades in drain current. As can be easily observed in Fig. 3, TFETs with HfO_2 gate oxide have smaller V_T and higher I_{ON} than those based on SiO_2. The S values are also markedly reduced.

As described in Fig. 4, the results on devices with different L_G = 100–400 nm show that V_T and S are independent of L_G. This is due to the fact that at low I_D the tunneling current is determined by the maximum electric field at the tunneling junction and unaffected by the carrier transport in the channel [16]. Fig. 4a shows that V_T is 4.5 V for both NTFETs and PTFETs with SiO_2, whereas V_T is 2.3 V for those with HfO_2 gate oxide. As for the S value, shown in Fig. 4b, both NTFETs and PTFETs with SiO_2 have $S \sim 1.1$ V/decade, which is reduced to 0.33 V/decade in devices with HfO_2. We note that one wafer (with HfO_2 gate oxide) from this lot yielded remarkably low S [5] for reasons that are still under investigation. Here, we only focus on a comparison of identically processed devices with different dielectrics.

The comparison reveals that thinner EOT can lead to lower V_T and S values due to the better electrostatic controllability from the gate. The theoretically achievable $S < 60$ mV/decade value in TFETs requires excellent electrostatic control of the maximum junction field, which implies minimizing gate EOT and sharpening the S/D lateral doping profile. As a result, the experimental reports of low S published thus far [5,7,17] have generally suffered from low I_{ON}, at least for reasonable V_D values.

3.2. Impact of device architecture on characteristics

A potential problem of symmetrical TFETs is the large I_{LEAK} under opposite gate bias, because interband tunneling can occur at either the source-channel or the drain-channel junction depending on the sign of V_{GS}. This ambipolar I_{LEAK} can be more severe for TFETs based on low bandgap semiconductors, such as Ge. The solution is to introduce an asymmetrical architecture, such as unequal source/drain doping [7,18], intrinsic regions and lateral heterojunctions [7,9].

Among these solutions, the introduction of intrinsic region is the simplest, requiring an easy change in the photomask, as shown in the inset of Fig. 2b. This method was originally proposed in a simulation paper [19]; the first experimental data have been presented in [5]. Here, we present a systematic study by the combination of simulation and experiment. We also demonstrate the possibility of completely suppressing the ambipolar I_{LEAK}. Fig. 5

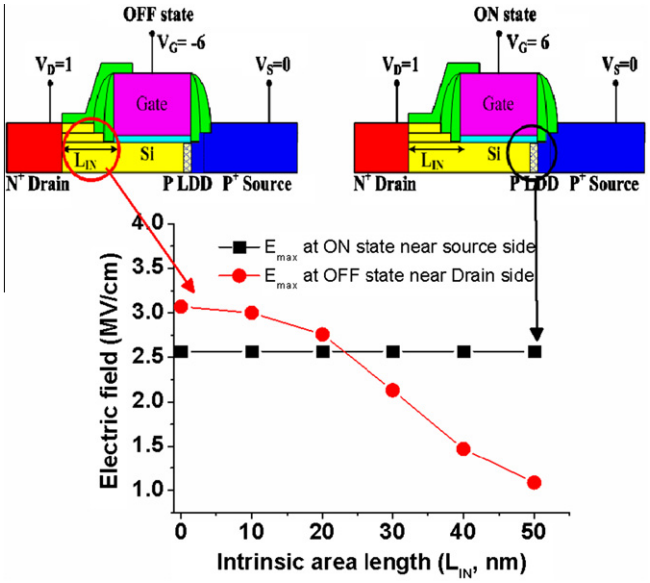

Fig. 5. The maximum electric field (E_{max}) at the tunneling junction of a NTFET with different L_{IN} under positive gate bias and negative gate bias.

shows a NTFET with intrinsic region operated under different V_{GS} and its corresponding simulated maximum electric field (E_{max}) at the tunneling junction. Under positive gate bias, the TFET is in the ON state and the tunneling occurs at source side. The E_{max} at the source side is almost constant as L_{IN} increases due to the negligible potential drop on L_{IN} region, see Fig. 5.

In contrast, as the gate is negatively biased, the TFET is in OFF state and the tunneling occurs at drain side where the intrinsic area is located. For the TFET with L_{IN} smaller than 20 nm, the E_{max} in the off state is even slightly larger than in the ON state, see Fig. 5. However, as L_{IN} increases beyond 20 nm, the E_{max} at the drain side falls quickly. Since the BTBT rate is exponentially dependent on E_{max}, it can be suppressed at the drain side by increasing L_{IN}. However, at the source side, the E_{max} does not change, so L_{IN} does not degrade I_{ON}.

A comparison of the simulated and experimental results for an NTFET with different values of L_{IN} is shown in Fig. 6, where the simulated tunneling current in Fig. 6a is obtained from Kane's model as discussed below. As expected, the simulated I_{LEAK} of the NTFET with $L_{IN} \leqslant 20$ nm is comparable to the I_{ON} due to the large E_{max}, but it can be markedly suppressed by increasing L_{IN} to 50 nm.

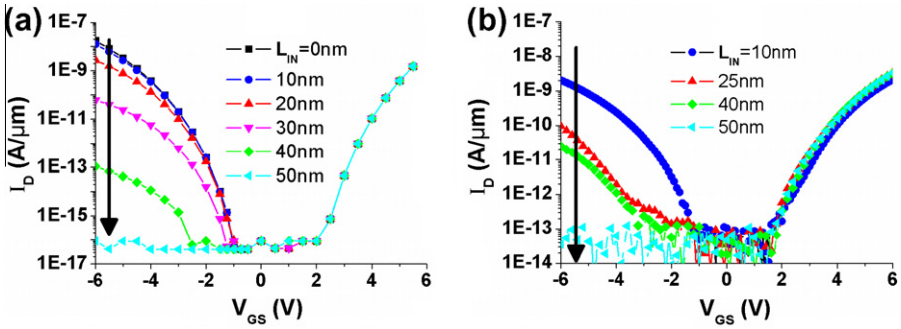

Fig. 6. I_D–V_{GS} curves of NTFETs with SiO_2 gate oxide and different L_{IN} at V_{DS} = 1 V from simulation (a) and experiment (b), all devices have L_G = 400 nm.

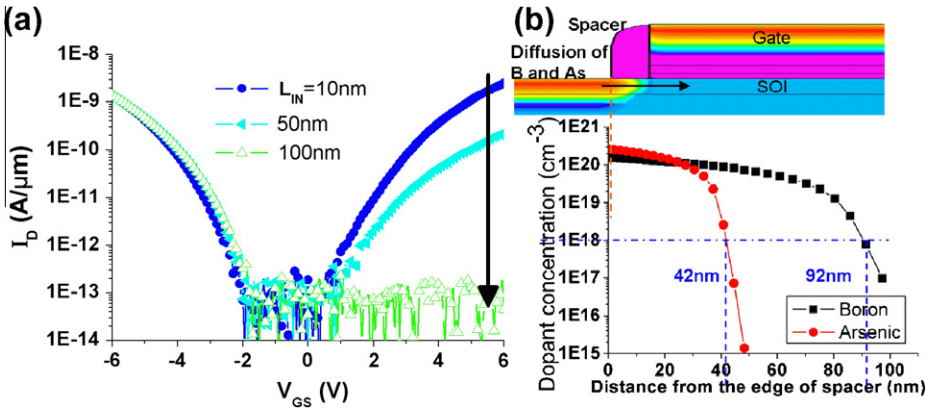

Fig. 7. I_D–V_{GS} curve of PTFETs with SiO_2 gate oxide and different L_{IN} (a) and the simulation of the lateral diffusion profiles of boron and arsenic dopants (b). The dotted line indicates the boundary for suppressing the tunneling current.

Fig. 6b shows the experimental results for NTFETs with four different L_{IN} from 0 to 50 nm. Again, in agreement with the simulation, the I_{LEAK} of the TFETs without L_{IN} is comparable to I_{ON}, but can be effectively suppressed by increasing L_{IN} to 50 nm.

In PTFETs, the I_{ON} is also unaffected by L_{IN}, as can be seen in Fig. 7a. However, the full suppression of I_{LEAK} in PTFETs requires a larger L_{IN} = 100 nm. We attribute this difference to the different diffusion coefficients of boron (B) and arsenic (As) in Si. Fig. 7b shows the simulated doping profiles of implanted B and As after the activation anneal. All parameters in simulation were adjusted according to the fabrication process. As previous work indicates [14], a doping concentration which is lower than $1 \times 10^{18}\ cm^{-3}$ can be used to effectively suppress the tunneling. In our case, the I_{LEAK} results from the tunneling at drain side which is doped by As and B in NTFETs and PTFETs, respectively. The characteristic diffusion distance from the edge of spacer to the $10^{18}\ cm^{-3}$ value point is ~40 nm for As and ~90 nm for B, as shown in Fig. 7b, qualitatively explaining our experimental observations.

The same tendency applies to TFETs with HfO_2 gate oxide and smaller EOT. As shown in Fig 8a, the I_{LEAK} of HfO_2 based NTFETs drops rapidly as L_{IN} increases. Note that the residual I_{LEAK} as L_{IN} exceeds 50 nm is caused by gate leakage, which cannot be suppressed by L_{IN}. However, for HfO_2-based PTFETs, L_{IN} as long as 100 nm reduces the I_{LEAK} but cannot completely suppress it, due to both the effects of the longer B diffusion length and stronger gate control of E_{max}, see Fig. 8b.

3.3. Impact of temperature on characteristics

Fig. 9a shows the I_D–V_{GS} of a NTFET with HfO_2 gate oxide, L_G = 400 nm and L_{IN} = 10 nm at temperatures ranging from 77 to 300 K. At low I_D, where the current is dominated by the interband

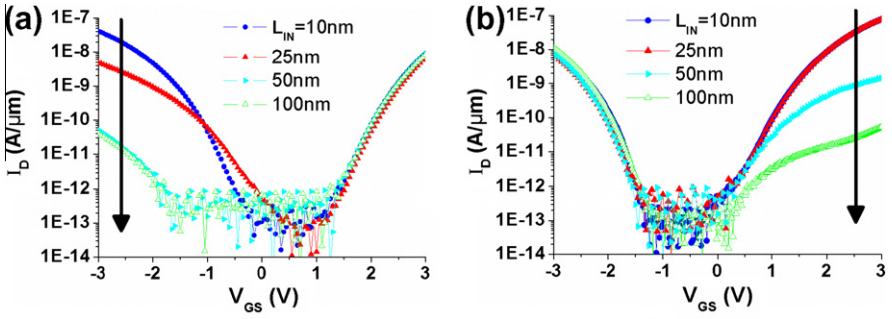

Fig. 8. I_D–V_{GS} curves of NTFETs (a) and PTFETs (b) with HfO_2 gate oxides and different L_{IN}.

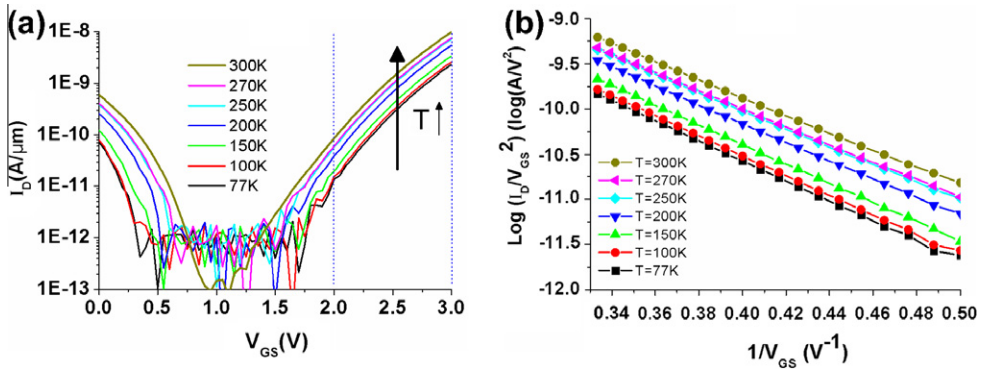

Fig. 9. (a) I_D–V_{GS} characteristics and (b) $\log(I_D/V_{GS}^2) - V_{GS}^{-1}$ curves at V_{DS} = 1 V for an NTFET with L_G = 400 nm as a function of temperature T.

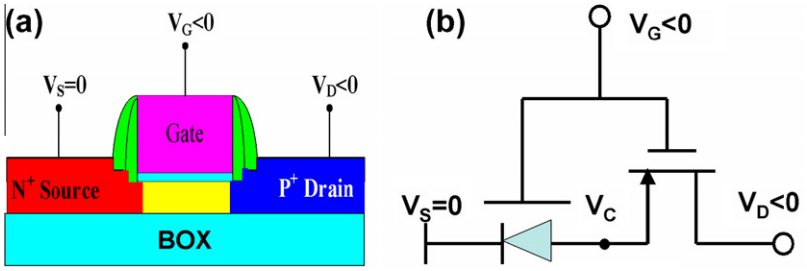

Fig. 10. (a) Schematic view of a TFET operating in P mode with V_{GS} < 0 biased sufficiently low to create a hole inversion channel under the gate. (b) The proposed model of the PTFET as a series combination of a gate-controllable source-channel tunnel diode with a PMOSFET.

tunneling at the source-channel junction, the temperature dependence of the TFET I_D can be qualitatively explained by the Kane tunneling model [13]:

$$I_D = A_K \cdot E_{max}^2 \cdot \exp\left(-\frac{B_K}{E_{max}}\right) \quad \text{with } E_{max} \propto V_{GS} \text{ and } B_K \propto E_G^{\frac{3}{2}} \tag{1}$$

where A_K, B_K are tunneling parameters which depend on the bandgap and carrier effective mass in the channel material. The dominant temperature effect on the TFETs performance comes from the temperature variation of bandgap E_G, which enters in the exponential of Eq. (1). In Si, E_G has weakly negative temperature dependence [20]:

$$E_G(T) = E(0) - \frac{\alpha \cdot T^2}{T + \beta} \tag{2}$$

As temperature increases, the E_G decreases, leading to a corresponding decrease in parameter B_K and hence an increasing tunneling current.

The validity of Kane's model can be examined by rewriting Eq. (1) as:

$$\log\left(\frac{I_D}{V_{GS}^2}\right) \propto -\frac{B_K}{V_{GS}} \tag{3}$$

Fig. 9b confirms the linear relationship between $\log(I_D/V_{GS}^2)$ and $1/V_{GS}$ over the entire temperature range. The slight variation in the slope reflects the increase of the B_K coefficient at low temperature. Since the temperature dependence of TFET I_D agrees with that reported previously [5] and with Eq. (1), we can drawn two main conclusions:

(i) The weak temperature dependence of the drain current I_D confirms that BTBT is the dominant mechanism in TFETs. By contrast, the drain current in MOSFETs is strongly temperature-dependent, mainly due to mobility variation.

(ii) The Kane model is at least qualitatively effective in describing the BTBT process in Si TFETs.

3.4. TFET model combining tunneling junction and channel transport

A schematic picture of a biased PTFET working is shown in Fig. 10a. At sufficiently negative V_{GS}, a hole layer is induced in the channel, creating a reverse-biased tunneling junction between the source and the channel. The tunneling junction is formed at the source side as a reverse biased P–N diode. We can model the resulting device as the series connection of a PMOSFET channel with a gate-controlled tunnel diode at the source-channel junction, as shown in Fig. 10b. The PMOSFET has a well defined V_D at the drain, but its source coincides with the cathode of the tunneling diode and is at a bias V_C determined by current continuity.

Because of the nonlinear equations describing the $I_D(V_{GS},V_D–V_C)$ of the MOSFET and the $I_D(V_{GS},V_C)$ tunneling current of the gated diode, a general solution can only be obtained numerically. However, at the relatively low tunneling I_D observed in our TFETs, we can simplify our model by considering the MOSFET to be either in the linear or the saturation regimes, leading to two possible values of V_C:

$$\begin{aligned} &V_C = V_D \quad \text{if } |V_D| < |V_{GS} - V_{th}| \text{(linear region) or} \\ &V_C = V_{GS} - V_{th} \quad \text{if } |V_D| > |V_{GS} - V_{th}| \text{(saturation region)} \end{aligned} \tag{4}$$

where V_{th} is the threshold voltage of the MOSFET channel (not the same as the V_T of the TFET discussed in Section 2). In linear region of the MOSFET, V_C follows V_D and the tunneling diode current depends both on V_{GS} and V_D. On the other hand, when $|V_D| \geqslant |V_{GS} - V_{th}|$ and the MOSFET is saturated, V_C becomes a function of V_{GS} only and the tunneling current I_D (V_{GS},V_C) becomes independent of V_D.

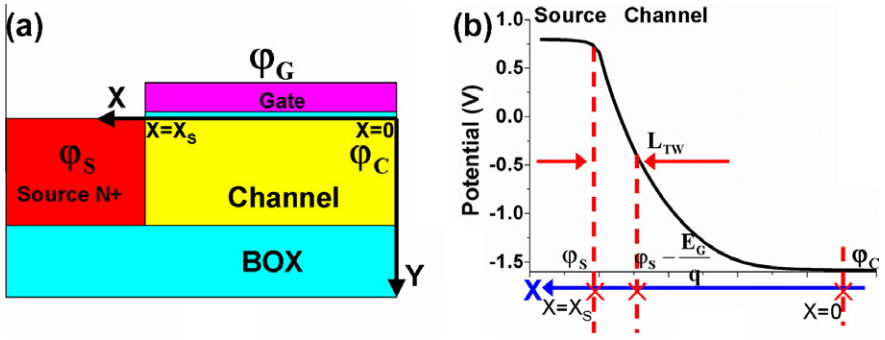

Fig. 11. (a) Schematic view of the tunneling junction in which the potential distribution is decided by the potentials of the gate φ_G, source φ_S and channel φ_C. (b) Potential profile along the tunneling junction obtained from TCAD simulation showing the shortest tunneling width L_{TW} between the source at potential φ_S and the point at the potential $(\varphi_S - E_G/q)$.

We can obtain an expression for $I_D(V_{GS},V_C)$ of the gate-controlled tunneling diode by solving the potential profile around the tunneling junction, shown in Fig. 11a, using the pseudo-2D Poisson equation approach described previously [12,21]. The surface potential along the tunneling direction can be defined in terms of the electrostatic potentials of gate (φ_G), source (φ_S), and channel (φ_C), referenced to the midgap Fermi level E_i in the nominally undoped channel:

$$\varphi_S = \frac{kT}{q}\cdot \ln\left(\frac{N_S}{n_i}\right)$$
$$\varphi_G = V_{GS} + V_{FB} \quad (5)$$
$$\varphi_C = V_C + V_{biC}$$

In Eq. (5), n_i is the carrier concentration of intrinsic channel material, N_S is the source doping concentration, V_{FB} is the flat-band voltage and V_{biC} is the built-in potential of the inverted channel. Generally, in a bulk device V_{biC} equals $2\varphi_B$, where φ_B is Fermi potential (difference between the channel Fermi level and midgap E_i [20]). However, in a lightly doped, fully depleted SOI MOSFETs, V_{biC} has a more complicated form [24].

We find that the surface potential increases almost exponentially from the channel φ_C to source φ_S, as illustrated in Fig. 11b. This potential profile determines that the shortest tunneling barrier width L_{TW} lies along the source-channel direction and is determined by the point where the surface potential falls $\sim E_G/q$ below the source potential φ_S. We can now insert the mean electric field in the tunneling direction E_{TW} along L_{TW} into Eq. (1), as this has been shown to give better accuracy than the local E_{max} [11,22]. The analytical expression of the tunneling current becomes:

$$I_D = A_K\cdot E_{TW}^2\cdot \exp\left(-\frac{B_K}{E_{TW}}\right) \quad \text{with } E_{TW} = \frac{E_G}{q\cdot L_{TW}}$$
$$= \frac{E_G}{q}\frac{1}{L_d\cdot \ln\left[\frac{(\varphi_S-\varphi_G+\sqrt{(\varphi_S-\varphi_G)^2-(\varphi_C-\varphi_G)^2}}{\left(\varphi_S-\varphi_G-\frac{E_G}{q}\right)+\sqrt{\left(\varphi_S-\varphi_G-\frac{E_G}{q}\right)^2-(\varphi_C-\varphi_G)^2}}\right]} \text{ and}$$
$$L_d = \sqrt{\frac{\varepsilon_S}{\varepsilon_{ox}}\cdot T_{ox}\cdot T_s} \quad (6)$$

where L_d is the characteristic decay length of the potential profile [23]. By substituting the Eq. (4) into Eq. (5) to obtain φ_C in the two operating regimes, the tunneling current can be calculated via Eq. (6).

The remaining unknowns are the tunneling parameters A_K and B_K, which are often estimated for a one-dimensional tunneling junction assuming a constant electric field [13]. Instead, we will treat them as fitting parameters extracted from an experimental I_D–V_{GS} curve under a fixed V_D and then used over the entire range of V_{GS} and V_D. For all of our devices, the extracted B_K value is ~24 MV/cm, which is consistent with other reports [12,22]. Fig. 12 shows a comparison between our model (lines) and the experimental results (dots) of a PTFET with 6 nm SiO_2 gate oxide over a wide range of V_{GS} and V_D. The model reproduces measured I_D reasonably well over most of the biasing range, indicating its validity in both the linear and saturation regimes of the TFET channel. The discrepancy at low V_D and V_{GS} in both the I_D–V_{GS} and I_D–V_D characteristics may be due to trap-assisted tunneling that is not captured by Eq. (6). A more detailed discussion of our series-connected diode and MOSFET model, including its extension to other channel materials and device architectures, will be reported separately [25].

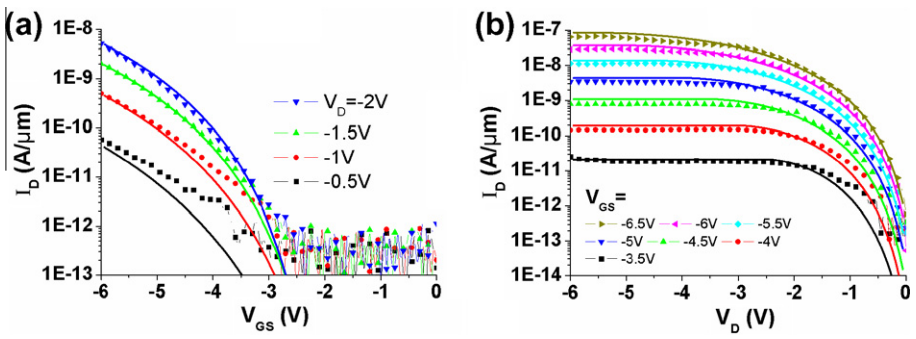

Fig. 12. Quantitative fit between model (lines) and experimental results (dots) of (a) I_D–V_{GS} and (b) I_D–V_D curves of SOI TFET with gate oxides of 6 nm SiO_2.

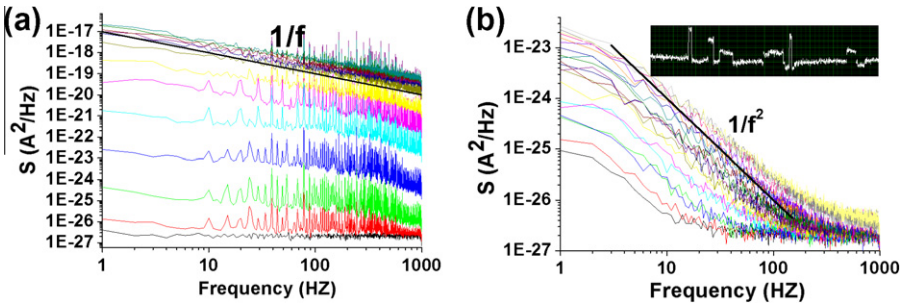

Fig. 13. Comparison of LFN spectra between NMOSFET (L_G = 350 nm, V_{DS} = 50 mV, V_{GS} = 0.1–1.5 V) (a) and NTFET (L_G = 5 μm, V_{DS} = 1 V, V_{GS} = 3–5 V) (b). The inset image shows the RTS signal in NTFET.

3.5. Low frequency noise (LFN) characteristics

The LFN caused by the carrier trapping–detrapping process in the slow oxide traps near the channel-dielectric interface has a $1/f$ signature in MOSFETs. As the area of MOSFET decreases below 1 μm^2, only a few slow oxide traps exist in the entire device, leading to a random telegraph signal (RTS) current noise. The RTS produces a Lorentzian spectrum whose slope is $1/f^2$ [14].

Fig. 13 compares the LFN of NMOSFET and NTFETs with the same 6 nm SiO_2 gate oxides showing totally different spectral behavior. In the NMOSFET with a gate area of 3.5 μm^2 (L_G = 350 nm) the LFN is $1/f$, whereas in the NTFET, the spectrum of the noise is Lorentzian with $1/f^2$ slope even though it is much larger (area = 25 μm^2, L_G = 5 μm). The random telegraph signal can also be observed from the inset image in Fig. 13b, in which two or three trapping–detrapping events are visible.

For TFET, the current is mainly determined by the junction tunneling rate, while the channel provides a way for carrier transport to the drain. The trapping of carriers into the oxide above the channel can only cause the fluctuation of the channel conductance, whereas the tunneling rate at the tunneling junction stays stable. The tunneling rate can only be affected by the trapping process at the Si/SiO_2 interface above the tunneling junction, which is very narrow (around 10 nm). Hence, the effective LFN-generating area of the TFET is very small (0.05 μm^2), including only a discrete numbers of traps, just as in a very small MOSFET. This is why the RTS noise is observed in TFET even though its gate area is nominally large. Conversely, the measured RTS noise confirms that carrier tunneling acts as the primary mechanism in our TFETs. A more detailed discussion of LFN in TFETs, including device-to-device variability, is available in Ref. [26].

4. Conclusions

In this paper, we report on the various aspects of Si TFET performance. We demonstrate that the use of HfO_2 gate oxide with smaller EOT leads to a lower threshold V_T and subthreshold slope S than identically processed thick SiO_2 oxide TFETs, with S decreasing by a factor of ~3. We show that the introduction of an intrinsic region L_{IN} between the channel and the drain in both types of TFETs can largely suppress the I_{LEAK} without impacting I_{ON}. The required L_{IN} falls in the 50–100 nm range, depending on the dopant diffusion. We propose a new TFET model combining the gated tunneling junction in series with the MOSFET channel, which reproduces experimental data over a wide range of drain and gate bias. Finally, we report on low-frequency noise in MOSFET and TFETs and demonstrate that in TFETs the random telegraph signal noise is dominant even in large gate area devices. This is so because the tunneling junction area that determines the current is much smaller than the physical gate length L_G.

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