

Full Two-Dimensional Markov Chain Analysis of Thermal Soft Errors in Subthreshold Nanoscale CMOS Devices

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Abstract—Thermally induced fluctuations in the logic state of a simple flip-flop occur on a timescale that renders them impossible to simulate through Monte Carlo methods. In a previous work, an analytical framework based on Markov chains and queue theory was introduced along with a symbolic solution for a truncated 1-D queue, diagonally connecting the two stable logic states in a two-dimensional (2-D) queue. In this paper, a complete solution for a full 2-D queue is presented, which maps all the possible thermal noise fluctuations of electron populations in flip-flop inverters. The results for the mean time to thermally induced error confirm the estimates given by truncated approximations. This formalism is also capable of computing arbitrary probability moments as well as steady-state distributions and transient behavior of the system. The full 2-D queue can also capture the statistics of other noise sources, like radiation-induced charge generation where the flip-flop can transiently reside in a queue state far from the diagonal connecting the two stable logic states of a flip-flop.

Index Terms—CMOSFET logic devices, Markov processes, Monte Carlo methods, numerical analysis, reliability.

I. INTRODUCTION

RELIABILITY analysis for subthreshold and low-voltage regimes of operation is motivated by the growing field of ultralow-power digital circuits, which furnish one possible avenue for reducing the overall energy consumption. The reduction in the operating voltage V_{dd} reduces the error margin with respect to different noise sources and raises the need for probabilistic frameworks capable of analyzing the effect of various noise sources on low-power devices. The error rate estimates arising from such models can serve as a guideline for designing logic circuits operated at ultralow V_{dd} [1]–[6].

For devices or systems with sufficiently high error rates, Monte Carlo techniques can be effectively employed to estimate the time to error. However, Monte Carlo approaches become computationally prohibitive when the error rates are low: For the simple flip-flop circuit that we will use to demonstrate

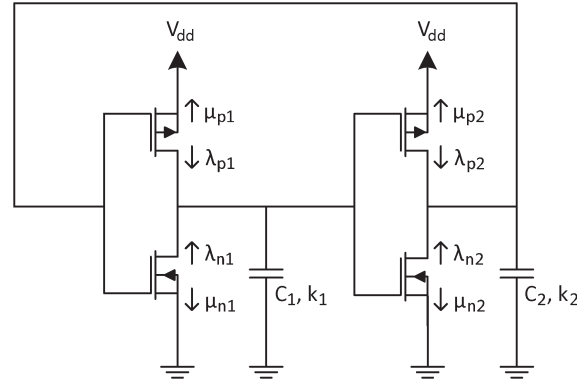


Fig. 1. Modeled flip-flop circuit. Capacitors C_1 and C_2 represent the node capacitances associated with each inverter. For each transistor, the charging and discharging rates λ and μ determine the electron populations k_1 and k_2 on the node capacitances.

our approach, the Monte Carlo computation time increases exponentially with the number of electrons stored on the node capacitances, as detailed in [7]. For this reason, in our previous work [7], [8], a probabilistic framework for the analysis of thermal-noise-induced variations in the logic stability of memory circuits (flip-flops) has been developed. Assuming Poisson processes for the arrival and departure of carriers at the source and drain of a transistor operated in subthreshold regime [9], the charging and discharging rates for the nodal capacitors C_1 and C_2 shown in Fig. 1 can be expressed in terms of the corresponding Poisson rates μ and λ as

$$\begin{aligned} C_i \text{ charging rate} &= \lambda_{ni} + \lambda_{pi} \\ C_i \text{ discharging rate} &= \mu_{ni} + \mu_{pi}. \end{aligned} \quad (1)$$

The charge on capacitors C_1 and C_2 can be mapped onto a 2-D state queue, where each state corresponds to a unique combination of charges k_1 and k_2 on capacitors C_1 and C_2 .

The two valid logic states, namely, “0” and “1”, correspond to states in opposite corners of the 2-D queue. If the noise source is purely thermal, it was shown [7], [8] that thermally induced transitions between the valid states are exponentially rare and occur predominantly on a diagonal path of the 2-D queue. However, other mechanisms of upset, such as radiation events, could create a wide range of charge amounts at either electronic node. This sudden change in the carrier population on the two inverters also changes the state of the system as represented in the 2-D queue, often moving the system far from the

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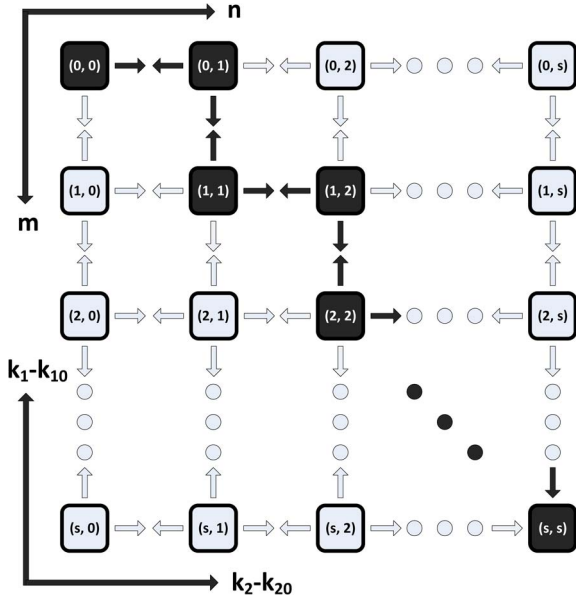


Fig. 2. Two- and one-dimensional Markov chains where state (m, n) corresponds to the flip-flop having $k_1 = s - m + k_{10}$ electrons on one inverter and $k_2 = n + k_{20}$ electrons on the other. The choice of (m, n) over k_1 and k_2 in labeling the states simplifies the algebraic notation and removes the offset electrons k_{10} and k_{20} . The two stable states of the flip-flop are $(0, 0)$ and (s, s) .

stable corner states. Thermal broadening at higher temperatures also necessitates taking into account the states farther from the diagonal. To study the stability of the system in these situations and also in order to confirm the diagonal approximation [7] in estimating the thermally induced soft error rates, a complete solution of the full 2-D queue is necessary. A numerical solution to the full 2-D queue is presented in this paper.

This paper is organized as follows. Section II contains the formulation of the 2-D Markov chain, Section III presents a numerical solution to the full 2-D queue, Section IV expands the formulation of the 2-D queue to arbitrary moments, Section V solves for the steady-state thermal distribution and transient behavior of a 2-D queue, and Section VI contains the conclusions.

II. FORMULATION OF 2-D MARKOV CHAIN

In this section, a probabilistic formulation of a 2-D Markov chain [10] is presented. Instead of formulating for probability density functions (PDFs), an approach for obtaining probability moments of arbitrary degree is established, from which the PDFs can be calculated. For generality, a 2-D chain of $s + 1$ by $s + 1$ states, extending from the stable state $(0, 0)$ to the other stable state (s, s) , is assumed (see Fig. 2), where state (m, n) corresponds to the flip-flop having $k_1 = s - m + k_{10}$ electrons on one inverter and $k_2 = n + k_{20}$ electrons on the other. The choice of (m, n) over k_1 and k_2 in labeling the states simplifies the algebraic notation, as well as removing the offset electrons k_{10} and k_{20} [(i.e., the minimum number of electrons always present in the node capacitors (~ 20 for the simulations in this paper))]. The rates of transmission from any state to its adjacent states are given in four matrices of the same size named \mathbf{u} , \mathbf{d} , \mathbf{r} , and \mathbf{l} for up, down, right, and left, respectively [7].

In this formalism, the initial state is completely arbitrary but the final state or sink is always assumed to be the bottom-right corner state (s, s) . This could represent a stable state in a flip-flop with N electrons on one inverter and zero electrons on the other, ignoring the offsets. Once the sink is reached, a soft error will be recorded and the behavior of the system beyond this point will become irrelevant. Therefore, for computational purposes, it is assumed that the rates for getting out of the sink in all directions are zero.

The random sources governing the transitions in the sub-threshold regime are assumed to be Poisson distributions [9], having their mean equal to the corresponding transition rates.

A. Forming a System of Equations for Calculating the Mean Transit Time

For a given 2-D Markov chain of $s + 1$ by $s + 1$ states, there are $(s + 1) \times (s + 1) - 1$ transit times. The sink has a zero transit time; therefore, it is excluded from the system of equations. For every state, there is an equation connecting its transit time to the sink to the transit times of its adjacent states.

Associated to each state (m, n) are four independent Poisson sources for each main direction with the corresponding rates of $u_{m,n}$, $d_{m,n}$, $r_{m,n}$, and $l_{m,n}$, generating events according to their respective means. They can be written as

$$P_{iu0}(t) = \text{Prob}(\text{going up independently})/dt = ue^{-ut} \quad (2)$$

$$P_{ido}(t) = \text{Prob}(\text{going down independently})/dt = de^{-dt} \quad (3)$$

$$P_{iro}(t) = \text{Prob}(\text{going right independently})/dt = re^{-rt} \quad (4)$$

$$P_{ilo}(t) = \text{Prob}(\text{going left independently})/dt = le^{-lt} \quad (5)$$

where the subscripts for the rates are dropped for better readability.

Since these event sources are independent from each other, whichever triggers first causes the system to jump to the corresponding adjacent state and to continue from that state, which, in general, may have different distributions for its events. For the system to move, for example, up at time t , first, an ‘‘up’’ event should happen, and second, no other events, namely, ‘‘down’’, ‘‘right,’’ or ‘‘left’’ should have happened until time t . This can be written mathematically as

$$\begin{aligned} P_{iu}(t) &= \text{Prob}(\text{‘up’ event} | \text{no other events until time } t) / dt \\ &= P_{iu0}(t) \left(1 - \int_0^t P_{ido}(t') dt' \right) \\ &\quad \times \left(1 - \int_0^t P_{iro}(t') dt' \right) \left(1 - \int_0^t P_{ilo}(t') dt' \right) \\ &= ue^{-(u+d+r+l)t}. \end{aligned} \quad (6)$$

For an arbitrary direction, one has

$$P_{ix}(t) = xe^{-(u+d+r+l)t}, \quad x = u, d, r, l. \quad (7)$$

Note that this PDF is not normalized to unity since the system may never take one particular direction. On the other hand, $\sum_{x=u,d,r,l} P_{ix}(t)$ is normalized, as the system has to exit the state one time or another.

The transit time from state (m, n) to the final state can be represented as the sum of the transit time to an adjacent state and the transit time from there to the final state. The sum of two transit times multiplied by their joint probability, integrated over all possible values for them, and applied for all directions, gives the mean transit time

$$T_{m,n} = \sum_{x=u,d,r,l} \int_0^{\infty} \int_0^{\infty} (t_{ix} + t_{xf}) P_{ixf}(t_{ix}, t_{xf}) dt_{ix} dt_{xf} \quad (8)$$

where t_{ix} is the transit time from the initial state to the neighbor state x and t_{xf} is the transit time from the neighbor state x to the final state or sink. The index (m, n) is implicit in all variables although dropped for better readability.

By the definition of a Markov chain, the probability distribution for t_{xf} is independent of t_{ix} , since the system has no memory of which path it has taken so far. The joint probability P_{ixf} thus reads

$$P_{ixf}(t_{ix}, t_{xf}) = P_{ix}(t_{ix}) P_{xf}(t_{xf}). \quad (9)$$

The form of $P_{ix}(t_{ix})$ is known from (7) for a Poisson source, but $P_{xf}(t_{xf})$ is not known *a priori*. Putting (9) into (8) gives a double integral over t_{ix} and t_{xf} :

$$T_{m,n} = \sum_{x=u,d,r,l} \int_0^{\infty} \int_0^{\infty} (t_{ix} + t_{xf}) P_{ix}(t_{ix}) P_{xf}(t_{xf}) dt_{ix} dt_{xf}. \quad (10)$$

For the first term in (10), the integrals can be rearranged to

$$\left(\int_0^{\infty} t_{ix} P_{ix}(t_{ix}) dt_{ix} \right) \left(\int_0^{\infty} P_{xf}(t_{xf}) dt_{xf} \right) = \int_0^{\infty} t_{ix} P_{ix}(t_{ix}) dt_{ix} \quad (11)$$

noting the fact that $P_{xf}(t_{xf})$ is normalized to unity.

Similarly, rearranging the integrals in the second term of (10) yields

$$\left(\int_0^{\infty} t_{xf} P_{xf}(t_{xf}) dt_{xf} \right) \left(\int_0^{\infty} P_{ix}(t_{ix}) dt_{ix} \right) = T_{xf} \int_0^{\infty} P_{ix}(t_{ix}) dt_{ix} \quad (12)$$

where the first term in parentheses is recognized to be the mean transit time from the neighbor state x to the sink. Putting (11) and (12) back into (10) yields

$$T_{m,n} = \sum_{x=u,d,r,l} \int_0^{\infty} (t_{ix} + T_{xf}) P_{ix}(t_{ix}) dt_{ix}. \quad (13)$$

Evaluating the integral in (13) using (7) finally gives

$$T_{m,n} = z_{m,n} (1 + u_{m,n} T_{m-1,n} + d_{m,n} T_{m+1,n} + r_{m,n} T_{m,n+1} + l_{m,n} T_{m,n-1}) \quad (14)$$

where all the subscripts are restored for clarity and $z_{m,n}$ is defined by

$$z_{m,n} = (u_{m,n} + d_{m,n} + r_{m,n} + l_{m,n})^{-1}. \quad (15)$$

III. SOLUTION FOR THE 2-D MARKOV CHAIN

In this section, after discussing the computational challenges in solving for the equations derived in the previous section, a recursive method capable of addressing these challenges is presented. Both the full 2-D queue and a 1-D diagonal approximation of it are solved using this technique. The 1-D approximation in calculating the mean transit times is confirmed for a fully depleted silicon-on-insulator (FD-SOI) flip-flop.

A. Computational Burdens in Solving for the Transit Times

For the simulations in this paper, a 32-nm FD-SOI technology described in [11] with an effective gate length $L_G \sim 25$ nm and Si channel thickness of 10 nm is used. This technology was chosen for analysis since FD-SOI devices are an advanced technology with low parasitic capacitance that promises to become a mainstream logic and memory technology.

A realistic FD-SOI [11] flip-flop with W/L ratio of 5, operated at subthreshold voltage of $V_{dd} = 0.3$ V, has $N \sim 300$ electrons. The number of electrons increases to $N > 1000$ when transistors with larger W/L ratios are used, for example, for designing radiation-immune systems. This makes solving the system of equations derived in previous sections pose a two-fold challenge. First, since the number of states for the corresponding 2-D system is N^2 , the matrix of equations during Gaussian elimination will contain N^4 elements. The required memory to store such a matrix is approximately 5 TB for the case of $N \sim 1000$, assuming an 8-B double-precision format. Second, for $N > 40$, the system of equations becomes seriously ill conditioned, such that for $N > 50$, the results become totally invalid [12].

To address these challenges, an approach for solving the system of equations is presented in the following sections, employing a recursive algorithm along with the use of arbitrary/multiple precision arithmetic (MPA)¹ where more bits are allocated for storing each element than in conventional double-precision format.

Increasing the degree of precision by using MPA compensates for the numerical errors caused by system sensitivity, removing the ill-conditioning problem. The number of bits needed for each floating-point element to avoid ill conditioning was empirically found to be on the order of number of electrons N .

The recursive approach, not only reduces the complexity of the 2-D system from $O(N^6)$ to $O(N^4)$ [13] but also has a highly scalable structure, making it possible to implement a multithreaded Gaussian algorithm to reduce processing times. The processing time for solving the system aforementioned is

¹The GMP free library was used for the simulations in this project.

about 5 h on a 16-core workstation.² Using this technique, the required memory also drops to 60 GB even when using MPA.

B. Solving Recursively for the Mean Transit Times in a 1-D Chain

Before presenting the full 2-D solution, the solution for a 1-D approximation of the queue, representing the main diagonal between the two stable states at the corners [7], as shown in Fig. 2, is presented here. The 1-D approximation gives an efficient and fast estimation of thermal probability moments within an order of magnitude.

Applying (14) to the shaded diagonal states in Fig. 2 yields

$$\begin{aligned}
 T_{s-1} &= z_{s-1}(1 + l_{s-1}T_{s-2}) \\
 T_{s-2} &= z_{s-2}(1 + l_{s-2}T_{s-3} + r_{s-2}T_{s-1}) \\
 &\vdots \\
 T_n &= z_n(1 + l_nT_{n-1} + r_nT_{n+1}) \\
 &\vdots \\
 T_0 &= r_0^{-1} + T_1
 \end{aligned} \tag{16}$$

in which r and l indicate forward and backward rates. Starting with state $s - 1$, substituting the expression for T_{s-1} into T_{s-2} and rearranging terms gives

$$\begin{aligned}
 T_{s-2} &= z_{s-2}(1 + l_{s-2}T_{s-3} + r_{s-2}z_{s-1}(1 + l_{s-1}T_{s-2})) \\
 &= y_{s-2}z_{s-2}(1 + l_{s-2}T_{s-3} + r_{s-2}x_{s-1})
 \end{aligned} \tag{17}$$

where

$$\begin{aligned}
 y_{s-2} &= (1 - z_{s-2}r_{s-2}y_{s-1}z_{s-1}l_{s-1})^{-1} \\
 y_{s-1} &= 1 \\
 x_{s-1} &= z_{s-1}.
 \end{aligned} \tag{18}$$

By induction, the general term is easily proven to be

$$\begin{aligned}
 T_n &= y_n z_n (1 + l_n T_{n-1} + r_n x_{n+1}) \\
 x_n &= y_n z_n (1 + r_n x_{n+1}) \\
 y_n &= (1 - z_n r_n y_{n+1} z_{n+1} l_{n+1})^{-1}.
 \end{aligned} \tag{19}$$

As the form of (19) suggests, the mean transit time for each state is expressed in terms of that of its predecessor. At the end of the chain, substituting T_1 into T_0 yields

$$T_0 = \frac{r_0^{-1} + y_1 z_1 (1 + r_1 x_2)}{1 - y_1 z_1 l_1}. \tag{20}$$

Now that the value of T_0 is known, the transit times of higher states up to T_{s-1} can be calculated, using (19), by back substitution.

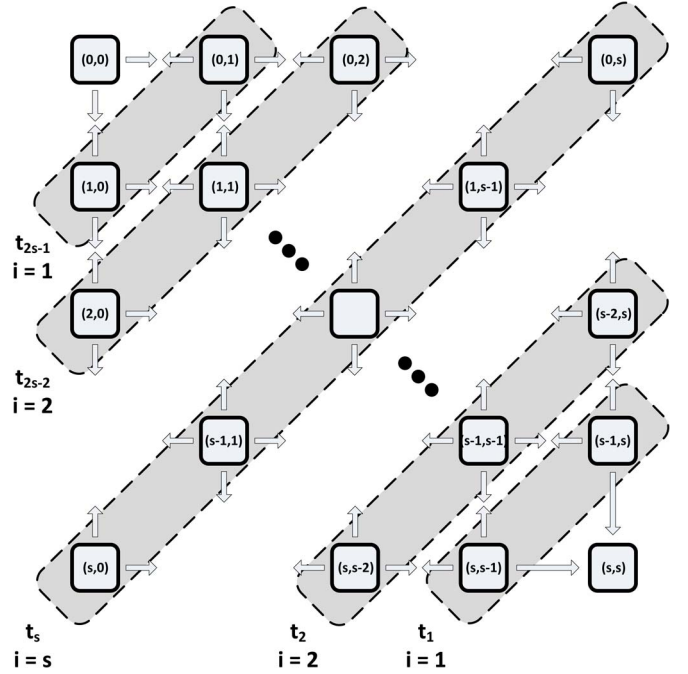


Fig. 3. Diagonal grouping of states for solving the chain recursively.

C. Solving Recursively for the Mean Transit Time in a 2-D Chain

The same approach is taken to solve for transit times of a 2-D system by relabeling the states as in Fig. 3. As the figure suggests, index i runs from 1 to s , starting from the bottom-right corner, and back to 1 again. Note that diagonal t_i has $i + 1$ elements.

For diagonal $i = 1$, as a start of the induction sequence, the two equations concerning $T_{s-1,s}$ and $T_{s,s-1}$ could be written from (14) as

$$\begin{aligned}
 T_{s-1,s} &= z_{s-1,s}(1 + u_{s-1,s}T_{s-2,s} + l_{s-1,s}T_{s-1,s-1}) \\
 T_{s,s-1} &= z_{s,s-1}(1 + u_{s,s-1}T_{s-1,s-1} + l_{s,s-1}T_{s,s-2})
 \end{aligned} \tag{21}$$

or in matrix form

$$\mathbf{A}^1 \mathbf{t}_1 = \mathbf{B}^1 \begin{bmatrix} \mathbf{t}_2 \\ 1 \end{bmatrix} \tag{22}$$

where

$$\mathbf{A}^1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad \mathbf{t}_1 = \begin{bmatrix} T_{s-1,s} \\ T_{s,s-1} \end{bmatrix} \quad \mathbf{t}_2 = \begin{bmatrix} T_{s-2,s} \\ T_{s-1,s-1} \\ T_{s,s-2} \end{bmatrix} \tag{23}$$

$$\mathbf{B}^1 = \begin{bmatrix} (zu)_{s-1,s} & (zl)_{s-1,s} & 0 & (zc^M)_{s-1,s} \\ 0 & (zu)_{s,s-1} & (zl)_{s,s-1} & (zc^M)_{s,s-1} \end{bmatrix}. \tag{24}$$

Note that the last column of matrix \mathbf{B}^1 gets multiplied by the unity in (22). The coefficients $c_{m,n}^M$ will be used later when calculating the higher moments ($M > 1$). For transit times ($M = 1$), $c_{m,n}^M = 1$ for all values of (m, n) .

Solving for vector \mathbf{t}_1 in terms of vector \mathbf{t}_2 yields

$$\mathbf{t}_1 = \mathbf{R}^1 \begin{bmatrix} \mathbf{t}_2 \\ 1 \end{bmatrix} \tag{25}$$

²Four Quad-Core 2.3-GHz AMD Optron 8356 with 64-GB physical memory.

in which

$$\mathbf{R}^1 = (\mathbf{A}^1)^{-1} \mathbf{B}^1 = [\mathbf{X}^1 | \mathbf{Y}^1]. \quad (26)$$

Here, matrix \mathbf{R}^1 is partitioned into matrix \mathbf{X}^1 and vector \mathbf{Y}^1 . \mathbf{X}^1 is a 2-by-3 matrix which multiplies to vector \mathbf{t}_2 , and \mathbf{Y}^1 is a 2-by-1 vector which represents the part of \mathbf{t}_1 independent from \mathbf{t}_2 .

In general, diagonal \mathbf{t}_i is linked to \mathbf{t}_{i+1} and \mathbf{t}_{i-1} , but the dependence of \mathbf{t}_{i-1} on \mathbf{t}_i is known from an earlier step; therefore, \mathbf{t}_i can be expressed solely based on \mathbf{t}_{i+1} . Using (14) and the same formalism introduced in (22)–(26), diagonal \mathbf{t}_i can be expressed in terms of diagonal \mathbf{t}_{i+1} for $i \leq s$ (the lower triangle of the queue) as

$$\mathbf{A}^i \mathbf{t}_i = \mathbf{B}^i \begin{bmatrix} \mathbf{t}_{i+1} \\ 1 \end{bmatrix} \quad (27)$$

where

$$\mathbf{t}_i = \begin{bmatrix} T_{s-i,s} \\ T_{s-i+1,s-1} \\ \vdots \\ T_{s-1,s-i+1} \\ T_{s,s-i} \end{bmatrix} \quad \mathbf{t}_{i+1} = \begin{bmatrix} T_{s-i-1,s} \\ T_{s-i,s-1} \\ \vdots \\ T_{s-1,s-i} \\ T_{s,s-i-1} \end{bmatrix} \quad (28)$$

$$\mathbf{A}^i = \begin{bmatrix} (zd)_{s-i,s} \mathbf{X}_1^{i-1} \\ (zr \mathbf{X}_1^{i-1} + zd \mathbf{X}_2^{i-1})_{s-i+1,s-1} \\ \vdots \\ (zr \mathbf{X}_{i-1}^{i-1} + zd \mathbf{X}_i^{i-1})_{s-1,s-i+1} \\ (zr)_{s,s-i} \mathbf{X}_i^{i-1} \end{bmatrix} - \mathbf{I}_{i+1,i+1} \quad (29)$$

and \mathbf{B}^i is denoted as shown at the bottom of the page, where the subscripts for z, u, d, r, l , and c are stated only once at the end of each row for better readability and \mathbf{I} denotes the identity matrix. Note that the last column of \mathbf{B}^i which multiplies to the unity in (27) is separated from the others for clarity. In addressing row j of matrix \mathbf{X}^i , the notation \mathbf{X}_j^i is used.

When $i = s$, the formulas for \mathbf{t}_s and \mathbf{A}^s are the same as in (28) and (29), with i replaced by s . However, because of the changes in the boundary conditions at the edge of the 2-D queue, \mathbf{t}_{s+1} changes form to

$$\mathbf{t}_{s+1} = \begin{bmatrix} T_{0,s-1} \\ T_{1,s-2} \\ \vdots \\ T_{s-1,0} \end{bmatrix} \quad (31)$$

and \mathbf{B}^s changes to the form shown at the bottom of the page. For the upper triangle of the queue, diagonals are again labeled by index i but are now decreasing from $s-1$ down to 1. The forms of \mathbf{A} , \mathbf{B} , and \mathbf{t} matrices are given as follows, with \mathbf{B}^{2s-i} denoted as shown at the bottom of the next page:

$$\mathbf{t}_{2s-i} = \begin{bmatrix} T_{0,i} \\ T_{1,i-1} \\ \vdots \\ T_{i-1,1} \\ T_{i,0} \end{bmatrix} \quad \mathbf{t}_{2s-i+1} = \begin{bmatrix} T_{0,i-1} \\ T_{1,i} \\ \vdots \\ T_{i,1} \\ T_{i-1,0} \end{bmatrix} \quad (33)$$

$$\mathbf{A}^{2s-i} = \begin{bmatrix} (zr \mathbf{X}_1^{2s-i-1} + zd \mathbf{X}_2^{2s-i-1})_{0,i} \\ (zr \mathbf{X}_2^{2s-i-1} + zd \mathbf{X}_3^{2s-i-1})_{1,i-1} \\ \vdots \\ (zr \mathbf{X}_i^{2s-i-1} + zd \mathbf{X}_{i+1}^{2s-i-1})_{i-1,1} \\ (zr \mathbf{X}_{i+1}^{2s-i-1} + zd \mathbf{X}_{i+2}^{2s-i-1})_{i,0} \end{bmatrix} - \mathbf{I}_{i+1,i+1}. \quad (34)$$

At the end of the recursion, i.e., when $i = 1$ again, the equation reads

$$\begin{bmatrix} T_{0,1} \\ T_{1,0} \end{bmatrix} = \begin{bmatrix} X_{1,1}^{2s-1} & Y_1^{2s-1} \\ X_{2,1}^{2s-1} & Y_2^{2s-1} \end{bmatrix} \begin{bmatrix} T_{0,0} \\ 1 \end{bmatrix}. \quad (36)$$

$$\mathbf{B}^i = - \begin{bmatrix} (zu \quad zl \quad 0 \quad \cdots \quad 0)_{s-i,s} \\ (0 \quad zu \quad zl \quad \cdots \quad 0)_{s-i+1,s-1} \\ (0 \quad 0 \quad \vdots \quad \ddots \quad 0) \\ (0 \quad 0 \quad zu \quad zl \quad 0)_{s-1,s-i+1} \\ (0 \quad 0 \quad 0 \quad zu \quad zl)_{s,s-i} \end{bmatrix} \begin{bmatrix} z (c^M + d \mathbf{Y}_1^{i-1})_{s-i,s} \\ z (c^M + r \mathbf{Y}_1^{i-1} + d \mathbf{Y}_2^{i-1})_{s-i+1,s-1} \\ \vdots \\ z (c^M + r \mathbf{Y}_{i-1}^{i-1} + d \mathbf{Y}_i^{i-1})_{s-1,s-i+1} \\ z (c^M + r \mathbf{Y}_i^{i-1})_{s,s-i} \end{bmatrix} \quad (30)$$

$$\mathbf{B}^s = - \begin{bmatrix} (zl \quad 0 \quad 0 \quad \cdots \quad 0)_{0,s} \\ (zu \quad zl \quad 0 \quad \cdots \quad 0)_{1,s-1} \\ (0 \quad 0 \quad \vdots \quad \ddots \quad 0) \\ (0 \quad 0 \quad 0 \quad zu \quad zl)_{s-1,1} \\ (0 \quad 0 \quad 0 \quad 0 \quad zu)_{s,0} \end{bmatrix} \begin{bmatrix} z (c^M + d \mathbf{Y}_1^{s-1})_{0,s} \\ z (c^M + r \mathbf{Y}_1^{s-1} + d \mathbf{Y}_2^{s-1})_{1,s-1} \\ \vdots \\ z (c^M + r \mathbf{Y}_{s-1}^{s-1} + d \mathbf{Y}_s^{s-1})_{s-1,1} \\ z (c^M + r \mathbf{Y}_s^{s-1})_{s,0} \end{bmatrix} \quad (32)$$

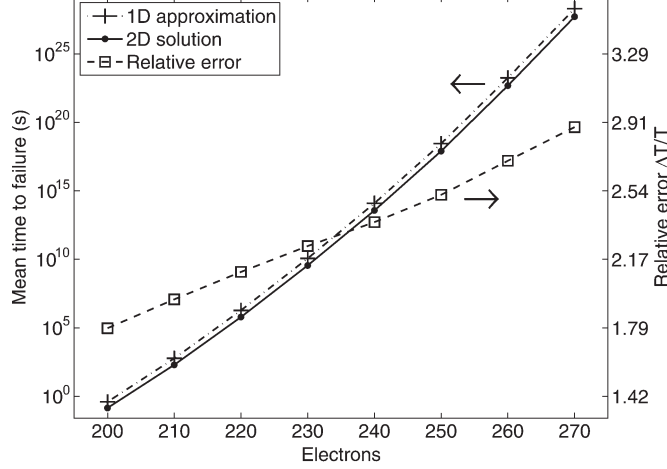


Fig. 4. Transit time $T_{0,0}$ from state $(0, 0)$ to state (s, s) for different numbers of electrons and the corresponding relative errors introduced due to the 1-D diagonal approximation, calculated for an FD-SOI flip-flop with $W/L = 5$, operated at $V_{dd} \sim 0.2-0.25$ V ($N \sim 200-270$) at $T = 100$ °C.

However, from (14)

$$T_{0,0} = z_{0,0} (c_{0,0}^M + r_{0,0}T_{0,1} + d_{0,0}T_{1,0}). \quad (37)$$

Combining (36) and (37) yields

$$T_{0,0} = \frac{z_{0,0} (c_{0,0}^M + r_{0,0}Y_1^{2s-1} + d_{0,0}Y_2^{2s-1})}{1 - z_{0,0} (r_{0,0}X_{1,1}^{2s-1} + d_{0,0}X_{2,1}^{2s-1})}. \quad (38)$$

Now that $T_{0,0}$ is known, all $T_{m,n}$ can be calculated by back substitution.

It is worthy to note that, in order to change the sink to state $(0, 0)$ to study the effects of process-induced asymmetric devices in a flip-flop, it suffices to mirror the elements of the rate matrices horizontally and vertically, swap the mirrored \mathbf{u} and \mathbf{d} matrices, do the same to the mirrored \mathbf{r} and \mathbf{l} matrices, and use the aforementioned formalism with state (s, s) still as the sink.

Fig. 4 shows the transit time $T_{0,0}$ from state $(0, 0)$ to state (s, s) , calculated using both the 1-D approximation and the full 2-D solution for different numbers of electrons in the $V_{dd} \sim 0.2-0.25$ V range. Fig. 4 also shows the relative error introduced by the 1-D approximation calculated using the following:

$$\text{Relative error} = |T_{0,0}^{2D} - T_{0,0}^{1D}| / T_{0,0}^{2D}. \quad (39)$$

As the figure suggests, the 1-D solution is a good approximation in estimating for the mean transit time as the relative error for it is on the order of unity and is only slowly increasing with the number of electrons.

IV. CALCULATION OF THE HIGHER MOMENTS

To calculate the probability moment μ^M , (8) must change to [14]

$$\mu_{m,n}^M = \sum_{x=u,d,r,l} \int_0^\infty \int_0^\infty (t_{ix} + t_{xf})^M P_{ixf}(t_{ix}, t_{xf}) dt_{ix} dt_{xf}. \quad (40)$$

Expanding the binomial and carrying out the integrals on t_{xf} for a few higher moments yields

$$\begin{aligned} \mu^2 &= \sum_x (I_2 + 2I_1\mu_x^1 + I_0\mu_x^2) \\ \mu^3 &= \sum_x (I_3 + 3I_2\mu_x^1 + 3I_1\mu_x^2 + I_0\mu_x^3) \\ \mu^4 &= \sum_x (I_4 + 4I_3\mu_x^1 + 6I_2\mu_x^2 + 4I_1\mu_x^3 + I_0\mu_x^4) \end{aligned} \quad (41)$$

in which $\mu^1 = T$ (transit times) and the integrals I_n are defined by

$$I_n = \int_0^\infty t_{ix}^n P_{ix}(t_{ix}) dt_{ix}. \quad (42)$$

Carrying out the integrals on t_{ix} , summing over x , and collecting terms yields the general form for the M th moment

$$\begin{aligned} \mu_{m,n}^M &= z_{m,n} (c_{m,n}^M + u_{m,n}\mu_{m-1,n}^M + d_{m,n}\mu_{m+1,n}^M \\ &\quad + r_{m,n}\mu_{m,n+1}^M + l_{m,n}\mu_{m,n-1}^M). \end{aligned} \quad (43)$$

Coefficients $c_{m,n}^M$ are given in the following:

$$\begin{aligned} c_{m,n}^2 &= 2z_{m,n} (1 + u_{m,n}\mu_{m-1,n}^1 + d_{m,n}\mu_{m+1,n}^1 \\ &\quad + r_{m,n}\mu_{m,n+1}^1 + l_{m,n}\mu_{m,n-1}^1) \\ c_{m,n}^3 &= 3z_{m,n} \left(2z_{m,n} + 2z_{m,n} \sum_{x=u,d,r,l} x_{m,n}\mu_x^1 \right. \\ &\quad \left. + \sum_{x=u,d,r,l} x_{m,n}\mu_x^2 \right) \\ c_{m,n}^4 &= 4z_{m,n} \left(6z_{m,n}^2 + 6z_{m,n}^2 \sum_{x=u,d,r,l} x_{m,n}\mu_x^1 \right. \\ &\quad \left. + 3z_{m,n} \sum_{x=u,d,r,l} x_{m,n}\mu_x^2 \right. \\ &\quad \left. + \sum_{x=u,d,r,l} x_{m,n}\mu_x^3 \right). \end{aligned} \quad (44)$$

$$\mathbf{B}^{2s-i} = - \begin{bmatrix} (zl & 0 & 0 & \cdots & 0)_{0,i} \\ (zu & zl & 0 & \cdots & 0)_{1,i-1} \\ (0 & 0 & \vdots & \ddots & 0) \\ (0 & 0 & 0 & zu & zl)_{i-1,1} \\ (0 & 0 & 0 & 0 & zu)_{i,0} \end{bmatrix} \begin{bmatrix} z (c^M + r\mathbf{Y}_1^{2s-i-1} + d\mathbf{Y}_2^{2s-i-1})_{0,i} \\ z (c^M + r\mathbf{Y}_2^{2s-i-1} + d\mathbf{Y}_3^{2s-i-1})_{1,i-1} \\ \vdots \\ z (c^M + r\mathbf{Y}_i^{2s-i-1} + d\mathbf{Y}_{i+1}^{2s-i-1})_{i-1,1} \\ z (c^M + r\mathbf{Y}_{i+1}^{2s-i-1} + d\mathbf{Y}_{i+2}^{2s-i-1})_{i,0} \end{bmatrix} \quad (35)$$

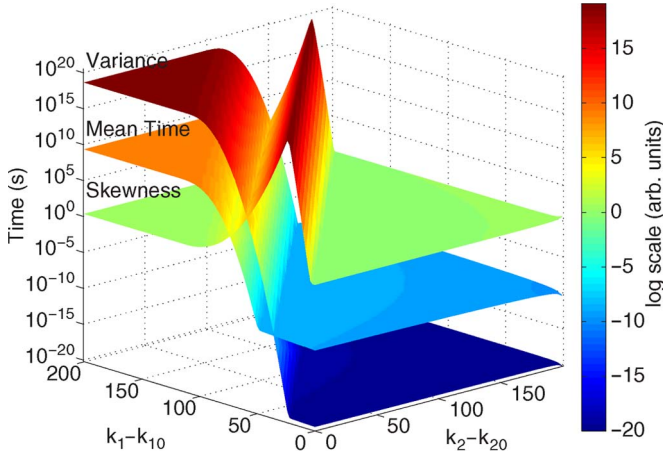


Fig. 5. First three moments of the PDF give the mean time to failure (in seconds), variance, and skewness of the probability distribution. The x - and y -axes map the 2-D queue, while the z -axis presents the numerical results for time to failure, variance, and skewness in an FD-SOI CMOS flip-flop operated at $V_{dd} = 0.22$ V at room temperature. The offset electrons k_{10} and k_{20} are about 20.

Plugging these coefficients into (22)–(35), the same recursive approach can be taken to solve for the higher moments.

Once the first four moments are calculated, they can be related to the variance, skewness, and kurtosis using the following [15]:

$$\begin{aligned} \text{variance} &= \mu_2 - \mu_1^2 \\ \text{skewness} &= \frac{\mu_3 - 3\mu_1\mu_2 + 2\mu_1^3}{(\mu_2 - \mu_1^2)^{3/2}} \\ \text{kurtosis} &= \frac{\mu_4 - 4\mu_1\mu_3 + 6\mu_1^2\mu_2 - 3\mu_1^4}{(\mu_2 - \mu_1^2)^2}. \end{aligned} \quad (45)$$

An illustration for the mean time to failure, variance, and skewness for an FD-SOI CMOS flip-flop is shown in Fig. 5. The device was biased at $V_{dd} = 0.22$ V with 15% threshold variation among the p- and n-transistors and operated at room temperature, resulting in $N \sim 200$ electrons. The mean time to failure for this device is $\sim 10^9$ s, which is equivalent to 30 years. This is a very high error rate on a practical basis: Nowadays, a modern processor has about 8 MB of built-in SRAM cache [16], utilizing more than 67 million flip-flops running concurrently. Assuming independent errors, the mean time to failure drops down to about 30 s for such a system, assuming no error correction. Clearly, operating the system at higher voltages improves the stability exponentially, as shown in Fig. 4. On the other hand, higher temperature, which is expected in future circuits, will also reduce the noise margins. Our approach is capable of accounting for the variation in these technological and operational factors to produce an estimate of error rates for subthreshold flip-flops.

Note that, as much as the high ends of the mean time and variance surfaces characterize the probability of the device to suffer a soft error (i.e., to move from one stable domain to the other (also see Fig. 9)), the low ends of the same surfaces are good measures for device relaxation properties (i.e., to relax to a stable state within the same stability domain) given a small perturbation.

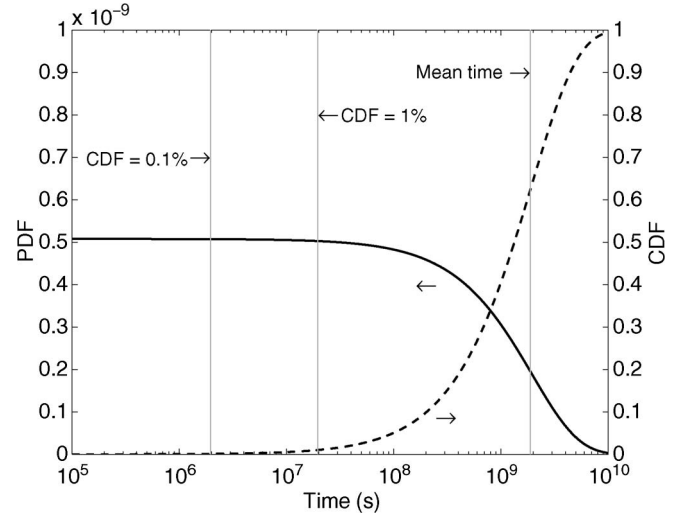


Fig. 6. PDF and CDF for a flip-flop operated at $V_{dd} = 0.22$ V. The mean time to failure for this device is about 2×10^9 (s); however, there are 1% and 0.1% chances that the device fails before 2×10^7 (s) and 2×10^6 (s), respectively.

As Fig. 5 suggests, the variance is typically twice as large in orders of magnitude as the mean; therefore, the standard deviation is on the same order of magnitude as the mean, suggesting a very wide probability distribution [17]. The PDF and cumulative distribution function (CDF) for state (0, 0) of this system are calculated using the first three moments and shown in Fig. 6. Although the mean time to failure for this device is about 2×10^9 (s), there are 1% and 0.1% chances that the device fails before 2×10^7 (s) and 2×10^6 (s), respectively.

V. FORMULATION OF THE STEADY-STATE THERMAL DISTRIBUTION AND TRANSIENT BEHAVIOR OF A 2-D SYSTEM

A. Steady-State Thermal Distribution

The same numerical approach can be used to derive the steady-state thermal distribution of a 2-D system. Given an initial probability distribution for the states of the system, the continuity equation governs the dynamics of probability flow between the states

$$-\alpha \frac{\partial P_{m,n}^{ss}(t)}{\partial t} = (\nabla \cdot r P^{ss}(t))|_{m,n} \quad (46)$$

in which α is a constant of proportionality and $r P^{ss}(t)$ indicates the net probability flow out of state (m, n) . As $t \rightarrow \infty$, the system acquires a global steady state and the probabilities lose their time dependence, making the left-hand side of (46) zero. In this condition, expanding the discrete divergence in the right-hand side of the same equation gives

$$\begin{aligned} &(u_{m,n} + d_{m,n} + r_{m,n} + l_{m,n})P_{m,n}^{ss} \\ &= d_{m-1,n}P_{m-1,n}^{ss} + u_{m+1,n}P_{m+1,n}^{ss} \\ &+ l_{m,n+1}P_{m,n+1}^{ss} + r_{m,n-1}P_{m,n-1}^{ss}. \end{aligned} \quad (47)$$

Equation (47), applied to all the states within a 2-D queue, produces a system of equations which can be solved using

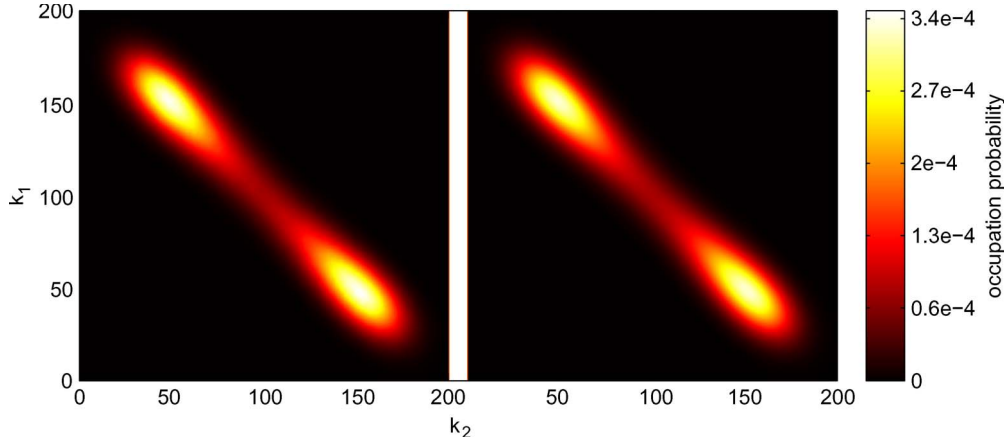


Fig. 7. Comparison between (left) the Monte Carlo simulation for the steady-state probability distribution of a flip-flop after 10^9 iterations and (right) the analytic solution, showing the two stable domains of the device at the top-left and bottom-right corners of the figures. The device is driven at even lower voltages ($V_{dd} = 70$ mV) for the Monte Carlo simulation to observe flips between the stable states of the device. The relative difference between the two results is $\sim 2\%$, which could asymptotically decrease with increasing the number of iterations in the Monte Carlo simulation.

the same techniques described in Section III. For this purpose, according to (47), the rate matrices must change to

$$\begin{aligned} u_{m,n}^{\text{new}} &= d_{m-1,n} \\ d_{m,n}^{\text{new}} &= u_{m+1,n} \\ r_{m,n}^{\text{new}} &= l_{m,n+1} \\ l_{m,n}^{\text{new}} &= r_{m,n-1} \end{aligned} \quad (48)$$

while $z_{m,n}$ is still given by (15) using the original rates. The coefficients $c_{m,n}^M$ should all be set to zero and (37) must change to $P_{0,0}^{\text{ss}} = \text{an arbitrary nonzero constant}$. The 2-D distribution can be normalized later on, after calculating all the elements. Also, in a steady-state behavior, the sink state loses its meaning and (21) must be replaced with

$$\begin{aligned} P_{s,s}^{\text{ss}} &= z_{s,s} (d_{s-1,s} P_{s-1,s}^{\text{ss}} + r_{s,s-1} P_{s,s-1}^{\text{ss}}) \\ P_{s-1,s}^{\text{ss}} &= z_{s-1,s} (u_{s,s} P_{s,s}^{\text{ss}} + d_{s-2,s} P_{s-2,s}^{\text{ss}} \\ &\quad + r_{s-1,s-1} P_{s-1,s-1}^{\text{ss}}) \\ P_{s,s-1}^{\text{ss}} &= z_{s,s-1} (l_{s,s} P_{s,s}^{\text{ss}} + d_{s-1,s-1} P_{s-1,s-1}^{\text{ss}} \\ &\quad + r_{s,s-2} P_{s,s-2}^{\text{ss}}). \end{aligned} \quad (49)$$

To check the validity of the analytic solutions, Monte Carlo simulations were performed and compared with analytic results in Fig. 7. For this purpose, a simple fixed-capacitance device model was picked [7], driven at even lower voltages ($V_{dd} = 70$ mV) for the Monte Carlo simulation to observe flips between the stable states of the device and, hence, to obtain a fairly smooth steady-state distribution after 10^9 iterations. The relative difference between the two results is $\sim 2\%$, which could asymptotically decrease with increasing the number of iterations in the Monte Carlo simulation.

The thermal distribution for an FD-SOI CMOS flip-flop with 15% threshold variation is shown in Fig. 8. Because of the asymmetry in the device resulting from the threshold variation, it is $\sim 10^{13}$ times more likely for us to find the device in the stronger stable state than in the weaker stable state if we let the device run indefinitely without applying an input.

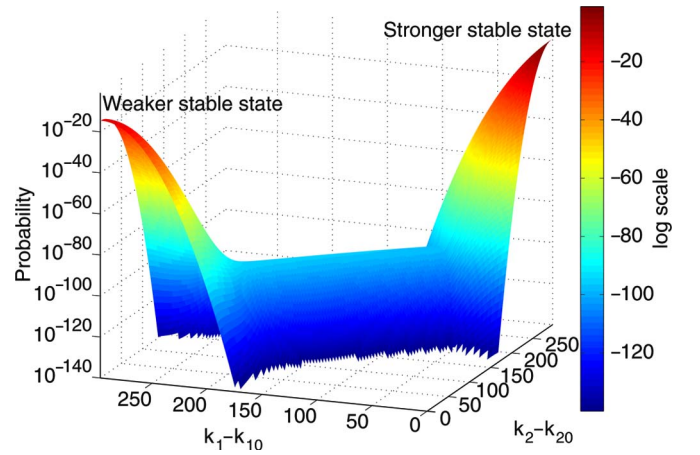


Fig. 8. Process-induced threshold variations in the transistors that make the flip-flop render a given logic state to be more stable than the other. Steady-state thermal broadening for an FD-SOI CMOS flip-flop operated at $V_{dd} = 0.3$ V illustrates the confining of the system within the well-defined logic states and exponentially rare transitions. The x - and y -axes map the 2-D queue, while the z -axis presents the numerical results for the occupation probability of states. The offset electrons k_{10} and k_{20} are about 20.

B. System Transient Behavior

Given a perturbation to the system, for example, due to an incident alpha particle [18], the system changes its state abruptly, most likely to a state away from the two stable states. Such a volatile system will eventually relax to either of its stable states via a transient route on the 2-D queue. Depending on the strength of the initial perturbation and the probabilistic nature of the system in responding to it, the final state might not be identical to the initial one, leading to a soft error. We need to know the probability of collapse to either of the stable states, given an arbitrary initial state anywhere on the 2-D queue. The equations to be solved are

$$P_{m,n}^{\text{tr}} = z_{m,n} (u_{m,n} P_{m-1,n}^{\text{tr}} + d_{m,n} P_{m+1,n}^{\text{tr}} + l_{m,n} P_{m,n-1}^{\text{tr}} + r_{m,n} P_{m,n+1}^{\text{tr}}) \quad (50)$$

where $P_{m,n}^{\text{tr}}$ denotes the probability of collapse to state (s, s) if we let the system initiate from state (m, n) . The probability

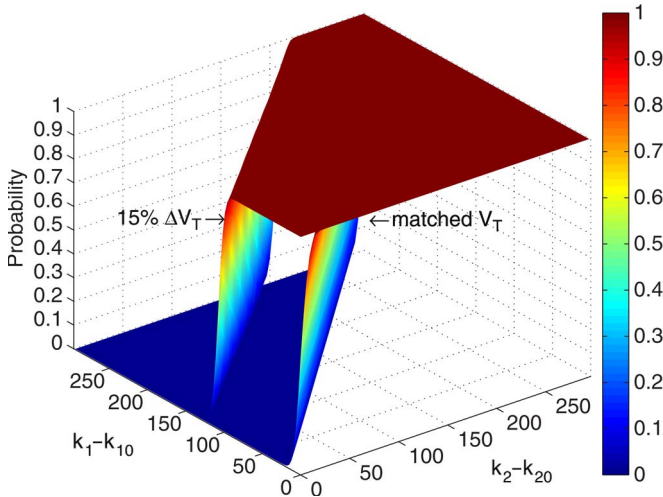


Fig. 9. Transient collapse probability for FD-SOI CMOS flip-flops with matched and 15% mismatched V_T 's, operated at $V_{dd} = 0.3$ V. Starting from any state (m, n) on the 2-D queue, the height indicates the probability for the system to collapse to state $(300, 300)$ corresponding to $k_1 - k_{10} = 0$ and $k_2 - k_{20} = 300$. The probability of collapse to state $(0, 0)$ corresponding to $k_1 - k_{10} = 300$ and $k_2 - k_{20} = 0$ is the 1's complement of this value. The offset electrons k_{10} and k_{20} are about 20.

of collapse to state $(0, 0)$ is evidently $1 - P_{m,n}^{tr}$. Equation (50) can be solved using the same technique described previously for solving the mean times. The only differences here are that the coefficients $c_{m,n}^M$ are zero except for $c_{s-1,s} = d_{s-1,s}$ and $c_{s,s-1} = r_{s,s-1}$ (stemming from the fact that $P_{s,s}^{tr} = 1$) and that (37) changes to $P_{0,0}^{tr} = 0$.

The transient collapse probability for FD-SOI CMOS flip-flops with matched and 15% mismatched V_T 's is shown in Fig. 9. It is evident from the figure that the threshold voltage variation in the device makes the domain of one stable state smaller in favor of the other stable state, which, overall, leads to a less stable device.

VI. CONCLUSION

Monte Carlo simulations of thermal-noise-induced fluctuations in model flip-flops operated at very low voltages have shown that the states within the 2-D queue involved in logic transitions reside near the main diagonal. As described in this paper, the Monte Carlo technique cannot be applied to investigate realistic devices operated at nontrivial voltages because of the timescales involved. In previous works, approximate methods such as symbolic 1-D solution [7] and truncated 2-D queues [8] have been presented and their ability to capture the scaling trend of mean time to error with supply voltage has been outlined.

Raising the complexity of the problem by considering different sources of noise, such as radiation [18], operating voltages above threshold, or adding pass-gate transistors in more evolved memory circuits is expected to change the near-diagonal behavior of fluctuations seen in subthreshold flip-flops, and such approximation methods may fail to capture the statistics of logic noise. As a basis for our future work in expanding the reliability analysis, in this paper, we have presented a complete solution to the full 2-D queue. The pillars of the new approach

are using arbitrary/multiple precision arithmetic to circumvent the ill conditioning that arises with the increased dimension of the queue and a recursive algorithm to solve for the statistics of every state in the 2-D queue.

The present analysis is restricted to the subthreshold region, where the departure and arrival of electrons from/into node capacitors can be represented as two independent Poisson processes. The ongoing work aims at extending the analysis above threshold and considering more complex circuits, where the statistics of electron events can be different from that of a Poisson process, but it is still expected that an algebraic rendering of the problem in a multidimensional queue representation is possible.

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REFERENCES

- [1] T. Yasufuku, T. Niiyama, Z. Piao, K. Ishida, M. Murakata, M. Takamya, and T. Sakurai, "Difficulty of power supply voltage scaling in large scale subthreshold logic circuits," *IEICE Trans. Electron.*, vol. E93-C, no. 3, pp. 332–339, Mar. 2010.
- [2] Y. K. Ramadass and A. P. Chandrakasan, "Minimum energy tracking loop with embedded DC–DC converter enabling ultra-low-voltage operation down to 250 mV in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 256–265, Jan. 2008.
- [3] A. Tajallia, E. J. Brauerb, and Y. Leblebici, "Ultra-low power 32-bit pipelined adder using subthreshold source-coupled logic with 5FJ/stage PDP," *Microelectron. J.*, vol. 40, no. 6, pp. 973–978, Jun. 2009.
- [4] D. Bol, R. Ambroise, D. Flandre, and J. D. Legat, "Interests and limitations of technology scaling for subthreshold logic," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 10, p. 1508, Oct. 2009.
- [5] R. Kumar and V. Kursun, "Temperature-adaptive voltage scaling for enhanced energy efficiency in subthreshold memory arrays," *Microelectron. J.*, vol. 40, no. 6, pp. 1013–1025, Jun. 2009.
- [6] R. Vaddi, S. Dasgupta, and R. P. Agarwal, "Device and circuit co-design robustness studies in the subthreshold logic for ultralow-power applications for 32 nm CMOS," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 654–664, Feb. 2010.
- [7] F. C. Sabou, D. Kazazis, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Markov chain analysis of thermally-induced soft errors in subthreshold nanoscale CMOS circuits," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 3, pp. 494–503, Sep. 2009.
- [8] P. Jannaty, F. C. Sabou, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Numerical queue solution of thermal noise-induced soft errors in subthreshold CMOS devices," in *Proc. 20th GLSVLSI*, 2010, pp. 281–286.
- [9] R. Sarpeshkar, T. Delbruck, and C. A. Mead, "White noise in MOS transistors and resistors," *IEEE Circuits Devices Mag.*, vol. 9, no. 6, pp. 23–29, Nov. 1993.
- [10] D. T. Gillespie, *Markov Processes*. New York: Academic, 1991.
- [11] C. Fenouillet-Beranger, S. Denorme, B. Icard, F. Boeuf, J. Coignus, O. Faynot, L. Brevard, C. Buj, C. Soonekindt, J. Todeschini, J. C. Le-Denmat, N. Loubet, C. Gallon, P. Perreau, S. Manakli, B. Minghetti, L. Pain, V. Arnal, A. Vandoreen, D. Aime, L. Tosti, C. Savardi, F. Martin, T. Salvétat, S. Lhostis, C. Laviro, N. Auriac, T. Kormann, G. Chabanne, S. Gaillard, O. Belmont, E. Laffosse, D. Barge, A. Zauner, A. Tarnowka, K. Romanjec, H. Brut, A. Lagha, S. Bonnetier, F. Joly, N. Mayet, A. Cathignol, D. Galpin, D. Pop, R. Delsol, R. Pantel, F. Pionnier, G. Thomas, D. Bensahel, S. Deleoniibus, T. Skotnicki, and H. Mingam, "Fully-depleted SOI technology using high-k and single-metal gate for 32 nm node LSTP applications featuring $0.179 \mu\text{m}^2$ 6T-SRAM bitcell," in *IEDM Tech. Dig.*, Dec. 2007, pp. 267–270.
- [12] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes: The Art of Scientific Computing*, 3rd ed. New York: Cambridge Univ. Press, 2007, p. 69.
- [13] G. Strang, *Introduction to Linear Algebra*, 3rd ed. Wellesley, MA: Wellesley-Cambridge Press, 2003, pp. 452–453.

- [14] M. Abramowitz and I. A. Stegun, Eds., *Handbook of Mathematical Functions: With Formulas, Graphs, and Mathematical Tables*. Mineola, NY: Dover, 1965, p. 928.
- [15] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes: The Art of Scientific Computing*, 3rd ed. New York: Cambridge Univ. Press, 2007, pp. 723–724.
- [16] [Online]. Available: <http://www.intel.com/products/processor/>
- [17] M. Abramowitz and I. A. Stegun, Eds., *Handbook of Mathematical Functions: With Formulas, Graphs, and Mathematical Tables*. Mineola, NY: Dover, 1965, pp. 997–1010.
- [18] P. Jannaty, F. C. Sabou, M. Gadlage, R. I. Bahar, J. Mundy, W. R. Patterson, R. A. Reed, R. A. Weller, R. D. Schrimpf, and A. Zaslavsky, "Two-dimensional Markov chain analysis of radiation-induced soft errors in subthreshold nanoscale CMOS devices," *IEEE Trans. Nucl. Sci.*, 2010.



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