A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration

J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, *Fellow, IEEE*

***Abstract*—We demonstrate experimentally a capacitor-less one-transistor dynamic random access memory (DRAM) based on fully depleted silicon-on-insulator substrate. In our device, the charges are directly stored in front gate capacitor (C_G) and read out through a fast feedback regeneration process. The simulated read/write times of our device reach below 1 ns, much faster than conventional 1T-1C DRAM. The read/write biasing voltages can be scaled down to 1.1 V, achieving long retention time ($t_{re} > 5$ s).**

***Index Terms*—Capacitor-less, dynamic random access memory (DRAM), feedback, high speed.**

I. Introduction

THE capacitor-based 1T-1C dynamic random access memory (DRAM) has been the prevalent dynamic memory device in recent decades, exhibiting high integration density and good reliability, but suffering from low access speed [1]. The conventional 6-T static random access memory, on the other hand, provides high access speed but low density [2]. Memory devices that can provide both high integration density and high speed are thus of great interest, and several devices have been proposed during the past decade [3]. One example is the thyristor-based RAM (T-RAM) [4]–[6], which is compact and fast, but requires accurate control of the bipolar transistors and precise doping control to achieve stable characteristics [5]. Another example is the field effect diode (FED) with two front gates, which has shown sharp switching and hysteresis properties [7]–[9]. This FED, based on field effect-controlled barrier modulation, was originally proposed for electron static discharge protection [7] and then as a memory device with good simulated scaling capability [9].

In this letter, we demonstrate experimentally the use of a simplified field effect-controlled device (Z^2-FET, for zero-slope, zero-impact ionization FET [10]) as a fast, compact, and refreshable memory. Our fully depleted silicon-on-insulator (FD-SOI) device has only one front gate (V_G) which together with the backgate bias (V_{BG}) forms two adjacent carrier injection barriers. The device also works with fixed oxide charge (Q_S), similar to feedback FET (FB-FET) [11], [12]. The Z^2-FET shows sharp switching and V_G-controlled hysteresis [10] and has fast DRAM functionality without any external capacitor.

Manuscript received October 21, 2011; revised November 14, 2011; accepted November 14, 2011. Date of publication December 27, 2011; date of current version January 27, 2012. The work at Minatec is funded by the RTRA program of the Grenoble Nanosciences Foundation. A. Zaslavsky also acknowledges support by the U.S. National Science Foundation (award ECCS-1068895). Another author (CLR) also acknowledges support by the European STEEPER project (FP7/2007-2013, Grant agreement no. 257267). The review of this letter was arranged by Editor L. Selmi.

J. Wan and S. Cristoloveanu are with IMEP-LAHC, INP-Grenoble, MINATEC, 38016 Grenoble, France (e-mail: wanj@minatec.inpg.fr; sorin@enserg.fr).

C. Le Royer is with CEA-LETI, MINATEC, 38054 Grenoble, France (e-mail: cyrille.leroyer@cea.fr).

A. Zaslavsky is with School of Engineering, Brown University, Providence, RI 02912 USA (e-mail: Alexander_Zaslavsky@brown.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2011.2176908

II. Device Structure and DC Characteristics

Our device is a lateral *pin* diode in the FD-SOI channel, where the intrinsic channel is partially covered by the front gate (L_G) and partially uncovered (L_{IN}) as in an asymmetric tunneling TFET [13]. The device operates with either backgate (V_{BG}) or fixed oxide charge Q_S in the CVD-deposited SiO_2 in the L_{IN} region only (the SiO_2 gate insulator under L_G is thermally grown and contains negligible trapped charge). When the *pin* source-drain diode is forward biased, as shown in Fig. 1(a), the drain current initially remains low because of the injection barriers to electrons (due to front gate $V_G < 0$) and holes (due to $V_{BG} > 0$ or positive Q_S on the intrinsic region L_{IN}). As $|V_D|$ is increased, the drain current I_D increases sharply at a point V_{ON} determined by V_G, as shown in Fig. 1(b), and the I_D–V_D curve exhibits pronounced hysteresis when $|V_D|$ is swept back to zero. Note that our device is fabricated in a standard FD-SOI process with metal gate and raised source/drain technology [13].

The surface potential [see Fig. 1(c)] shows the electron and hole injection barriers formed by V_G and V_{BG} (or Q_S) under low $|V_D|$, respectively. As $|V_D|$ increases close to $|V_G|$, the channel under the gate is depleted and the electron injection barrier is lowered. This causes electron injection from n^+-doped drain into the channel; the electrons flow to the p^+-doped source and induce a potential change at the source junction, thereby reducing the hole injection barrier. As the V_D reaches V_{ON}, the hole barrier is sufficiently reduced to permit hole flow from source to drain, causing positive feedback [7], [10], [11] that turns on the device and eliminates the injection barriers, see the simulated surface potential at $V_D = -2$ V in Fig. 1(c). Since the process does not involve impact ionization [10] or bipolar transistor action and the carrier injection is controlled by the field effect-induced barrier, the device characteristics are relatively insensitive to the temperature. Fig. 1(d) shows the simulated relation between V_{ON} and the amount of Q_S, revealing that V_{ON} is only sensitive to the Q_S over a small range of densities. With enough surface charge, V_{ON} saturates and becomes independent of Q_S, so precise control over Q_S is not required. A value of $Q_S \sim 10^{12}$ cm^{-2} is enough for our devices with $L_{IN} \geq 200$ nm. For devices with shorter L_{IN}, higher surface charge density is needed [see Fig. 1(d)]. This can

0741-3106/$26.00 © 2011 IEEE

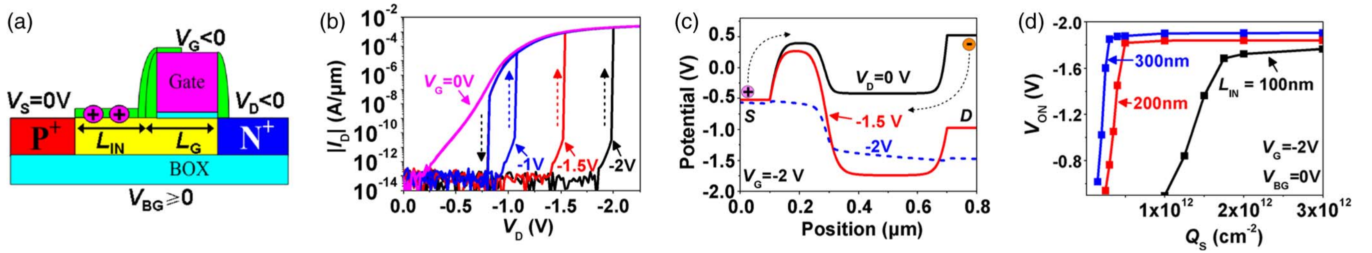

Fig. 1. (a) Schematic layout of the Z^2-FET device operating with backgate bias ($V_{\mathrm{BG}} > 0$) or surface charge (Q_{S}; $V_{\mathrm{BG}} = 0$). The dimensions are $L_{\mathrm{G}} =$ 400 nm, $L_{\mathrm{IN}} = 200$ nm, $T_{\mathrm{si}} = 20$ nm, $T_{\mathrm{ox}} = 6$ nm SiO_2, $T_{\mathrm{BOX}} = 140$ nm and the fixed charge ($Q_{\mathrm{S}} \sim 10^{12}$ cm^{-2}) is formed on the CVD-deposited SiO_2 layer. (b) I_{D}–V_{D} experimental curves versus V_{G}. (c) Modeled surface potential distribution from source to drain. (d) Simulated relation between the fixed oxide charge Q_{S} and the V_{ON}.

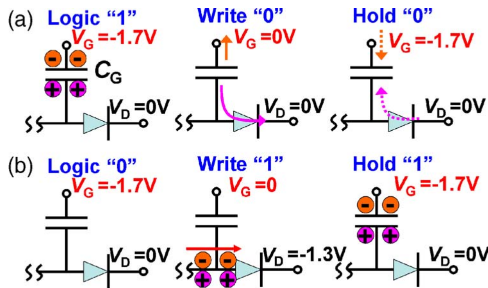

Fig. 2. Equivalent circuit picture of writing "0" (a) and "1" (b) logic states. The dashed line in the hold "0" rightmost panel of Fig. 2(a) corresponds to the leakage current in the reverse-biased drain junction that limits the retention time of logic "0."

be achieved by tuning the CVD process or using high voltage to charge the spacer, as in the FB-FET [11].

III. Capacitor-Less DRAM Operation

The logic states of the device are represented by the mobile charge stored on the front gate capacitor (C_{G}) formed by the gate oxide, with logic "1" corresponding to high charge storage, as shown in Fig. 2. The hold state corresponds to $V_{\mathrm{G}} = -1.7$ V and $V_{\mathrm{D}} = 0$. The logic state readout uses a V_{D} pulse with short fall/rise time (15 ns in the experiment, limited by our equipment): for logic "1," the negative V_{D} pulse discharges the holes stored on C_{G} and generates a transient drain current I_{D} high enough to initiate the feedback process and turn on the device. When the device returns to the hold state ($V_{\mathrm{G}} = -1.7$ V), the holes available in the body recharge the capacitor, enabling intrinsic charge regeneration. Logic "0" corresponds to no charge on C_{G} and hence no response to the V_{D} pulse (the device remains turned off).

The write procedures for logic "0" and "1" are illustrated by the equivalent circuit in Fig. 2. Since the body-source junction is reverse biased, blocking the flow of transient current, only drain and gate need be considered. The writing of logic "0" is shown in Fig. 2(a), where V_{G} is pulsed from -1.7 V to 0, while $V_{\mathrm{D}} = 0$. This discharges the C_{G} through the forward-biased drain diode, overwriting the former "1" state. As V_{G} decreases back to -1.7 V in the hold state, C_{G} is basically not recharged; parasitic recharging occurs via the small leakage current in the reverse-biased drain junction, giving logic "0" a finite but long retention time t_{re}.

Conversely, to write logic "1" from logic "0," V_{G} is pulsed from -1.7 V to 0 and V_{D} is simultaneously pulsed from 0 to -1.3 V, shown in Fig. 2(b). This turns on the device, corresponding to the $|V_{\mathrm{D}}| \gg |V_{\mathrm{G}}|$ situation in Fig. 1(b): the current goes high, and electrons and holes are injected into the channel. As the device switches back to the hold state, $V_{\mathrm{G}} = -1.7$ V and $V_{\mathrm{D}} = 0$, holes are stored on C_{G}. This represents the equilibrium configuration, so logic "1" has an infinite retention time t_{re} and requires no refreshing.

This DRAM functionality is demonstrated experimentally in Fig. 3. Fig. 3(a) shows the writing of logic "0" by pulsing V_{G} from -1.7 V to 0 and then returning to the hold state. Subsequently, using the V_{D} readout pulse, the correct "0" value is read out after a delay $t_0 = 1$ s, but not after 1.5 s. Fig. 3(b) shows the writing of logic "1," as well as the correct readout after both $t_0 = 1$ s and 10 s (as explained earlier, logic "1" has an infinite t_{re}).

The retention t_{re} of logic "0" is determined by the leakage in the reverse-biased drain junction and thus strongly affected by the bias. With the writing and reading waveforms as in Fig. 3, the experimentally measured t_{re} decreases as $|V_{\mathrm{G}}|$ in the holding stage and $|V_{\mathrm{D}}|$ in the reading stage increase—see Fig. 4(a). Experimentally, our DRAM prototype works down to $|V_{\mathrm{D}}| = |V_{\mathrm{G}}| = 1.1$ V, which is competitive with conventional 1T-1C DRAM and lower than floating-body DRAMs. This is helpful for prolonging t_{re}.

IV. Modeling and Reliability

Fig. 4(b) shows the TCAD simulation in Altas [14], reproducing the operating procedure in Fig. 3. In simulation, the read/write times reach below 1 ns, easily outperforming conventional DRAM. In a conventional 1T-1C DRAM, the capacitance needs to be large to store enough charge to reliably distinguish logic "1" and "0" states. This increases read/write time and dynamic power consumption. In our Z^2-FET DRAM, only a few charges need to be stored on C_{G}. Instead of directly reading out the stored charge, as in a 1T-1C DRAM, in our device the stored charge seeds the positive feedback that is activated with the fast reading pulse. Additional simulations (not shown) demonstrate that both L_{G} and L_{IN} are scalable below 40 nm.

Preliminary reliability tests performed on our capacitor-less DRAM show no significant degradation after 6×10^{10} cycles. Also, as mentioned previously, the device characteristics are relatively insensitive to temperature T: increasing T by 80 °C decreases the $|V_{\mathrm{ON}}|$ for $V_{\mathrm{G}} = -2$ V in Fig. 1(b) by only ~0.12 V.

Our device exhibits similar performance with $V_{\mathrm{BG}} \sim 2$ V or with surface charge [10]. The use of V_{BG} instead of Q_{S}

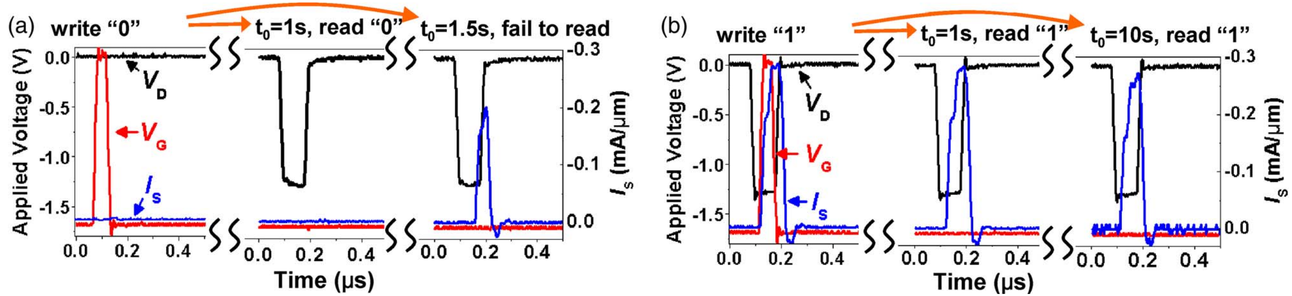

Fig. 3. Experimental results show the DRAM operation waveforms. (a) The logic "0" is written by V_G pulse and read out correctly by V_D pulse after a delay of $t_0 = 1$ s, but not after $t_0 = 1.5$ s, due to limited retention time t_re. (b) The logic "1" is written by simultaneous V_G and V_D pulses and read out correctly by V_D pulse after $t_0 = 1$ and 10 s (t_re is unlimited in logic "1").

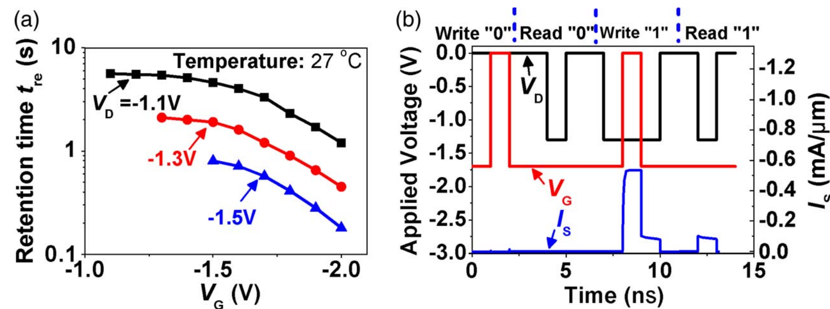

Fig. 4. (a) Experimental logic "0" retention time t_re versus V_G bias under different V_D reading pulses at room temperature. The longest t_re is over 5 s, achieved under the lowest bias $V_\mathrm{G} = V_\mathrm{D} = -1.1$ V. (b) The TCAD simulation shows that the read/write time can reach below 1 ns.

may be advantageous in terms of process control and variability issues. Finally, the voltage waveforms, shown in Fig. 3 for a single memory device, can be easily adapted for array application [15].

V. Conclusion

We have presented a compact, capacitor-less DRAM device in FD-SOI utilizing the field effect-controlled barrier modulation and charge regeneration mechanism. The read and write procedures use fast V_G and V_D pulses for manipulating the charges stored on the front gate capacitor. Experimentally, the gate and drain biasing can be scaled down to 1.1 V, lower than conventional DRAM, to achieve a retention time up to 5 s. Simulations predict access times below 1 ns, thanks to the small C_G needed to store the charge. Our Z^2-FET device has the advantages of compact, single front gate footprint, undoped channel, and no impact ionization or bipolar action.

References

[1] C. J. Radens, S. Kudelka, L. Nesbit, R. Malik, T. Dyer, C. Dubuc, T. Joseph, M. Seitz, L. Clevenger, N. Arnold, J. Mandelman, R. Divakaruni, D. Casarotto, D. Lea, V. C. Jaiprakash, J. Sim, J. Faltermeier, K. Low, J. Strane, S. Halle, Q. Ye, S. Bukofsky, U. Gruening, T. Schloesser, and G. Bronner, "An orthogonal 6F trench sidewall vertical device cell for 4 Gb/16 Gb DRAM," in *IEDM Tech. Dig.*, 2000, pp. 349–352.

[2] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *VLSI Symp. Tech. Dig.*, 2005, pp. 128–129.

[3] M. Bawedin, S. Cristoloveanu, A. Hubert, K.-H. Park, and F. Martinez, "Floating body SOI memory: The scaling tournament," in *Semiconductor-on-Insulator Materials for Nanoelectronics Applications*, A. Nazarov, J.-P. Colinge, F. Balestra, J.-P. Raskin, F. Gamiz, and V. Lysenko, Eds. Heidelberg, Germany: Springer-Verlag, 2011, pp. 393–421.

[4] H.-J. Cho, F. Nemati, R. Roy, R. Gupta, K. Yang, M. Ershov, S. Banna, M. Tarabbia, C. Sailing, D. Hayes, A. Mittal, and S. Robins, "A novel capacitor-less DRAM cell using thin capacitively-coupled thyristor (TCCT)," in *IEDM Tech. Dig.*, 2005, pp. 311–314.

[5] K. J. Yang, R. N. Gupta, S. Banna, F. Nemati, H.-J. Cho, M. Ershov, M. Tarabbia, D. Hayes, and S. T. Robins, "Optimization of nanoscale thyristors on SOI for high-performance high-density memories," in *Proc. Int. SOI Conf.*, 2006, pp. 113–114.

[6] R. Gupta, F. Nemati, S. Robins, K. Yang, V. Gopalakrishnan, J. J. Sundarraj, R. Chopra, R. Roy, H.-J. Cho, W. P. Maszara, N. R. Mohapatra, J. Wuu, D. Weiss, and S. Nakib, "32 nm high-density high-speed T-RAM embedded memory technology," in *IEDM Tech. Dig.*, 2010, pp. 12.1.1–12.1.4.

[7] A. A. Salman, S. G. Beebe, M. Emam, M. M. Pelella, and D. E. Ioannou, "Field Effect Diode (FED): A novel device for ESD protection in deep sub-micron SOI technologies," in *IEDM Tech. Dig.*, 2006, pp. 1–4.

[8] Y. Yang, A. A. Salman, D. E. Ioannou, and S. G. Beebe, "Design and optimization of the SOI field effect diode (FED) for ESD protection," *Solid State Electron.*, vol. 52, no. 10, pp. 1482–1485, Oct. 2008.

[9] Y. Yang, A. Gangopadhyay, Q. Li, and D. E. Ioannou, "Scaling of the SOI field effect diode (FED) for memory application," in *Proc. Int. Semicond. Device Res. Symp.*, 2009, pp. 1–2.

[10] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A feedback silicon-on-insulator steep switching device with gate-controlled carrier injection," *Solid-State Electron.*, 2012, to be published. French patent no. FR1102747, Sep. 12, 2011.

[11] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T.-J. K. Liu, "Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages," in *IEDM Tech. Dig.*, 2008, pp. 1–4.

[12] C. W. Yeung, A. Padilla, T.-J. K. Liu, and C. Hu, "Programming characteristics of the steep turn-on/off feedback FET (FBFET)," in *VLSI Symp. Tech. Dig.*, 2009, pp. 176–177.

[13] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "SOI TFETs: Suppression of ambipolar leakage and low-frequency noise behavior," in *Proc. Eur. Solid-State Device Res. Conf.*, 2010, pp. 341–344.

[14] Atlas Version 2. 10. 4. R

[15] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Cellule mémoire dynamique munie d'un transistor à effet de champs à pente sous le seuil verticale," French Patent no. FR11/03232, Oct. 21, 2011.