Z^2-FET Used as 1-Transistor High-Speed DRAM

Jing Wan,[1a)] Cyrille Le Royer,[2] Alexander Zaslavsky,[1,3] and Sorin Cristoloveanu[1]

[1]IMEP-INPG/Minatec, 3 Parvis Louis Néel, 38016 Grenoble Cedex 1, France

[2] CEA, LETI, MINATEC, F-38054 Grenoble, France

[3] School of Engineering, Brown University, Providence, Rhode Island 02912, USA

[a)] Corresponding author: wanj@minatec.inpg.fr

***Abstract*—We have recently demonstrated a new device named Z^2-FET (*zero* subthreshold swing and *zero* impact ionization) and proposed it as a 1-transistor DRAM. The device is built on an FD-SOI substrate and operates by feedback between carrier flows and injection barriers. We now present additional results obtained from extensive experiments and simulations. Experimentally, the I_{ON}/I_{OFF} ratio exceeds 10^9 and supply voltage (V_{DD}) scales down to 1.1 V with the DRAM retention time as high as 0.15 s at 75 °C. In simulation, the access time reaches below 1 ns and the Z^2-FET can be scaled down to 30 nm. We also discuss various operation modes.**

I. Introduction

The conventional dynamic random access memory (DRAM), combining one transistor and one external capacitor (1T-1C DRAM), has shown good reliability and high integration density [1]. However, the external capacitor is not scalable, as it needs to store enough charge and maintain a long retention time. Thus it requires high aspect-ratio structure, which is challenging to fabricate [2]. The access speed of DRAM is also limited by the required minimum charge storage [1].

The single-transistor capacitor-less DRAM (1-T DRAM) is of great interest due to its compact size [3-4]. Most 1-T DRAMs use the floating body effect, where the stored majority carriers control the flow of minority carriers. Most floating body memories use impact ionization or band-to-band tunneling for writing, leading to slow write speeds and requiring relatively high V_{DD} [5]. These problems have been mitigated recently by using the bipolar writing mode [6]. Another interesting 1-T DRAM is thyristor-based: it shows high integration density and access speed [7-8], but requires precise doping control to obtain stable bipolar characteristics under various temperatures [9]. A field effect diode (FED) with two front gates was used for electrostatic discharge protection and proposed as a capacitor-less memory device [10-12]. Recently, we demonstrated the use of the Z^2-FET as capacitor-less and high speed DRAM using transient feedback [13]. The Z^2-FET is simpler and more compact, with a single front gate and an undoped channel.

Here we systematically study the Z^2-FET used as a 1-T DRAM. The dc (direct current) measurements show sharp switching and gate-controlled hysteresis, resulting from the feedback between carrier flows and their injection barriers, as confirmed by simulation. Unlike the thyristor, the Z^2-FET shows good temperature stability, and does not involve impact ionization or doping-sensitive bipolar action. The Z^2-FET is used as 1-T DRAM with the charge directly stored in the gate capacitor and non-destructively read out through internal feedback amplification. We demonstrate experimentally the scaling of V_{DD} down to 1.1 V. The retention time is studied in detail as the function of temperature, biasing and device size.

II. Device Structure and DC Performance

A. Device structure and DC characteristics

The Z^2-FET is a forward-biased gated *pin* diode built on an FD-SOI substrate with channel partially covered by a gate (L_G) and the rest ungated (L_{IN}), schematically shown in Fig. 1(a). The device operates with either backgate voltage or surface charge Q_S. In a *p*-type device, the front gate is adjacent to the n^+ doped drain and negatively biased. Either a backgate voltage $V_{BG} > 0$ or a positive Q_S on the ungated region is required. Figure 1(b) shows the scanning electron microscope (SEM) image of the *n*-type device, where the gate is adjacent to the p^+ doped drain and positively biased, whereas $V_{BG} < 0$. The device is similar in layout to an asymmetric tunneling FET (TFET) and is fabricated in an advanced SOI process [14-15], featuring HfO_2 gate oxide and raised source/drain. Figures 1(c) and (d) show the measured I_D-V_D curves as a function of V_G in *p*-type and *n*-type devices, respectively. The device is initially in the OFF state at low $|V_D|$, and turns on sharply as $|V_D|$ increases beyond a turn-on voltage (V_{ON}). As $|V_D|$ sweeps back below 0.8 V, the device is turned off. The V_{ON} is linearly controlled by V_G and thus a large controlled hysteresis is obtained.

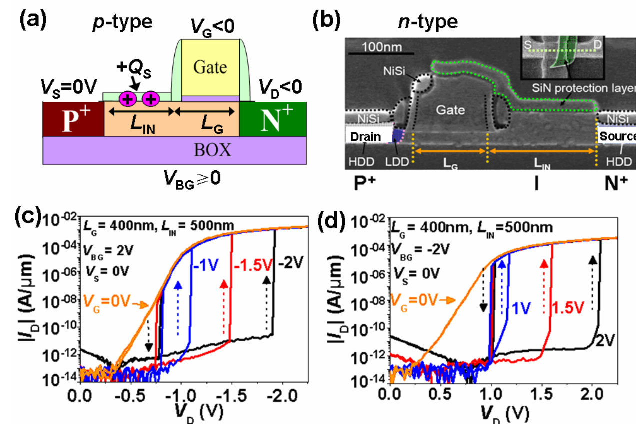

Fig. 1: (a) Schematic structure of the *p*-type Z^2-FET and (b) SEM image of the *n*-type device [14-15]. The device either operates with backgate voltage or surface charge Q_S. Experimental I_D-V_D curves in *p*-type (c) and *n*-type (d) V_{BG}-operated Z^2-FETs show sharp switching and gate-controlled hysteresis. The device parameters are T_{ox} = 3 nm HfO_2, T_{Si} = 20 nm, T_{BOX} = 140 nm, L_G = 400 nm and L_{IN} = 500 nm.

B. Operation principle

The operation principle is understood by TCAD simulation in Silvaco [16]. The simulated I_D-V_D curves reproduce the experimental results well, see Fig. 2(a). The dots in Fig. 2(a) correspond to the simulated results at V_G = –2 V including impact ionization. They show no difference, indicating that the impact ionization is not a factor in the Z^2-FET. The electron and hole injection barriers are formed in the L_G and

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L_{IN} regions by the $V_G < 0$ and $V_{BG} > 0$ (or positive Q_S), respectively, blocking carrier injection under low $|V_D|$, see Fig. 2(b). This biasing scheme emulates a virtual *p/n/p/n* thyristor, but without recourse to any channel doping. As $|V_D|$ increases towards $|V_{ON}|$, the L_G region is depleted, and thus the electron barrier is reduced, causing electron injection from the drain into the channel. The electrons flow to the source and induce a potential drop that reduces the hole injection barrier. This permits hole injection and initiates positive feedback that completely eliminates the injection barriers, see the $V_D = -2$ V curve in Fig. 2(b). As a result, the device turns on sharply to a high current [13], similar to the feedback FET (FB-FET) [17].

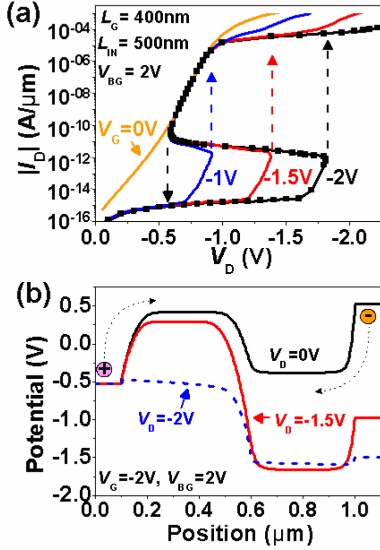

Fig. 2: (a) Simulated I_D-V_D curves of the *p*-type V_{BG}-operated Z^2-FETs reproducing the experimental results in Fig. 1(c). Including the impact ionization (dots) has no effect on the simulation results. (b) Surface potential profile for different V_D values, showing electron and hole injection barriers that are eliminated at $V_D = 2$V.

C. *Reliability and scalability*

In the absence of impact ionization or doping-related bipolar action, the characteristics of Z^2-FET are relatively insensitive to temperature (*T*) variation. Figure 3 shows that the $|V_{ON}|$ of the Q_S-operated Z^2-FET decreases by only ~0.12 V as *T* increases by 80 °C. Simulations show that the V_{BG}-operated device is scalable down to $L_G = L_{IN} \sim 30$ nm given an advanced SOI structure with ultra-thin $T_{Si} = 5$ nm, $T_{BOX} = 15$ nm and $T_{ox} = 1$ nm, which is helpful to enhance the controllability of front and back gates, see Fig. 4.

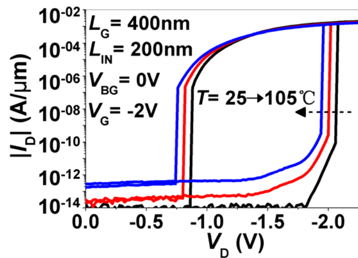

Fig. 3: Experimental I_D-V_D measurements on Q_S-operated Z^2-FET *vs.* *T*, showing small temperature sensitivity of the I_D-V_D hysteresis. The Q_S-operated device is similar to the V_{BG}-operated device in Fig. 1, except that $L_{IN} = 200$ nm, $T_{ox} = 6$ nm SiO_2, $V_{BG} = 0$ and $Q_S \sim 10^{12}$ cm^{-2} formed in the CVD-deposited SiO_2 layer on L_{IN} region [13].

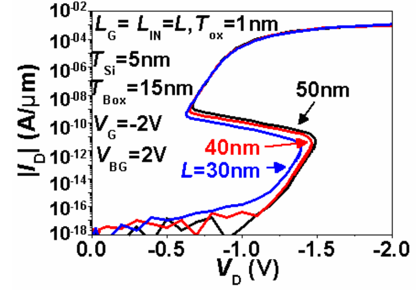

Fig. 4: Simulated scaling of the V_{BG}-operated Z^2-FET (T_{Si} = 5 nm, T_{ox} = 1 nm SiO_2 and T_{BOX} = 15 nm), showing adequate I_D-V_D hysteresis down to $L_G = L_{IN} = 30$ nm.

III. 1-T DRAM Application

A. *1-T DRAM operation using the Z^2-FET*

Thanks to the V_G-controlled hysteresis and temperature insensitivity, the Z^2-FET is well-suited for 1T-DRAM memory application. Figures 5(a) and (b) show the experimental DRAM operation using Q_S-operated Z^2-FET for logic "0" and "1", respectively. The experimental rise/fall times are 15 ns, limited by our equipment. The two logic states are distinguished by the charge stored on the front-gate capacitance C_G, see Fig. 6. For writing "0", $V_G = V_D = 0$ is used to discharge C_G through the drain junction, as shown in Fig. 6(a). In contrast, writing "1" is achieved by turning on the Z^2-FET by applying $V_G = 0$ and $V_D = -1.3$ V. In the ON state, electrons and holes are injected into the channel and the holes are stored on C_G, as the device returns back to hold stage – see Fig. 6(b).

The logic states are read out by pulsing V_D from 0 to –1.3 V while keeping $V_G = -1.7$ V. For logic "1", the transient current due to the C_G discharging generates a voltage drop at the drain junction and causes electron injection from drain. This triggers feedback to turn on the device, with the current

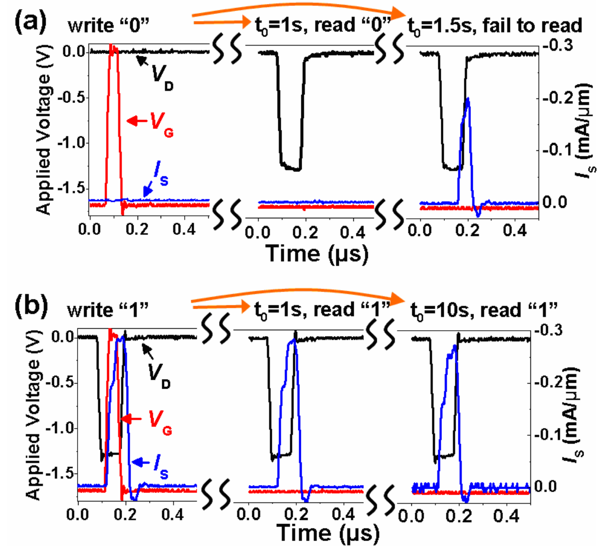

Fig. 5: Experimental results show the DRAM operation waveforms using the Q_S-operated Z^2-FET. (a) The logic "0" is written by V_G pulse and read out correctly by V_D pulse after a delay of t_0 = 1 s, but not after t_0 = 1.5 s, due to limited retention time t_{re}. (b) The logic "1" is written by simultaneous V_G and V_D pulses and read out correctly by V_D pulse after t_0 = 1 and 10 s (t_{re} is unlimited in logic "1").

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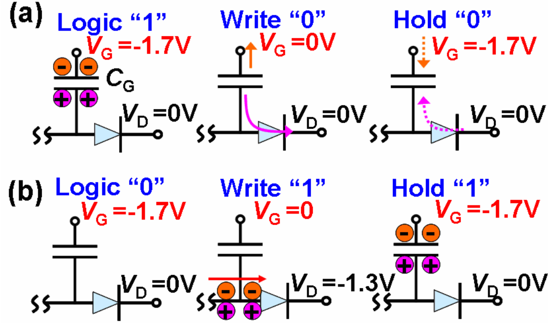

Fig. 6: Schematic writing of (a) "0" and (b) "1" logic states illustrated with an equivalent circuit including the gate capacitor (C_G) and channel-drain junction.

reaching 200 µA/µm, see Fig. 5(a). Conversely, for logic "0", no charge is stored on C_G. Since there is no discharging current, the device stays in the OFF state during the read pulse. Figure 5 (a) shows that the read of logic "0" fails only after a delay t_0 > 1.5 s due to the recharging of C_G by the reverse leakage current, indicated by the dashed arrow in the right-most panel of Fig. 6(a). Thus, while logic "0" requires periodic refreshing, "1" is stable and needs no refreshing.

B. Z^2-FET DRAM performance

The supply voltage of the Z^2-FET DRAM is scalable down to 1.1 V experimentally, which is lower than floating body memories and conventional 1T-1C DRAMs [1, 5], see Fig. 7(a) and (b). The retention time actually improves to 5.5 s due to lower leakage current, but the readout current of the "1" logic state is reduced to ~60 µA/µm.

The ultimate simulated write/read times of our device are very short, down to 1 ns, as shown in Ref. 13. Compared to the 1T-1C DRAM, where a large amount of charge is required to drive the external amplifier, the Z^2-FET DRAM needs less charge storage ΔQ_G because of its internal feedback amplification. Basically, the memory effect is triggered not by ΔQ_G, as in SOI 1T-DRAMs, but by the induced discharge current $\Delta Q_G/\Delta t$.

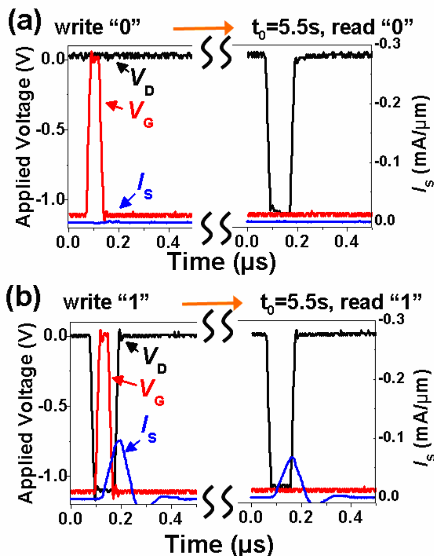

Fig. 7: Transient measurements showing that the Z^2-FET DRAM in Fig. 5 operates under $|V_{DD}|$ = 1.1V with t_{re} increasing to 5.5 s, albeit with lower current for logic "1".

Unlike the standard 1T-1C DRAM, the reading of Z^2-FET DRAM is not only nondestructive but also helps to prolong the retention time (t_{re}) of the logic "0", as shown in Fig. 8. During the readout of the "0" level, the device stays in the OFF state and the residual charges accumulated in C_G are evacuated by the reading pulse. Conversely, the readout of logic "1" turns on the device and regenerates the stored charge in the channel.

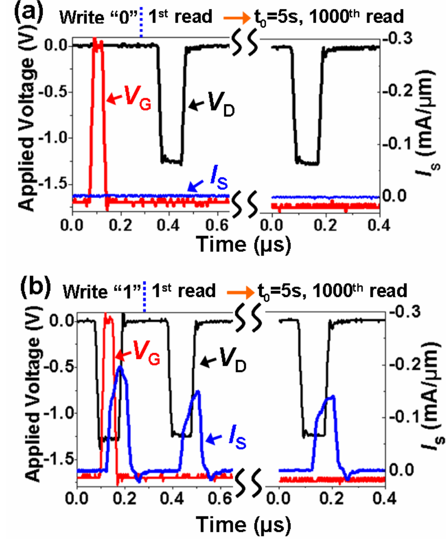

Fig. 8: Measurements on Q_S-operated Z^2-FET DRAM show non-destructive reading of logic (a) "0" and (b) "1" states. The reading pulse V_D is applied periodically every 5ms and outputs correctly after 5 s. The retention of the logic "0" is prolonged by the reading pulses, compared to Fig. 5.

C. Retention time dependence of temperature and scaling

The retention time t_{re} of "0" is determined by the leakage of the drain junction and the capacitance C_G, and thus depends on the device dimensions, biasing voltages, and temperature T, as shown in Fig. 9. We find that t_{re} decreases due to reverse drain junction leakage if either T, $|V_G|$ in the holding stage, or $|V_D|$ in the reading stage are increased. Also, downscaling L_G reduces C_G and thus reduces t_{re}, see Fig. 9(c).

D. Alternative modes of operation

The 1T-DRAM using the V_{BG}-operated Z^2-FET in Fig. 1(c) shows similar behavior, see Fig. 10. Using V_{BG} instead of Q_S is advantageous for controllability and reliability. No degradation is observed after cycling the write/read sequence 6×10^{10} times.

An alternative operation mode of the Z^2-FET uses the source-side MOSFET to write the C_G, as shown in Fig. 11(a). The C_G is charged through a MOSFET, as in a standard 1T-1C DRAM, but the stored charge is still read out through the internal feedback, ensuring less required charge and higher speed. This mode is suitable for a device with two independent gates. Here, we use the V_{BG}-operated Z^2-FET for demonstration, as shown in Fig. 11(b), where the C_G is initially discharged through the drain junction (write "0"), and then recharged by the V_{BG} pulse turning on the source-side MOSFET. The readout correctly outputs high current. This mode may be advantageous because of design rules analogous to the conventional 1T-1C DRAM.

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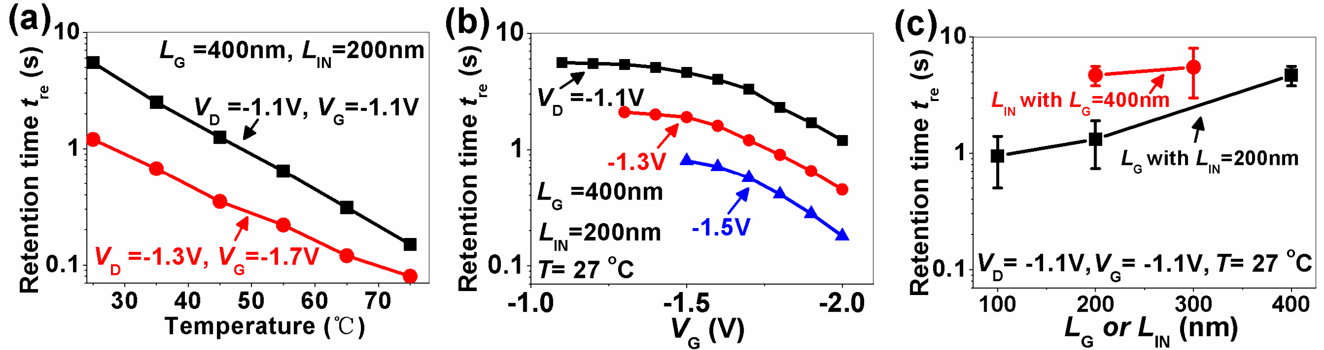

Fig. 9: Experimental results show the dependence of retention time t_{re} of logic "0" on the (a) temperature T; (b) applied V_G and V_D in holding and reading stages, respectively; and (c) dimensions (L_G and L_{IN}). The devices are Q_S-operated Z^2-FET DRAMs.

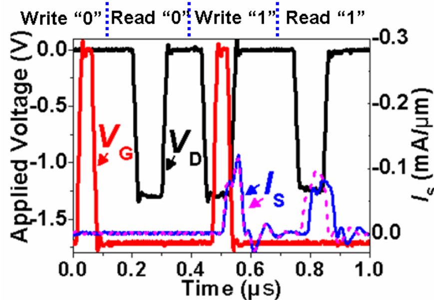

Fig. 10: DRAM operation waveform of the V_{BG}-operated Z^2-FET with V_{BG} = 2 V. The dashed curve shows the output current after $6{\times}10^{10}$ cycles.

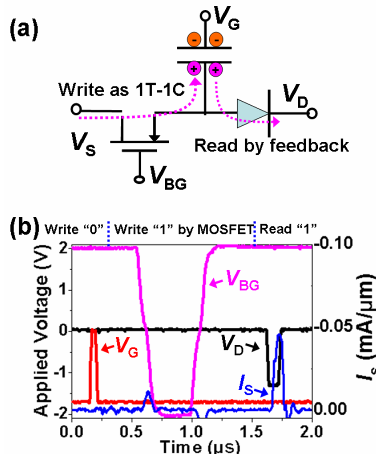

Fig. 11: (a) Schematic view and (b) experimental demonstration of the DRAM mode using the source MOSFET for writing and internal feedback for reading.

IV. CONCLUSION

We have systematically studied the use of Z^2-FET as a 1-T DRAM. The device possesses $I_{ON}/I_{OFF} > 10^9$, $|V_{DD}| \sim 1.1$ V, t_{re} ~ 0.15 s at 75 °C, simulated access time of ~1 ns and scalability down to 30 nm. The high performance and compact form are of interest for future memory generations.

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