Innovative Capacitorless SOI DRAMs

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INTRODUCTION

While the scaling of MOS transistors is still ongoing, the miniaturization of the DRAM storage capacitor is reaching a critical limit. A promising solution consists of eliminating the capacitor. Instead, the charges can be stored in the floating body of an SOI MOSFET, which is also used to read out the memory states. The floating-body 1T-DRAM takes advantage of floating-body and coupling effects that are usually regarded as parasitic phenomena.

In the last decade, competing 1T-DRAM variants have been proposed: partially or fully depleted, planar, vertical or semi-vertical (FinFET), single-gate or double-gate, etc [1-19]. We will focus on our novel concepts (MSDRAM, ARAM, and Z^2-RAM), by addressing the device architecture, operating mechanisms, and scaling issues.

We will finally show that 1T-DRAMs are also compatible with the 'unified memory' paradigm. Solutions are proposed for combining, within a single SOI transistor, volatile and nonvolatile memory functionalities as well as for reaching multiple memory states (≥ 4).

1T-DRAM MECHANISMS

The body of SOI transistors is fully isolated, providing an ideal storage volume. State '1' (high drain current I_1) reflects an excess of majority carriers in the body, which causes the potential and the current to increase. Reciprocally, state '0' features lower current (I_0) and higher threshold voltage due to the removal of majority carriers from the body. In FD SOI n-MOSFETs, negative back-gate biasing is required to retain the majority carriers in the accumulated back-channel. The front and back interfaces are electrostatically coupled, which enables reading the memory state via the front-channel drain current. The magnitude of the current reflects the condition at the back channel: lack of holes (memory state '0') or dynamic excess (state '1').

1T-DRAMs can be categorized according to the mechanism serving to generate the majority carriers: impact ionization, parasitic bipolar transistor, band-to-band tunneling (B2BT), gate tunneling current, and photo-generation. The programming of '0' state requires hole removal by forward biasing the drain-to-body junction. A more efficient solution is to use the dynamic coupling between front and back gates; a sharp increase of the gate bias raises the body potential and naturally turns on the junctions.

1T-DRAM reading is non-destructive because the drain voltage is in general low and does not alter the memory states. Early 1T-DRAM schemes used the threshold voltage shift to read the current in strong inversion. For enhancing the retention time, the transistor architecture can be modified: body engineering by inserting an intermediate low-bandgap SiGe storage layer [13] or source/drain engineering (wide-bandgap SiC electrodes, dopant segregated Schottky contacts, etc) [14,15]. In the following, we describe three advanced solutions compatible with down scaling.

MSDRAM

The MSDRAM is based on the MSD hysteresis effect [7]. The back channel is biased in moderate inversion, the front gate is swept from strong accumulation to 0 V and the drain voltage is low. For high negative V_{G2}, B2BT occurs and rapidly fills the front channel with holes. The memory is at equilibrium and high current (I_1) flows at the back channel. For reverse V_{G1} scan, there are no holes immediately available and the body potential drops in deep depletion, temporarily suppressing the back-channel current (I_0). A very wide memory window is obtained and the current ratio I_1/I_0 exceeds 6 orders of magnitude. Specific source and drain architectures and ultrathin BOX allow enhancing the retention time while reducing the programming voltage (≤ 2 V), back-gate bias and power consumption. The cell scalability was demonstrated by 2D simulations of a 25-nm-long channel cell. The retention time for $I_1/I_0=10$ is 14 s and the programming time is 5 ns. Recent measurements confirm that the MSD effect is maintained in small-area MOSFETs (0.1 μm^2) [20].

ARAM AND A2RAM

The operation of most 1T-DRAMs is based on the coexistence of electrons and holes in the body. However, in ultrathin SOI films (T_{si} < 10 nm), the 'super-coupling' effect forbids the simultaneous formation of adjacent accumulation and inversion layers. ARAM concept solves the super-coupling problem by physically isolating, with a middle oxide (MOX), the holes and electrons in two semi-bodies [16]. The upper semi-body serves for hole storage and the lower semi-body for electron current sensing. To write '1', excess holes are generated by impact ionization or B2BT in the upper semi-body. These holes induce a dynamic increase of the upper

978-1-4673-2691-9/12/$31.00 ©2012 IEEE

semi-body potential, which allows an electron current to flow in the lower semi-body due electrostatic coupling. If no holes are stored, the lower semi-body is fully depleted and no current flows (state '0'). ARAM principles are also applicable in DG MOSFETs and FinFETs.

A second generation device (A2RAM) avoids the need for a MOX [17]. The body is composed of a fully depleted P-layer on top of a thin N^+ layer. The top semi-body stores the holes whereas the N-bridge is used for current sensing. When holes are accumulated at the surface, they screen the vertical electric field and electron current flows through the bridge. By contrast, if the top P-body is temporarily depleted of holes, the gate field is no longer screened and fully depletes the bridge, suppressing the drain current. Retention time over 100 ms was predicted at 85ºC in optimized 22-nm-node cells. Recent measurements have validated the A2RAM concept.

Z^2-RAM

The Z^2-FET is a forward-biased PIN diode [18], where the fully depleted body is only partially covered by the gate. At low V_D the diode is initially blocked because the front and back gates are biased to form potential barriers to the injection of electrons and holes from the N and P contacts, respectively. This gate biasing emulates a PNPN thyristor configuration, but without any body doping. The current remains low until V_D is increased sufficeintly to lower the electron injection barrier. Electrons injected from N contact into the body flow to the source, where they reduce the hole injection barrier. This allows holes to be injected and flow from source to drain, causing positive feedback that turns the device on and completely eliminates the injection barriers. This mechanism results in a strong gate-controlled $I_D(V_D)$ hysteresis.

To program the ‘1’ or ‘0’ states, holes are stored or not stored under the negatively biased front gate. Memory readout consists in discharging the stored charge. In the ‘1’ state, the discharge current $\Delta Q_G/\Delta t$ is sufficient to turn on the Z^2-FET and the read current is high. In the ‘0’ state, there is no discharge current and the diode remains blocked (negligible read current). The read pulse should be fast ($\Delta t \approx 1$ ns) in order to minimize the amount of stored charge needed to trigger the device. Besides excellent access speed, the Z^2-RAM features scalability down to 30 nm gate length, long retention, 1 V operating voltage, and regenerative readout.

UNIFIED MEMORY

The ‘unified memory’ (URAM) aims at combining non-volatile memory (NVM) and DRAM functionalities in a single transistor. A NVM charge trapping layer (ONO) is added to the 1T-DRAM structure [21-23]. Electrons are injected and trapped in the silicon nitride layer like in a standard SONOS memory. NVM programming and erasing steps can be achieved using either Fowler Nordheim or hot carrier injection.

Simultaneously, the floating body is used as a storage volume for the 1T-DRAM function. FinFETs with ONO BOX have been fabricated and tested in the URAM configuration [22]. The buried nitride layer serves to store the NVM charge, which is detected by the current flowing under the front gate. The physical separation of the two interfaces used for NVM programming and reading, respectively, avoids disturbance of the stored charge during sensing. Non-volatile functionality can also be activated by using ONO stack for the MOX dielectric in ARAMs.

In conclusion, the floating-body capacitorless DRAM is a very attractive memory device. There are several competing 1T-DRAM options among which the technologists and circuit designers will make the selection. B2BT is very efficient for ‘1’ state programming, whereas capacitive coupling is suitable for ‘0’ state. 1T-DRAM volatile memory capability can be enriched by adding nonvolatile charge storage.

Acknowledgements. This work was partly supported by projects from European Union (EUROSOI+, Reach 22), France (ANR, RTRA), Spain, and Korea (WCU).

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