Solid-State Electronics 76 (2012) 109–111

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Letter

A feedback silicon-on-insulator steep switching device with gate-controlled carrier injection

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ARTICLE INFO

Article history:
Received 5 January 2012
Received in revised form 2 May 2012
Accepted 21 May 2012
Available online 11 July 2012

The review of this paper was arranged by Prof. E. Calleja

Keywords:
Silicon on insulator
Sharp switching
Field-effect transistor
Positive feedback

ABSTRACT

We experimentally demonstrate a field-effect transistor with a single front gate built on fully-depleted silicon-on-insulator substrate that possesses extremely steep switching slope ($\ll$1 mV/decade) and gate-controllable hysteresis. The mechanism for the sharp switching, confirmed by simulations, involves the positive feedback between the gate-modulated charge injection barriers and the electron and hole components of the source–drain current. The transistor is named Z^2-FET as it features zero impact ionization (unlike thyristors) and zero subthreshold swing.

Sharp switching devices are of great interest to overcome the switching limitations of standard MOSFETs and achieve low subthreshold swing (SS). A number of such devices achieve sharp switching through the use of positive feedback. The thyristor uses two parasitic bipolar transistors triggered by impact ionization and is widely used in power electronics due to its sharp switching and high current drive [1]. A variant known as the thin capacitively-coupled thyristor (TCCT) has been built in fully-depleted silicon-on-insulator (FD-SOI) substrates and successfully demonstrated for SRAM and DRAM memories [2–4], but requires precise doping engineering to obtain reliable performance [5]. The field effect diode (FED) with two front gates, showing sharp switching and hysteresis, was originally used for electrostatic discharge (ESD) protection and then proposed for memory applications [6–8]. Recently, the feedback field effect transistor (FB-FET) has been shown to possess a small subthreshold slope (SS) and high I_{ON} [9,10]. The operation of the FB-FET involves the interaction between the electron and hole source–drain currents and the injection barriers arising from surface charges trapped in the gate spacers.

In this letter, we present a simple device that uses positive feedback similar to the FED and FB-FET except that no trapped surface charges and only one front gate are needed, simplifying the device structure and its fabrication. In our device, similar in layout to an asymmetrical tunneling FET (TFET, Fig. 1a) [11], one of the injection barriers is directly controlled by the front gate (V_G), whereas the other barrier is controlled by the back gate (V_{BG}). The device exhibits sharp switching at low 1–2 V operating voltages (Fig. 1b), as well as a large controllable hysteresis in the drain current–voltage (I_D–V_D) domain (Fig. 1c), where the turn-on voltage (V_{ON}) varies linearly with V_G. Our simulations confirm the gate control of electron and hole injection barriers (V_n and V_p) and show excellent agreement with the experimentally measured V_{ON} and I_D–V_D hysteresis values. They also confirm that while both electron and hole current flows are essential to the operation of our bipolar device, neither impact ionization nor channel doping is involved; front and back gate control alleviates the control of the surface charge or the fabrication of adjacent gates.

The schematic view of the Z^2-FET is presented in Fig. 1a. The fabrication process is described in detail elsewhere [11], here it suffices to mention that the device is built in FD-SOI with a 20 nm thick Si active layer and 140 nm buried oxide (BOX). The channel is undoped and partially covered by the gate in the region denoted by L_G = 400 nm, with a remaining ungated region L_{IN} = 500 nm between the gate and the source. The gate oxide is 3 nm HfO_2 deposited by atomic layer deposition (ALD). As in the TFET, the source and drain (S/D) have different dopants, but the resulting *p–i–n* junction is forward-biased rather than reverse-biased. For the measurement of transfer characteristics, V_G is swept from negative to positive and V_{BG} is kept at 2 V, see the *n*-type device in Fig. 1b. The electron and hole barriers are created by the front and back gates without the need for channel doping or surface charges.

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http://dx.doi.org/10.1016/j.sse.2012.05.061

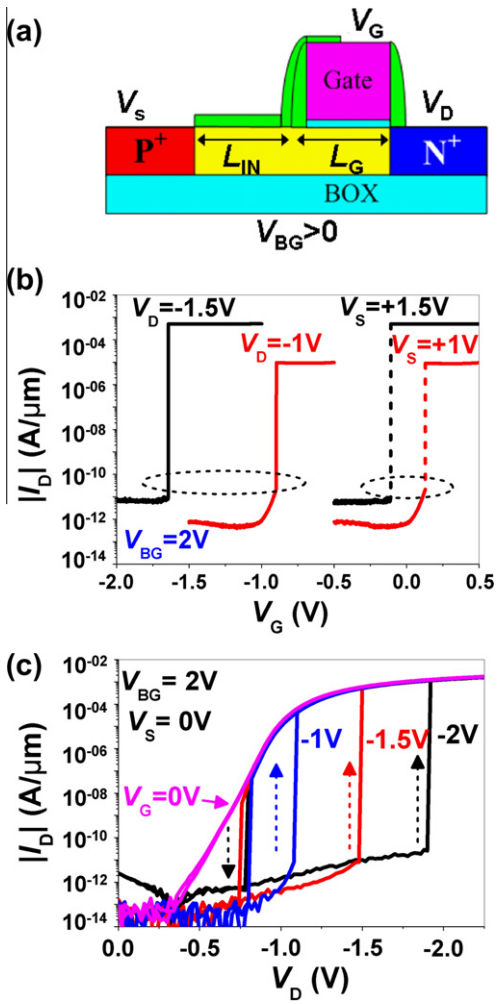

Fig. 1. (a) Shows the schematic view of the *n*-type Z^2-FET. (b) Measured I_D–V_G transfer curves (solid curves: grounded source; dashed curves: grounded drain; V_{BG} = 2 V) showing $I_{ON}/I_{OFF} > 10^8$, SS < 1 mV/dec and I_{ON} > 500 μA/μm. (c) Experimental I_D–V_D curves *vs.* $|V_G|$ = 0–2 V in 0.5 V steps, showing large I_D–V_D hysteresis as V_D is swept from zero through V_{ON}, where the current switches to a large I_{ON}. Device parameters are L_G = 400 nm, L_{IN} = 500 nm, W = 10 μm, with V_{BG} = 2 V.

The transfer I_D–V_G characteristics of the Z^2-FET in Fig. 1b are extremely abrupt: I_D or I_S increase by eight decades within ΔV_G = 1 mV, i.e. *zero* swing. The switching point is determined by the biased terminal (source or drain, defining whether the injection barriers for hole or electron is modified first) and corresponding voltage. This flexibility is very attractive for adjusting the switching voltage in practical CMOS circuits, which combine *n*-type and *p*-type devices (complementary *p*-type Z^2-FETs have also been demonstrated [12]).

Fig. 1c shows the I_D–V_D characteristics, with the source grounded and V_D swept from zero to negative values and then back to zero, for several values of V_G. When $|V_G| > 0.5$ V, the device remains in the I_{OFF} state as $|V_D|$ is increased from zero until V_{ON} is reached, at which point the current increases sharply to I_{ON} that corresponds to a forward-biased diode with a high current drive. The I_{ON}/I_{OFF} ratio is as high as 10^8 in a narrow range of $\Delta V_D < 20$ mV, see Fig. 1c. As $|V_D|$ is swept back down to zero, the current remains high until $|V_{OFF}|$ is reached. The size of the hysteretic loop is controlled by V_G, since $|V_{ON}|$ increases approximately linearly with $|V_G|$.

The mechanism of operation is understood via Silvaco TCAD simulations [13]. Fig. 2 shows the band-diagram in the channel of the device in Fig. 1a as a function of V_D for fixed V_G = −2 V and V_{BG} = 2 V. As $|V_D|$ is increased, the electron injection barrier V_n is reduced, increasing injection, until at $V_D = V_{ON} \sim -1.84$ V, a sufficiently high electron current is injected to reduce V_p, thereby permitting hole injection and establishing the positive feedback, leading the device to switch sharply to the I_{ON} state. This feedback markedly reduces the electron and hole barriers, as shown in Fig. 2 for V_D = −2 V. As compared to FB-FET [9,10], the barriers in our device are determined by V_G and V_{BG}, without recourse to surface charge storage in the gate spacers.

The corresponding simulation of I_D–V_D is shown in Fig. 3 for V_G = 0, −1, −1.5, and −2 V, in good agreement with the experimental results shown in Fig. 1c. The I_D remains low until V_{ON} is reached, at which point it jumps to the large I_{ON} value, indicated by the dashed line (as usual, the negative resistance zone is not observed, leading a hysteretic I_D–V_D characteristic). The added dots in the V_G = −2 V curve correspond to the same simulation with the impact ionization model turned on. As expected for our range of V_G and V_D, impact ionization is not a factor in the device operation.

In detail, the working mechanism of our device can be explained by the evolution of V_n and V_p as V_D decreases towards V_{ON}, see Fig. 4. At low $|V_D|$, the channel under the gate is strongly accumulated with holes due to V_G = −2 V, forming a high V_n barrier and thus blocking the electron injection. The channel potential under the gate (φ_C) decreases with V_D, since the channel–drain junction is forward biased. As V_D decreases below the clamping voltage (V_C), holes are depleted under the gate and the φ_C is clamped by the gate voltage, $\varphi_C \sim V_G$, because the BOX is much thicker than the top oxide. Thereafter, the V_n drops linearly with V_D, since $V_n = \varphi_C - (V_D + V_{biD})$, where V_{biD} is the channel-drain built-in potential. Accordingly, the electrons are injected into the channel and flow to the source. The electron current induces a potential

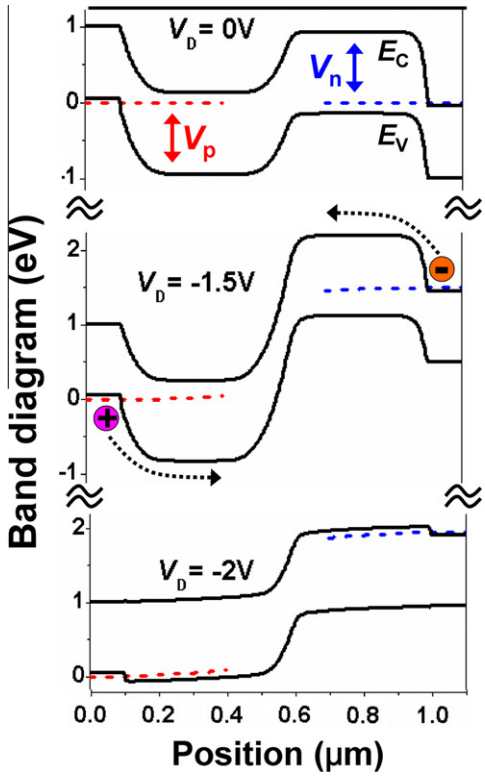

Fig. 2. Simulated band-diagrams of the Z^2-FET under constant V_G = −2 V with V_D = 0, −1.5 V and −2 V. The electron and hole injection barriers are indicated by the double arrows, which block the carriers flow at low $|V_D|$ and are eliminated at V_D = −2 V due to strong feedback.

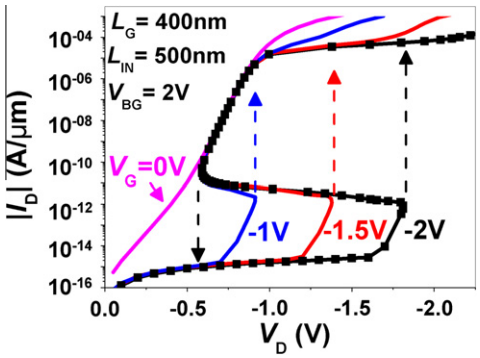

Fig. 3. Simulated I_D–V_D characteristics that reproduce the experimental data in Fig. 1c. The dashed arrows indicate the switching to I_{ON} observed in a dc measurement. Dots mark the $V_G = -2$ V curve simulated with impact ionization model turned on, indicating that impact ionization is not a factor.

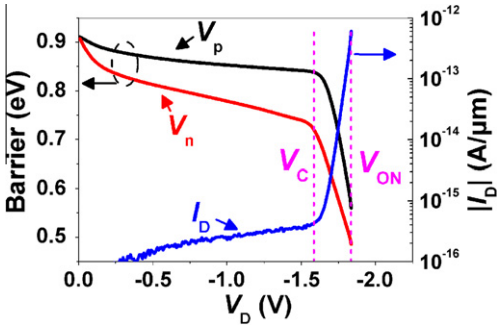

Fig. 4. Evolution of V_n, V_p and I_D as V_D decreases from 0 to V_{ON}. The electron injection barrier V_n is measured along the BOX interface, where it is lowest. In the $0 > V_D > V_C$ region, where V_C is the voltage needed to deplete the holes under the gate and clamp the surface potential to the gate voltage V_G, V_n and V_p remain high and I_D remains low. As V_D decreases below V_C, V_n falls linearly and I_D increases exponentially. High I_{ON} is obtained as V_D further decreases below V_{ON}, where V_n and V_p become negligible.

drop at the source junction and thus lowers the V_p. As V_D approaches V_{ON}, the V_p shrinks, enabling the injection of holes, which flow to the drain and lower V_n. The resulting positive feedback toggles the device to the ON state with high I_{ON}.

The active silicon layer needs to be thin enough for the gate-controlled injection barriers to block the carrier flow throughout the Si channel thickness. This makes the Z^2-FET suitable for the FD-SOI technology, which is evolving towards ultrathin Si channels.

Further simulations show that the Z^2-FET built in advanced SOI substrates with thin silicon and BOX is scalable down to $L_G = L_{IN} = 30$ nm without degrading significantly the $|V_{ON}|$ [12]. Also, in a Z^2-FET with ultra-thin BOX (~10 nm), a heavily-doped ground plane with appropriate polarity, currently used in advanced MOSFETs [14], can induce enough potential in the undoped channel to form the injection barrier even without V_{BG} [12]. Finally, our device can also function using surface charge (Q_S) in the L_{IN} region instead of V_{BG} to form one of the barriers [15], similar to FB-FET [9,10].

In conclusion, we have presented a device possessing gate-controllable hysteresis and a sharp switching property. The structure of the Z^2-FET is similar to asymmetrical TFET with the fabrication process fully compatible with the complementary MOS technology on FD-SOI. From simulations, the operating principle of the Z^2-FET is confirmed to involve positive feedback which is triggered by gate-controlled carrier injection. The Z^2-FET has the advantages of compact, single front gate footprint, undoped channel, no surface charges, no impact ionization and CMOS process compatibility. Thanks to its large hysteresis, where V_{ON} is almost linearly dependent on V_G, steep slope and scalability, the Z^2-FET can find applications as a sharp current switch, electrostatic discharge protection and memory device. We have recently demonstrated [12,15] that the hysteresis in Fig. 1c can be utilized to design fast and low-voltage capacitor-less, single-transistor dynamic memory (1T-DRAM).

Acknowledgments

The Grenoble Nanosciences Foundation (RTRA Program), the US National Science Foundation (Award ECCS-1068895) and the European STEEPER Project (FP7/2007-2013, Grant Agreement No. 257267) are thanked for support.

References

[1] Sze SM. Physics of semiconductor devices. New York: Wiley; 1981. p. 190–242.
[2] Nemati F, Cho H-J, Robins S, Gupta R, Tarabbia M, Yang KJ, et al. Fully planar 0.562 μm² T-RAM cell in a 130 nm SOI CMOS logic technology for high-density high-performance SRAMs. In: Tech dig IEDM; 2004. p. 273–6.
[3] Cho H-J, Nemati F, Roy R, Gupta R, Yang K, Ershov M, et al. A novel capacitor-less DRAM cell using thin capacitively-coupled thyristor (TCCT). In: Tech dig IEDM; 2005. p. 311–4.
[4] Gupta R, Nemati F, Robins S, Yang K, Gopalakrishnan V, Sundarraj JJ, et al. 32 nm high-density high-speed T-RAM embedded memory technology. In: Tech dig IEDM; 2010. p. 280–3.
[5] Yang KJ, Gupta RN, Banna S, Nemati F, Cho H-J, Ershov M, et al. Optimization of nanoscale thyristors on SOI for high-performance high-density memories. In: Intern SOI conf; 2006. p. 113–4.
[6] Salman AA, Beebe SG, Emam M, Pelella MM, Ioannou DE. Field effect diode (FED): a novel device for ESD protection in deep sub-micron SOI technologies. In: Tech dig IEDM; 2006. p. 1–4.
[7] Yang Y, Salman AA, Ioannou DE, Beebe SG. Design and optimization of the SOI field effect diode (FED) for ESD protection. Solid-State Electron 2008;52:1482–5.
[8] Yang Y, Gangopadhyay A, Li Q, Ioannou DE. Scaling of the SOI field effect diode (FED) for memory application. In: Intern semicond dev res symp; 2009. p. 1–2.
[9] Padilla A, Yeung CW, Shin C, Hu C, Liu T-JK. Feedback FET: a novel transistor exhibiting steep switching behavior at low bias voltages. In: Tech dig IEDM; 2008. p. 171–4.
[10] Yeung CW, Padilla A, Liu T-JK, Hu C. Programming characteristics of the steep turn-on/off feedback FET (FBFET). In: Tech dig VLSI symp; 2009. p. 176–7.
[11] Wan J, Le Royer C, Zaslavsky A, Cristoloveanu S. Tunneling FETs on SOI: suppression of ambipolar leakage, low-frequency noise behavior, and modeling. Solid-State Electron 2011;65–66:226–33.
[12] Wan J, Le Royer C, Zaslavsky A, Cristoloveanu S. A systematic study of the sharp-switching Z^2-FET device: from mechanism to modeling and applications. Solid-State Electron, submitted for publication.
[13] Silvaco. Atlas version 2.10.4.R.
[14] Fenouillet-Beranger C, Denorme S, Perreau P, Buj C, Faynot O, Andrieu F, et al. FDSOI devices with thin BOX and ground plane integration for 32 nm node and below. Solid-State Electron 2009;53:730–4.
[15] Wan J, Le Royer C, Zaslavsky A, Cristoloveanu S. A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration. IEEE Electron Dev Lett 2012;32:179–81.