Shot-Noise-Induced Failure in Nanoscale Flip-Flops Part II: Failure Rates in 10-nm Ultimate CMOS

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***Abstract*—In part I of this paper, a robust numerical framework based on Markov queueing theory and nonequilibrium Green's functions was presented to model the fluctuations in a CMOS flip-flop, which could potentially give rise to logic upsets. In part II, this framework is used to investigate quantitatively the failure in time for end-of-roadmap CMOS devices at the $L_G = 10$ nm length scale as a function of various parameters such as size, temperature, threshold voltage, process-induced threshold variation, and V_{DD}. It is shown quantitatively that process-induced variation and/or use of ultralow V_{DD} make the devices extremely vulnerable to noise. Higher temperatures give rise to higher failure rates through increased thermal fluctuations and through reduced $I_{\rm on}/I_{\rm off}$ ratios, due to an inverse dependence of the subthreshold slope on temperature. The effect of nonlinear voltage-dependent node capacitors are modeled via the use of arbitrary-shaped queues, and the corresponding results are reported.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS) devices, Fano factor, Markov processes, nonequilibrium Green's function, numerical analysis, reliability, shot noise, soft errors, SRAMs.**

I. Introduction

As DEVICE miniaturization drives the evolution of silicon technology by making it possible to integrate more devices per unit area, it also makes the quantum nature of current flow more pronounced at the nanoscale, leading to heightened noise sensitivity and higher failure rates. As ultimate CMOS devices are predicted to arrive within a decade [1], it is imperative to scrutinize possible vulnerabilities of such devices with respect to noise.

In Part I of this paper [2], an analytical approach based on nonequilibrium Green's functions and Markov queueing theory for predicting fault rates due to noise in low-power devices [3], [4] is described [5]–[7]. The noise in transistors is expressed in terms of Poissonian and sub-Poissonian current sources, representing different components of the current [8]–[10], and the fluctuation in devices is tied to transitions between the states of a 2-D queue.

In this Part II of this paper, we will demonstrate how this formalism can quantitatively capture the effects of various factors and parameters such as size, temperature, threshold voltage, process-induced variations, and V_{DD} on the failure rates of nanoscale flip-flops, which are made of 10-nm CMOS transistors. As will be shown, the marginal width-to-length ratio, below which the devices will no longer be safe to operate, is estimated to be $W/L_G = 1.5$. Increasing the temperature from $T = 300$ K to $T = 400$ K will reduce the reliability of devices by about ten orders of magnitude in a worst-case scenario. An asymmetrical threshold variation of $\Delta V_T = \pm 20$ mV will also cause severe reliability concerns. The aggregate effects of various reliability concerns on failure rates are also discussed. For example, it is estimated that the minimum operable V_{DD} without any threshold variation is about 0.4 V, as opposed to 0.3 V, when V_T variations are taken into account. To obtain more accurate results, we also present a technique for accommodating nonlinear voltage-dependent node capacitors via the use of arbitrary-shaped queues.

The rest of this paper is organized as follows. Section II gives a brief description of a 10-nm model transistor and some theoretical background on failure-rate calculation. Section III presents the error rates for flip-flops based on ITRS-predicted 10-nm-gate-length technology, whereas Section IV presents the conclusions.

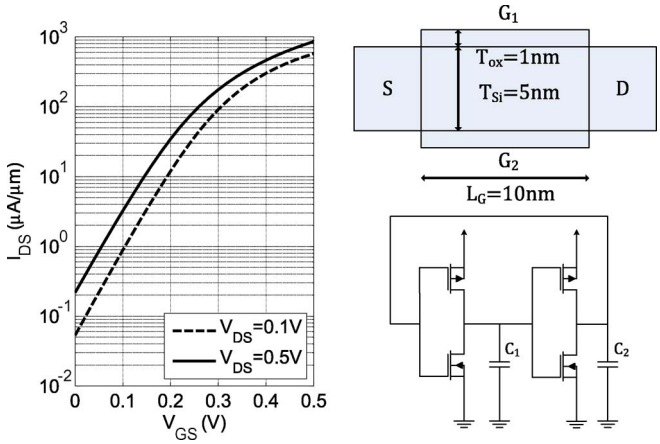

Fig. 1. Schematic of an ITRS-predicted LSTP DG-MOSFET, its I–V characteristics calculated using a 2-D Schrödinger–Poisson solver and the modeled flip-flop composed of four such transistors. Both intrinsic and parasitic capacitances are lumped into C_1 and C_2, as shown in the figure.

II. Theoretical Background

Fig. 1 illustrates both the schematic and the I–V characteristics of an ITRS-predicted low-standby-power double-gate

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metal–oxide–semiconductor field-effect transistor (LSTP DG-MOSFET) [1] with an effective gate length of $L_G = 10$ nm, a Si channel thickness of $T_{\rm Si} = 5$ nm and an equivalent oxide thickness of $T_{\rm ox} = 1$ nm. These devices make up a nanoscale flip-flop, as shown in the same figure.

The numbers of elementary charges on the two capacitors C_1 and C_2 in Fig. 1 map the states of a flip-flop onto a 2-D queue. The absolute rate of transition from any state (m, n) to any neighboring state (r, s) is derived in Part I, which is based on the probability of such transition at time t as follows:

$$R(m, n; r, s) = \int_0^\infty dt P_{\rm direct}(m, n; r, s; t). \quad (1)$$

Similarly, the average time spent in any state (m, n) upon entering that state is

$$A(m, n) = \sum_{(r,s)} \int_0^\infty dt\, t P_{\rm direct}(m, n; r, s; t). \quad (2)$$

Given these two fields, the mean transit times from any state (m, n) to any state (u, v) are expressed in the form of a linear system of equations as follows:

$$T(m, n; u, v) = A(m, n) + \sum_{(r,s)} R(m, n; r, s) T(r, s; u, v) \quad (3)$$

where the summation is the overall neighboring states of (m, n). Similarly, the steady-state occupation probability for any state, i.e., $P_{s.s.}(m, n)$, constitutes a system of equations as follows:

$$P_{s.s.}(m, n) = A(m, n) \sum_{(r,s)} \frac{R(r, s; m, n)}{A(r, s)} P_{s.s.}(r, s). \quad (4)$$

Upon solving for $T(m, n; u, v)$, using the techniques described in [2], the mean time to spontaneous failure for the device due to shot noise is inferred by taking state (m, n) to represent logic "0" of the flip-flop with C_1 fully charged and C_2 empty of charge, and by taking state (u, v) to represent logic "1" of the flip-flop with the roles of C_1 and C_2 interchanged.

Although the main focus of this paper is the effect of shot noise on device reliability, our formalism is also capable of handling other types of reliability concerns such as $1/f$ noise, random telegraph signal (RTS) noise and negative bias temperature instability (NBTI), through either incorporating their probability distributions [11] directly into the queue or modeling their effect using the threshold voltage shifts ΔV_T, as discussed later.

III. Results and Discussion

The flow between the states of a 2-D queue representing a 10-nm-gate-length technology is plotted in Fig. 2 over a full range of node capacitor voltages V_{C1} and V_{C2} with a typical fixed node capacitance of $C_i = 10^{-15}$ F/μm $(i = 1, 2)$, as predicted by the ITRS [1] (the effects of voltage-dependent capacitances will be discussed later). The operating temperature $T = 300$ K, $V_{DD} = 0.5$ V, and all transistors have equal threshold voltages of $|V_T| = 0.15$ V. The full voltage range corresponds to $N \sim 75$ states, each representing a single electron

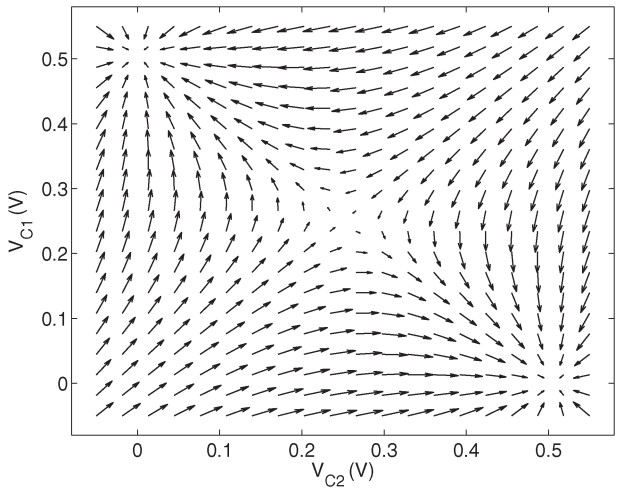

Fig. 2. Four sets of normalized average noise rates responsible for charging and discharging node capacitors C_1 and C_2, which are depicted as a 2-D vector field where each component denotes net charging rates.

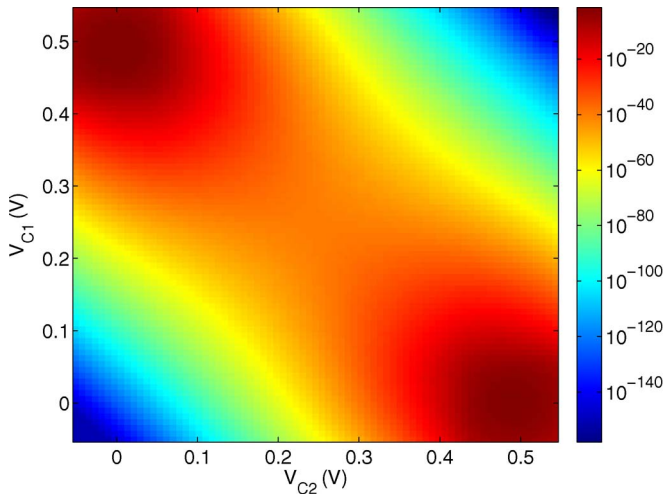

Fig. 3. Steady-state occupation probability for a flip-flop made out of 10-nm-gate-length CMOS transistors, driven at $V_{DD} = 0.5$ V. The x- and y-axes represent the voltages on the two node capacitors C_1 and C_2, and the color scheme represents the occupation probability in a logarithmic scale. The two states with highest probabilities correspond to $V_{C1} = 0$ and $V_{C2} = V_{DD}$, and $V_{C1} = V_{DD}$ and $V_{C2} = 0$.

on a capacitor. Fig. 2 was made by constructing a vector field out of (1), where the x and y components of the field are defined as

$$x(m, n) = R(m, n; m, n + 1) - R(m, n; m, n - 1) \quad (5)$$
$$y(m, n) = R(m, n; m + 1, n) - R(m, n; m - 1, n). \quad (6)$$

The two stable logic domains at the corners are separated by a diagonal.

The steady-state occupation probability for the same device is calculated using (4) and shown in Fig. 3 in a logarithmic scale over a full range of node capacitor voltages V_{C1} and V_{C2}. As suggested by the figure, the device spends most of its time in the neighborhood of its two stable logic states. The two stable logic states are connected by a ribbon through which a spontaneous transition from one stable domain to the other could take place. After identifying the two extreme states with

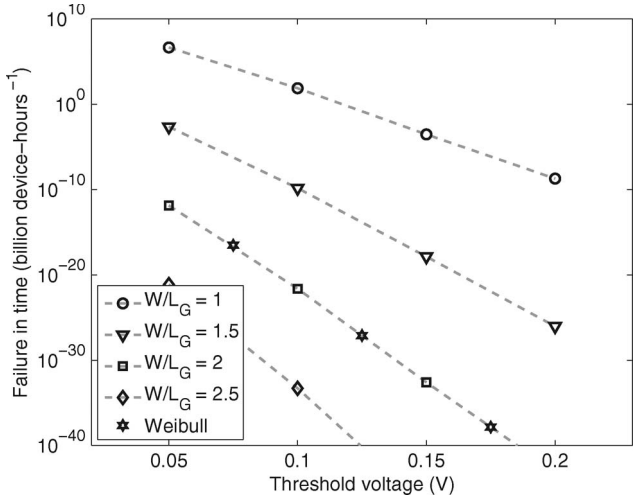

Fig. 4. FIT for an $L_G = 10$ nm gate-length technology operated at $V_{DD} = 0.5$ V, representing the number of soft errors in 10^9 device-operation hours, plotted for various values of the W/L_G ratio and threshold voltage V_T at $T = 300$ K. Higher threshold voltage and larger width lead to a more stable device. The stars for the $W/L_G = 2$ case represent data points obtained through the use of the Weibull distribution [12], instead of the gamma distribution for electron arrival times, indicating the robustness of our results (see text, as well as [2] for a discussion).

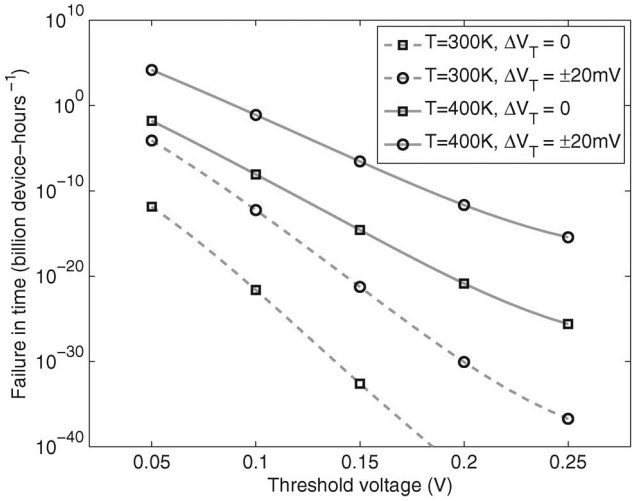

Fig. 5. Effect of temperature and threshold voltage variation on FIT for the same technology node. FITs are compared at two temperatures $T = 300$ K and $T = 400$ K, both for $W/L_G = 2$ and $V_T = 0.15$ V. Higher temperature has significant effect in increasing the failure rate. Likewise, threshold voltage variation between the two transistors making up an inverter increases FIT sharply.

maximum occupation probabilities, we define mean time to failure as the average time for a spontaneous transition between these two states.

The failure in time (FIT), which is defined as the number of failures per one billion device-operation hours, is calculated for the same technology node using the scheme portrayed in the previous section for different values of transistor width W and threshold voltage V_T and shown in Fig. 4. Reflected in the plot is that devices with wider transistors are more immune to soft error, which is due to the fact that wider transistors can store more charge because of their larger channel capacitance. Therefore, in order for the device to flip, a correspondingly longer chain of spontaneous transitions along the diagonal between the stable states (see Fig. 2) is required to push the device from one stable logic domain into another, resulting in an exponentially lower failure rate, e.g., an improvement of $\sim 10^{18}$ in FIT when doubling the device width at threshold voltages as low as $V_T = 0.05$ V.

Fig. 4 also suggests that devices with higher threshold voltage are more robust to shot-noise fluctuations, which is due to their larger $I_{\rm on}/I_{\rm off}$ ratios that accentuates the difference between the two logic states of a constituent inverter, resulting overall in a more robust device. Because of this, there is an inherent tradeoff between switching speed performance and noise immunity, as high V_T means lower $I_{\rm on}$ current and longer charging times for a given V_{DD}. According to Fig. 4, approximately every 5-mV increase in the threshold voltage improves the failure rate by an order of magnitude for a device with $W/L_G = 2$.

As discussed in Part I [2], the numerical results are not sensitive to the exact choice of electron interarrival time distributions as long as they have predefined means and variances and continuously reduce to the Poisson distributions as the Fano factor approaches unity. This has been shown in Fig. 4, where for the case of $W/L_G = 2$, the failure rates have been recalculated using the Weibull distribution [12] instead of the gamma distribution, confirming the fact that the failure rates are indeed unchanged.

The effect of temperature for the same technology node with $W/L_G = 2$ is illustrated in Fig. 5. Evident from the figure is that devices operated at a higher temperature of $T = 400$ K (shown in solid lines) have much higher failure rates than those operated at $T = 300$ K (shown in dashed lines). This is primarily due to increased thermal fluctuations but also due to the reduced subthreshold slope leading to lower $I_{\rm on}/I_{\rm off}$ ratios, as discussed above.

Fig. 5 also illustrates the effect of threshold voltage variation ΔV_T between the constituent transistors in a device, arising from process variations. We picked a worst-case symmetrical configuration for threshold variations such that p-channel MOS1 (PMOS1) and n-channel MOS2 (NMOS2) in Fig. 1 have $|V_T| = |V_{T0}| + \Delta V_T$ and PMOS2 and NMOS1 have $|V_T| = |V_{T0}| - \Delta V_T$, where $\Delta V_T = 20$ mV. As evident from the figure, threshold variation increases the failure rates by about eight orders of magnitude at threshold voltages as low as $V_T = 0.05$ V and by more than 16 orders of magnitude at threshold voltages as high as $V_T = 0.25$ V. However, the FIT increase at lower threshold voltages, although nominally smaller, is more detrimental to the robustness of the device in practice, as the failure rates are already high in such cases, e.g., on the orders of 10^{-4} at $T = 300$ K and 10^4 at $T = 400$ K.

As mentioned in the introduction, the effect of other types of noise such as RTS noise could be modeled through momentary variations in the threshold voltage [13], [14]. Using this technique, one can estimate the worst-case failure rate by taking the threshold voltage variation due to RTS noise and then reading off the corresponding failure rates from Figs. 4 and 5. A similar approach can be taken for estimating the effect of NBTI.

For the purposes of low-power electronics applications, it is desirable to design circuits that could be operated at low V_{DD} voltages. Fig. 6 shows the effect of lowering V_{DD} on

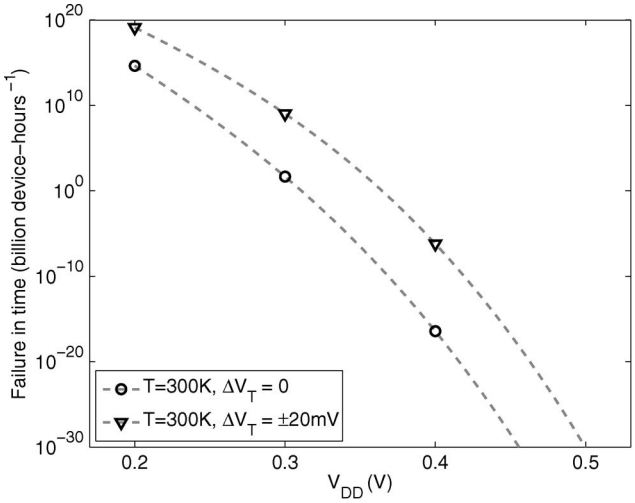

Fig. 6. Role of V_{DD} in changing the failure rates. Here, $W/L_G = 2$ and $V_T = 0.15$ V, and the FITs are plotted for two cases with and without threshold variations. For the case without the threshold variation, driving V_{DD} below 0.4 V makes the devices "unsafe" to the point that, for $V_{DD} < 0.3$ V, the devices are essentially inoperable.

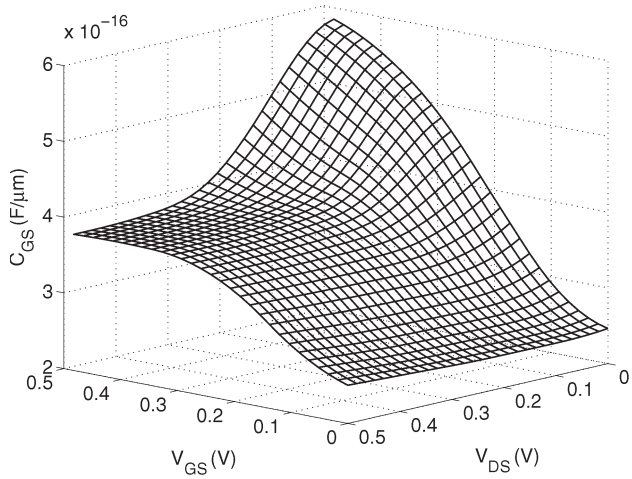

Fig. 7. C_{GS} surface over a full range of V_{DS} and V_{GS} bias, i.e., calculated using a Schrödinger–Poisson simulator combined with Synopsys Sentaurus Device CAD toolbox. Evident in the figure is the transition from subthreshold with smaller C_{GS} to above threshold where the C_{GS} flattens. In addition, the effect of V_{DS} on the capacitance is shown with lower capacitance at high V_{DS}.

increasing the failure rates for the same technology node. Although low-power circuits might be more immune to thermal fluctuations because of their cooler operating temperatures, lower V_{DD}results in fewer electrons on the node capacitors and smaller $I_{\rm on}/I_{\rm off}$ ratios, making soft errors more likely. For this reason, as Fig. 6 suggests, devices with $W/L_G = 2$ operated at $V_{DD} < 0.4$ V are prone to soft errors, with FITs on the order of $\sim 10^{-6}$ for devices with some threshold variation, whereas the same devices at $V_{DD} < 0.3$ V become essentially inoperable, having FITs greater than unity in both cases.

A. Modeling Voltage-Dependent Node Capacitors

In previous sections, the node capacitors have been taken as constant. However, the Markov queueing model is capable of reflecting detailed technology-dependent characteristics, such as the dependence of the gate capacitance C_{GS} on both V_{GS} and V_{DS}. To this end, the Q–V relation for a single MOSFET was calculated using our Schrödinger–Poisson solver over a full range of V_{GS} and V_{DS} values preceded by a calibration based on the results of the Synopsys Sentaurus Device [15] for the same DG-MOSFET geometry, accounting for the overlap and fringing parasitics, given the idealized geometry of Fig. 1. The $C_{GS} = \partial Q/\partial V_{GS}$ resulting from the Q–V surface is plotted in Fig. 7 over a full-range gate and drain bias. As expected, the capacitance increases when moving from subthreshold to above threshold. In addition, reflected in the figure is the effect of high V_{DS} values on C_{GS}, i.e., the characteristic of a short-channel effect in the ultrashort $L_G = 10$ nm device.

After appropriately summing up the Q–V surfaces for the two CMOSFETs and arriving at the Q–V relation for the two inverters as a function of node capacitor voltages V_{C1} and V_{C2}, the 2-D functions $Q_{C1}(V_{C1}, V_{C2})$ and $Q_{C2}(V_{C1}, V_{C2})$ can be systematically inverted, yielding two functions $V_{C1}(Q_{C1}, Q_{C2})$ and $V_{C2}(Q_{C1}, Q_{C2})$, where Q_{C1} and Q_{C2} are taken as integer multiples of the elementary charge. The current and the noise values at every state (Q_{C1}, Q_{C2}) are based on the corresponding values of V_{C1} and V_{C2} in that state. Fig. 8 illustrates the result of mapping a square region from the $V_{C1}-V_{C2}$ space into the $Q_{C1}-Q_{C2}$ space. The arbitrarily shaped queue can then be solved for either time to failure or occupation probability (shown in figure), taking into account the exact Q–V relation of the modeled device. The results of any computation on this queue can subsequently be mapped back onto the node-voltage space if desired; an example of which is shown in Fig. 3.

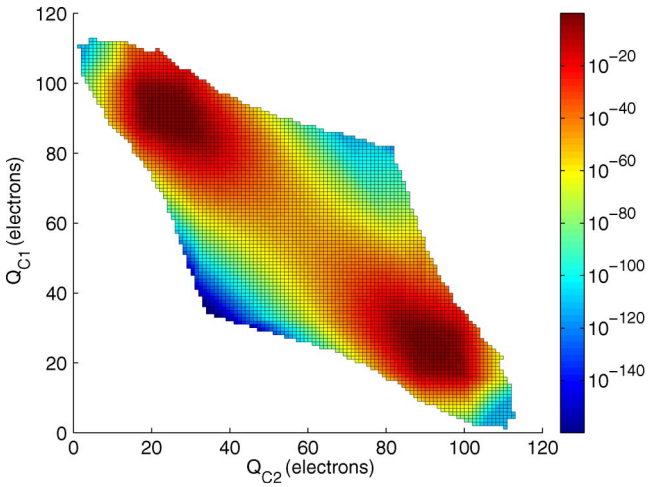

Fig. 8. Result of mapping a square region from the $V_{C1}-V_{C2}$ space into the node charge space $Q_{C1}-Q_{C2}$ by inverting the node charge functions $Q_{C1,C2}(V_{C1,C2})$ corresponding to Fig. 7 into $V_{C1,C2}(Q_{C1,C2})$ and by taking Q_{C1} and Q_{C2} to be integer multiples of the elementary charge. The color scheme shows an example of solving for occupation probability on the resulting arbitrarily shaped 2-D queue. The computed results can be easily mapped back to the node voltage space (see Fig. 3 as an example).

Utilizing the realistic Q–V relation instead of a constant capacitance model changes the failure rates only slightly. For example, for the case of $W/L_G = 2$ and $V_T = 0.15$ V (see Fig. 4), the FIT changes from 2.5×10^{-33} to 2.8×10^{-36}. This is true because the sum of the NMOS and PMOS capacitances is fairly constant, even as the individual transistor capacitances vary, as shown in Fig. 7.

IV. Conclusion and Future Work

Failure rates due to noise in flip-flops made up of ultimate CMOS technology were examined using the numerical framework based on Markov queueing theory and nonequilibrium Green's functions introduced in Part I of this paper [2]. Exploiting the ability of the model to account for specific technology-dependent characteristics, the effects of parameters such as the transistor width-to-length ratio, operating temperature, V_{DD} and threshold voltage variation, on the noise-induced error rates have been investigated. While wider transistors were found to be more immune to soft errors, and higher temperatures lead to greater error rates due primarily to mechanisms such as reduced subthreshold slopes and larger thermal driven charge oscillation, the most dramatic effect is caused by process-induced variations in the threshold voltage, which increases the failure rate by many orders of magnitude.

FIT, which is defined as the number of errors in one billion device-operation hours, is used in the analysis of the model 10-nm-gate-length technology to provide a comprehensive metric for the reliability of logic circuits with large numbers of devices. The results show that while the errors may be very small for an individual flip-flop, the scale-compounded effect on the overall logic circuit made of ultimate CMOS devices will pose reliability concerns for a given set of operating parameters and performance characteristics.

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