Z^2-FET: A zero-slope switching device with gate-controlled hysteresis

J. Wan,[1a)] C. Le Royer,[2] A. Zaslavsky,[1,3] and S. Cristoloveanu[1]
[1] IMEP-LAHC, INP-Grenoble, Minatec, 3 Parvis Louis Neel, BP 257, 38016 Grenoble, France
[2] CEA, LETI, MINATEC, F-38054 Grenoble, France
[3] School of Engineering, Brown University, Providence, Rhode Island 02912, USA
[a)] Corresponding author: wanj@minatec.inpg.fr

ABSTRACT

We present a novel switching device named Z^2-FET that features *zero* subthreshold swing and *zero* impact ionization. The device is built in fully-depleted silicon-on-insulator (FD-SOI) technology and is demonstrated to switch sharply with the subthreshold slope (SS) < 1 mV/dec and an I_{ON}/I_{OFF} current ratio > 10^{10}. The device further shows large hysteresis in drain current-drain voltage (I_D-V_D) domain with the turn-on voltage (V_{ON}) linearly controlled by gate voltage (V_G). Simulation confirms that the operation of the device is determined by the positive feedback between the flow of carriers and their injection barriers.

INTRODUCTION

Several devices, such as impact ionization metal-oxide-semiconductor (IMOS) [1,2] and tunneling field-effect-transistor (TFET) [3,4], have been proposed to tackle the thermal switching limitations in standard MOSFETs and achieve small SS. However, the IMOS requires high supply voltage V_{DD} and the TFETs demonstrated to date have low I_{ON}. Recently, a novel device, known as the feedback FET (FB-FET), has shown low SS and high I_{ON} [5,6]. The V_{ON} of FB-FET is largely determined by injection barriers due to trapped charge Q_S on the gate spacers, which requires high V_G and V_D and is difficult to control precisely [6]. A switching field effect diode (FED) with two front gates has been used for electrostatic discharge (ESD) protection [7].

In this work, a device with a single front gate built on an FD-SOI substrate is shown to have an extremely small SS and high I_{ON} under small V_{DD}. The operation of our device is understood by TCAD simulation to involve a similar mechanism to the FB-FET and FED except that one of the injection barriers is controlled by V_G instead of Q_S and the other is controlled by either back-gate voltage (V_{BG}) or Q_S, leading to good controllability and scalability with easy fabrication.

DEVICE STRUCTURE AND CHARACTERISTICS

Our device is a forward-biased *pin* diode with the intrinsic channel partially covered by the top gate (length L_G) and the rest uncovered (length L_{IN}), see Fig. 1. The device is fabricated in an FD-SOI process with advanced high-k, metal gate and raised source/drain techniques [4]. The device operates with either $V_{BG} > 0$ or positive surface charge on L_{IN} region, as shown in Fig. 1(a) and (b) respectively. For V_{BG}–operated device, the parameters are T_{ox} = 3nm HfO_2, T_{Si} = 20nm, T_{BOX} = 140nm, L_G = 400nm and L_{IN} = 500nm. The Q_S–operated device has similar dimensions, except that T_{ox} = 6nm SiO_2, L_G = 200nm and L_{IN} = 200nm. The surface charge, with density of 10^{12} cm^{-2}, is introduced by the chemical vapor deposited (CVD) SiO_2 interfacial layer on L_{IN} region.

In transfer characterization, the N^+ doped drain is grounded while the P^+ doped source is positively biased. Figure 2 shows that the device turns on sharply as V_G is swept. For the V_{BG}–operated device, the current increases almost 8 decades within ΔV_G = 1mV, shown in Fig. 2(a). The switch is even sharper for the Q_S–operated device with the I_{ON}/I_{OFF} ratio > 10^{10}, see Fig. 2(b). Figure 3 compares our device with recent IMOS, TFET and FB-FET results, showing higher I_{ON}/I_{OFF} ratio and sharper switching.

Steep switching is also observed in I_D-V_D measurements, where the source is grounded, see Fig. 4. As $|V_D|$ sweeps up from 0, the device switches sharply as $|V_D|$ reaches the ON voltage $|V_{ON}|$, linearly controlled by V_G. The device remains in the ON state as $|V_D|$ is swept down until $|V_D|$ ~ 0.8V, where the device turns off, resulting in a large V_G-controlled hysteresis.

OPERATING PRINCIPLE

Figure 5 shows the simulated I_D-V_D characteristics of the device operating with V_{BG} that are in excellent agreement with the experiments in Fig. 4(a). Including impact ionization into the simulation has no effect (see the V_G = –2V data in Fig. 5).

The surface potential plotted in Fig. 6(a) shows electron and hole injection barriers (V_n and V_p) formed by V_G and V_{BG}, respectively, blocking the carrier flow at low $|V_D|$, in the OFF state. These barriers are eliminated in the ON state (V_D = –2V). Figure 6(b) shows the evolution of V_n, V_p and I_D as a function of $|V_D|$. As $|V_D|$ increases to the clamping voltage ($|V_C|$), the channel is depleted and thus the channel potential is clamped by V_G. Increasing $|V_D|$ beyond $|V_C|$ lowers V_n linearly and causes the injection of electrons from n^+-drain into channel, which then flow to the p^+-source, inducing a potential drop at source junction and lowering the V_p. As $|V_D|$ increases further towards $|V_{ON}|$, the V_p is reduced sufficiently to permit hole injection into the channel, in turn reducing V_n and resulting in positive feedback to sharply turn on the device.

SCALING CAPABILITY

As L_G and L_{IN} scale down, the channel controlled by V_G and Q_S (or V_{BG}) is weakened, and thus the $|V_{ON}|$ decreases, as shown in Fig. 7. Better scaling capability can be achieved in V_{BG}-operated device by using thinner T_{Si}, T_{ox} and T_{Box} to enhance the channel controllability of V_G and V_{BG}. Simulations show that our device can operate down to $L_{IN} = L_G$ = 35nm keeping $|V_{ON}| > 1.5$V with an advanced structure of T_{ox} = 1nm, T_{Si} = 5nm and T_{Box} = 20nm, as shown in Fig. 8.

CONCLUSION

An FD-SOI sharply switching device using positive feedback has been demonstrated with I_{ON}/I_{OFF} > 10^{10} and SS < 1mV/dec, unmatched by IMOS, TFET and FB-FET. The device also possesses hysteresis with the V_{ON} linearly controlled by V_G. Our simulations demonstrate that the Z^2-FET can scale down to 35nm. Other advantages are: single front gate, undoped channel, no impact ionization or bipolar/thyristor action, and CMOS compatibility.

REFERENCES

[1] K. Gopalakrishnan et al., IEDM Technical Digest, p. 289, 2002.
[2] F. Mayer et al., ESSDERC, p. 303, 2006.
[3] W. Y. Choi et al., IEEE Electron Device Letters, p. 743, 2007.
[4] F. Mayer et al., IEDM Technical Digest, p. 163, 2008
[5] A. Padilla et al., IEDM Technical Digest, p. 171, 2008
[6] C. W. Yeung et al., VLSI Technology symposium, p. 176, 2009
[7] A. A. Salman et al., IEDM Technical Digest, p. 107, 2006

978-1-4577-2084-0/12/$26.00 ©2012 IEEE

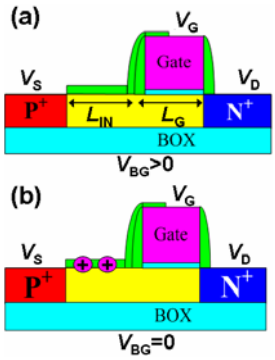


Fig. 1 Schematic view of the structure of Z^2-FETs operating with (a) backgate voltage (V_{BG}) and (b) surface charge (Q_S) on L_{IN} region.

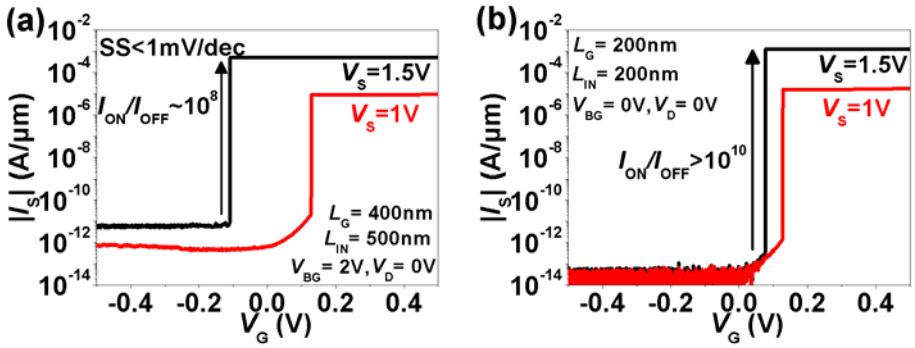


Fig. 2 Experimental I_S-V_G curves of the devices operating with (a) V_{BG} and (b) Q_S, schematically shown in Fig. 1(a) and (b). Note the zero SS in both variants of the Z^2-FET.

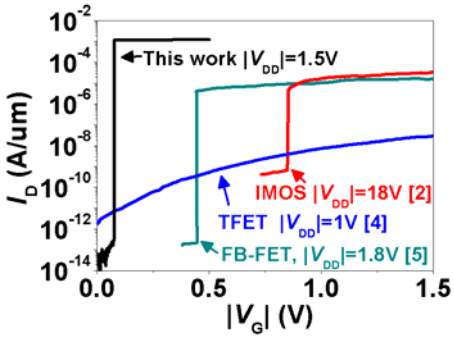


Fig. 3 Comparison between Z^2-FET and other sharp-switching devices.

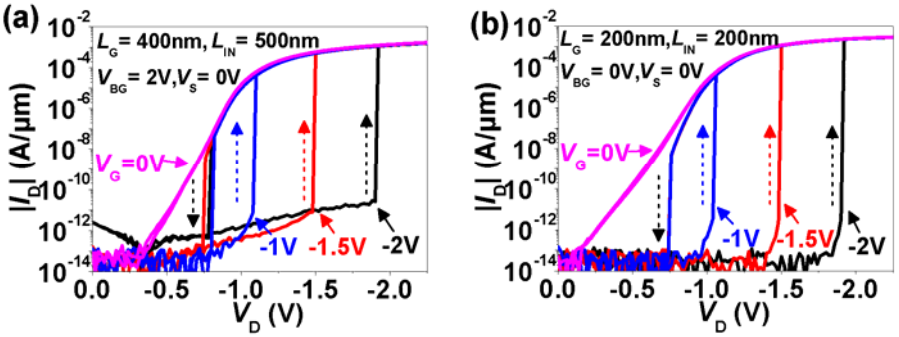


Fig. 4 Experimental I_D-V_D curves of the devices operating with (a) V_{BG} and (b) Q_S, respectively, showing sharp switching and hysteresis, indicated by the dashed arrows.

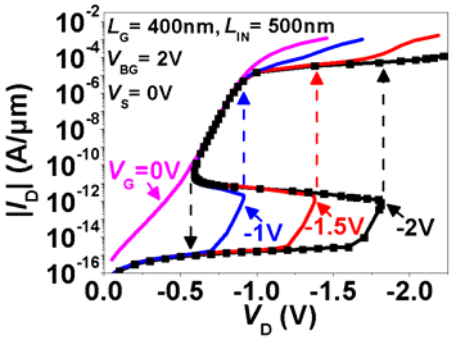


Fig. 5 Simulated I_D–V_D reproduces the experimental data in Fig. 4(a). Dots show the simulation with impact ionization turned on.

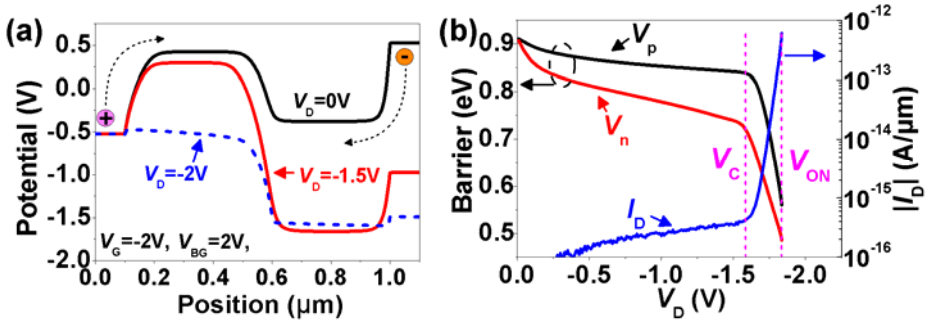


Fig. 6 (a) Simulated surface potential of the device under different V_D, showing that the carrier injection barriers under low $|V_D|$ is eliminated at V_D= –2V. (b) The evolution of the V_n and V_p as $|V_D|$ increases.

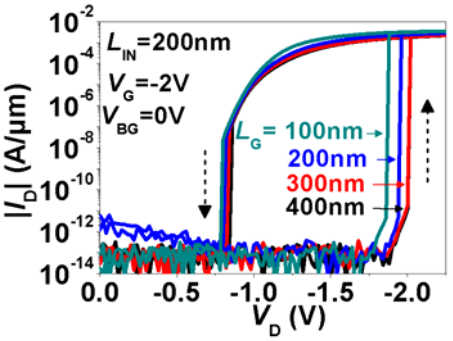


Fig. 7 Experimental I_D-V_D curves for the Q_S-operated devices with different L_G. The $|V_{ON}|$ decreases slightly as $L_G \leq$ 300nm.

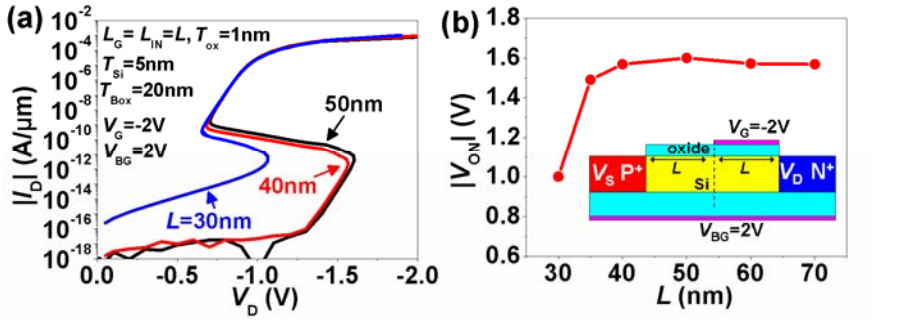


Fig. 8 Simulation is conducted to study the scaling capability of V_{BG}-operated Z^2-FET. Note that L_G = L_{IN} = L. (a) The simulated I_D-V_D curves show that the $|V_{ON}|$ is not affected by L until it decreases to 30nm. (b) The dependence of $|V_{ON}|$ on L reveals that the device can be scaled down to 35nm keeping the $|V_{ON}| > 1.5$V. The inset shows the simplified device structure used in simulation.

PBTI Characteristics of N-Channel Tunneling Field Effect Transistor with HfO_2 Gate Dielectric: New Insights and Physical Model

Genquan Han,[1] Yue Yang,[1] Pengfei Guo,[1] Chunlei Zhan,[1] Kain Lu Low,[1] Kian Hui Goh,[1] Bin Liu,[1] Eng-Huat Toh,[2] and Yee-Chia Yeo.[1]

[1]Dept. of Electrical and Computer Engineering, National University of Singapore (NUS), Singapore 117576.
[2]GLOBALFOUNDRIES Singapore Pte. Ltd., 60 Woodlands Industrial Park D Street 2, Singapore 738406.

Phone: +65 6516-2298, Fax: +65 6779-1103, E-mail: yeo@ieee.org

Abstract

We report the first comparison study of BTI characteristics of nTFET and nMOSFET with the same high-k/metal gate stack fabricated on the same wafer. NTFETs demonstrate smaller ΔV_{TH} and G_m loss in comparison with the nMOSFET under the same PBTI stress. We speculate that the trapped electrons density in HfO_2 gate dielectric above the tunnel junction (TJ) is lower than that above the channel, which leads to the superior PBTI characteristics in nTFET.

I. Introduction

Tunneling Field-Effect Transistor (TFET) is a promising device that enables supply voltage scaling below 0.5 V for ultra-low power logic applications [1]. There are few reliability studies, such as Bias Temperature Instability (BTI), performed on TFETs [2]. Moreover, all reported TFET BTI studies are based on SiON gate dielectric. To achieve good TFET performance, ultrathin equivalent oxide thickness (EOT) or high-k gate dielectric is required. Thus, BTI studies on TFETs with advanced gate dielectrics need to be done. In addition, a direct reliability comparison of TFETs and MOSFETs fabricated using the same process flow or on the same wafer has not been done.

In this paper, we report the first PBTI study of n-channel TFETs (*n*TFETs) with HfO_2 gate dielectric, and also report the first comparison of BTI characteristics of *n*TFETs and *n*MOSFETs fabricated on the same wafer. ΔV_{TH}, and G_m of TFET during and after stress are examined. New insights and physics behind the observed experimental results are discussed here.

II. Key Differences between *n*TFET and *n*MOSFET

In *n*MOSFETs under PBTI stress, electrons undergo direct tunneling from the inversion layer to traps distributed in the gate dielectric [3]-[8].

An *n*TFET [Fig. 1(a)] has a peak vertical electric field E_Y at TJ under positive gate bias V_{GS} [Fig. 1(b)]. Ref. 2 asserts that this potentially leads to larger PBTI degradation or threshold voltage shift ΔV_{TH} than *n*MOSFET.

However, it is pointed out here that although $|E_Y|$ is high near the TJ of *n*TFET, the inversion charge density Q_{inv} at the TJ is much lower than that in the channel [Fig. 1(b)]. It is hypothesized that the density of trapped electrons in the gate dielectric above TJ (n_{TJ}) may be different from that above the channel region (n_0) [Fig. 1(c)]. This could lead to a different PBTI behavior for *n*TFET as compared to *n*MOSFET.

III. Impact of trapped electrons near Tunneling Junction

We simulated nMOSFETs with no trapped electrons (fresh) and with a density n_0 of trapped electrons uniformly distributed in the gate dielectric [see I_{DS}-V_{GS} in Fig. 2(a)]. A similar simulation was done for nTFET, where the effect of a non-uniform trapped electron density is examined: n_0 is fixed and n_{TJ} (near the TJ) is varied. ΔV_{TH} is shown to be dependent on n_{TJ}. If $n_{TJ} < n_0$, nTFET has smaller ΔV_{TH} compared to nMOSFET; otherwise, nTFET has a larger ΔV_{TH} [Fig. 2(b)].

IV. Experimental Results and Discussion

We fabricated both nTFET and nMOSFET on the same wafer and using the same gate stack. Fig. 3 illustrates the nTFET and nMOSFET structures made. Fig. 4 shows the electrical characteristics of a typical nTFET. All devices used in this work have a L_G/W of 10 μm/400 μm.

I_{DS}-V_{GS} of a pair of long-channel nTFET and nMOSFET was measured before and after 1000 s PBTI stress at 2.0 V (Fig. 5). The I_{DS}-V_{GS} shift or ΔV_{TH} due to PBTI is lower for nTFET than nMOSFET. This is true for various PBTI stress voltages (Fig. 6).

Measured C_{inv}-V_G curves (Fig. 7) show that the inversion capacitance densities for nTFET and nMOSFET are the same. Q_{inv} is comparable for both devices. For L_G = 10 μm, the impact of the narrow TJ region (several nm from the source) on C_{inv} is negligible. For a given PBTI V_G stress or V_{Stress}, Q_{inv} and the vertical field in the gate dielectric over a large of the channel region is the same for nTFET and nMOSFET. Thus, it is expected that trapped electron density in HfO_2 over the channel region n_0 would be the same for nTFET and nMOSFET. ΔV_{TH} for nTFET is dependent on both n_0 and n_{TJ}.

To explain the differences in the ΔV_{TH}, it is hypothesized that n_{TJ} is lower than n_0 for the nTFET. ΔV_{TH} evolution in stress phase and recovery phase is shown in Fig. 8. Initial recovery of ΔV_{TH} for nTFET is lower than that of nMOSFET. As shown in Fig. 9, ΔV_{TH} versus time plot shows power law dependence for both devices. The power law slopes range from 0.17 to 0.24. Based on E_{ox} power law model, nTFETs achieve a longer lifetime at all V_{Stress} compared to nMOSFETs (Fig. 10). Fig. 11 shows the G_m degradation before and after PBTI stress at 2.0 V. Compared to nMOSFET, negligible or smaller G_m degradation is observed for nTFET. This is true at all V_{Stress} (Fig. 12). It should be noted that for some nTFETs, maximum G_m increased after the PBTI stress at 1.5 V, unlike nMOSFETs in which G_m is degraded after PBTI stresses. This observation has not been reported before.

V. Conclusions

It is observed that *n*TFETs with HfO_2 gate dielectric demonstrate reduced ΔV_{TH}, longer lifetime, and smaller G_m degradation as compared with *n*MOSFETs under the same PBTI stress. The PBTI characteristics of *n*TFET are explained in terms of the non-uniform distribution of trapped electrons in HfO_2. The density of trapped electrons in HfO_2 gate dielectric above the TJ is likely to be lower than that above the channel.

References

[1] C. Hu *et al.*, *IEDM*, pp. 387, 2010.
[2] G. F. Jiao *et al.*, *IEDM*, pp. 741, 2009.
[3] A. Kerber *et al.*, *IEEE TDMR*, vol. 9, pp. 147, 2009.
[4] S. Pae *et al.*, *IRPS*, pp. 352, 2008.
[5] X. Garros *et al.*, *IEDM*, p. 4.6.1, 2010.
[6] Z. Y. Liu *et al.*, *IRPS*, pp. 733, 2008.
[7] D. P. Ioannou *et al.*, *IRPS*, pp. 1044, 2010.
[8] C. D. Young *et al.*, *IRPS*, pp. 75, 2005.

978-1-4577-2084-0/12/$26.00 ©2012 IEEE

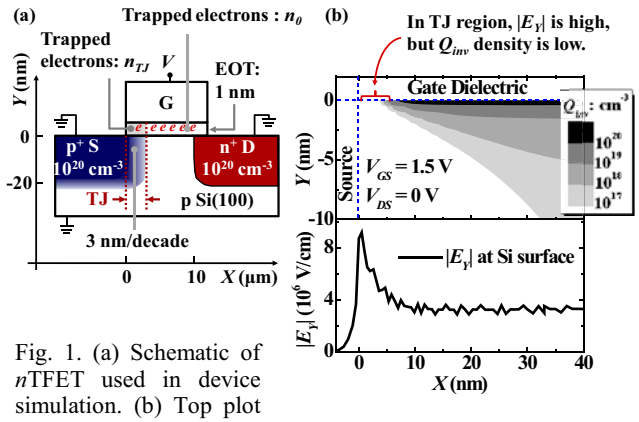
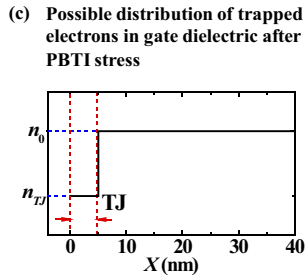


Fig. 1. (a) Schematic of *n*TFET used in device simulation. (b) Top plot depicts inversion charge density Q_{inv} contour, and bottom plot illustrates the magnitude of vertical electric field $|E_Y|$ at Si surface along source to channel direction at V_{GS} = 1.5 V. In the tunneling junction (TJ) region, $|E_Y|$ is high but Q_{inv} is low. At a PBTI stress, density of trapped electrons in the gate dielectric above channel region is assumed to be n_0, and that above TJ is a variable n_{TJ}, as shown in (c). For *n*MOSFET, at a same PBTI stress, trapped electrons with a density of n_0 distribute uniformly in gate dielectric.



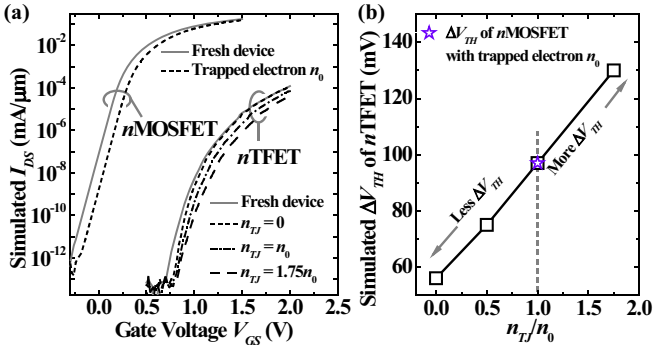


Fig. 2. (a) Simulated I_{DS}-V_{GS} curves of *n*MOSFET and *n*TFET with and without trapped electrons. Trapped electrons in HfO_2 above TJ have a large impact on ΔV_{TH} of *n*TFET. (b) If $n_{TJ} < n_0$, *n*TFET has smaller ΔV_{TH} compared to *n*MOSFET. Otherwise *n*TFET has larger ΔV_{TH}.

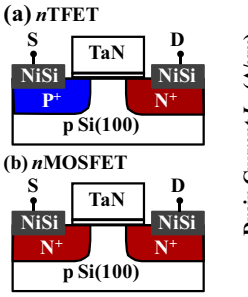


Fig. 3. Schematics of (a) *n*TFET and (b) *n*MOSFET.

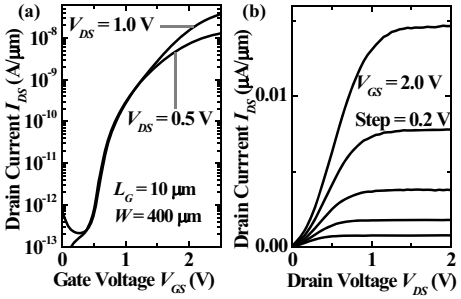


Fig. 4. (a) Measured I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} curves of a typical *n*TFET. All devices used in this study have a L_G/W of 10 μm/400 μm.

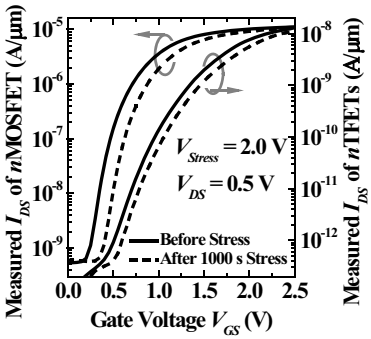


Fig. 5. Measured I_{DS}-V_{GS} curves of a pair of *n*TFET and *n*MOSFET before and after PBTI stress at 2.0 V. *n*TFET has a smaller threshold voltage shift after the PBTI stress compared to *n*MOSFET.

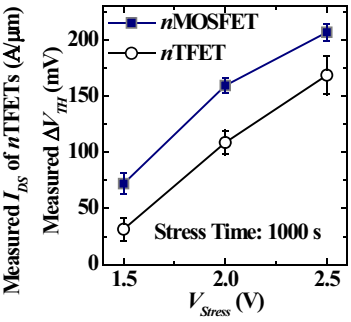


Fig. 6. ΔV_{TH} of *n*TFETs and *n*MOSFETs at different PBTI stresses. V_{TH} of *n*TFET and *n*MOSFET is extracted for V_{GS} at I_{DS} = 1 nA/μm and 1 μA/μm, respectively, measured at V_{DS} = 0.5 V.

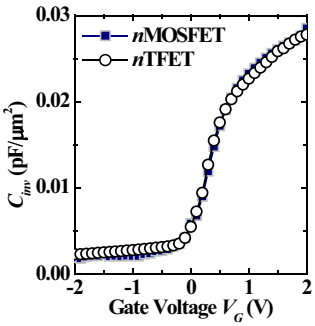


Fig. 7. Measured C_{inv}-V_G curves of a pair of fresh *n*TFET and *n*MOSFET. The impact of the narrow TJ region (several nm) on *n*TFET C_{inv} is negligible. For a given V_G, *n*TFET and *n*MOSFET have the same Q_{inv} and the same vertical field in HfO_2 above the channel region.

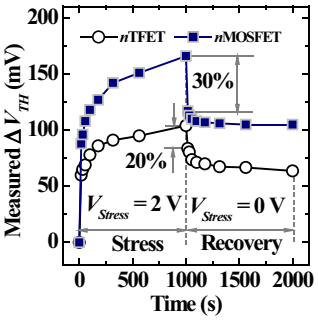


Fig. 8. ΔV_{TH} evolution in stress phase and recovery phase. An initial recovery in the first 18 seconds of *n*TFET is 20%, which is lower than that of *n*MOSFET.

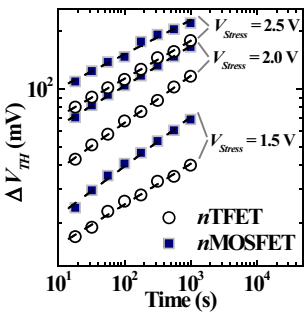


Fig. 9. ΔV_{TH} versus stress time characteristics for *n*TFETs and *n*MOSFETs at different PBTI stresses, showing a power law dependence.

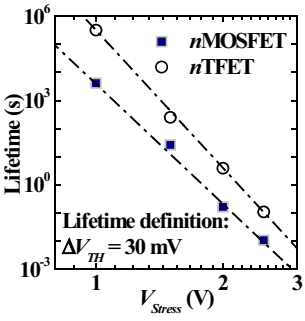


Fig. 10. PBTI lifetime projection of *n*TFET and *n*MOSFET, showing that *n*TFET has a longer lifetime than *n*MOSFET at all PBTI stresses.

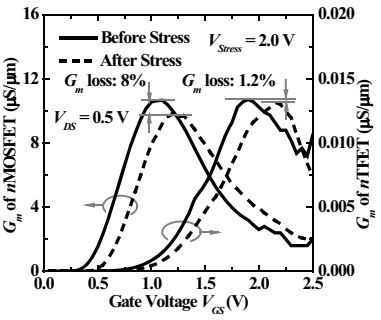


Fig. 11. G_m-V_{GS} curves of *n*TFET and *n*MOSFET before and after PBTI stress at 2.0 V. The data were obtained from the curves shown in Fig. 5.

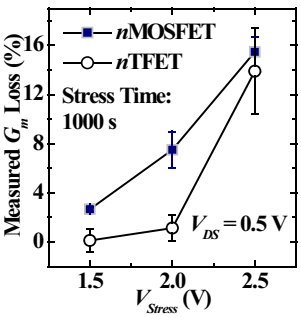


Fig. 12. *n*TFETs demonstrate less degradation of peak G_m as compared to *n*MOSFET at all PBTI stresses. The data were obtained at V_{DS} = 0.5 V.