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Innovative Sharp-Switching Devices

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Two families of sharp-switching SOI devices are discussed: tunneling field-effect transistors (TFETs) and band-modulation feedback transistors. The TFET is a reverse-biased *PIN* gated diode, where the gate voltage controls the electric field in the interband P^+/N^+ tunneling junction. Although the TFET current can in principle be switched faster than the subthreshold current of a MOSFET, experimental results have been disappointing to date. Several technological solutions for improving the I_{ON} current and subthreshold swing are reviewed. An innovative solution is to integrate a TFET with a bipolar transistor in a single device (BET-FET), where the bipolar current gain serves to amplify the tunneling current. A different approach is to use band modulation and feedback. The Z^2-FET has a TFET-like *PIN* configuration but is operated in forward bias. In the off-state, the diode current is blocked by electrostatic gate-controlled barriers. When the gate bias reaches a turn-on value, the device switches abruptly (< 1 mV/decade) to a high I_{ON}. We discuss the physical mechanism and unchallenged performance of the Z^2-FET, and propose several CMOS-compatible applications, such as 1T-DRAM and SRAM, chemical sensors, logic and protection circuits.

Introduction

In MOSFETs, the subthreshold swing (*SS*) is unscalable, being limited by Fermi-Dirac carrier statistics to 60 mV/decade of current at room temperature. Only fully depleted (FD) transistors (planar FDSOI, FinFETs or nanowire FETs) can reach this minimum swing, which is still insufficient for very low operating voltage (below 0.5 V). The *SS* parameter governs the off current (*i.e.,* leakage power) and operating voltage (*i.e.,* dynamic power). Sharper switching devices would enable the CMOS circuits to expand their capabilities with respect to scaling and power reduction.

There has been a recent trend to explore transistors based on alternative principles: tunneling FETs (TFETs) and feedback FETs. We review their performance, physics, and CMOS compatibility. In Section 2, the current status of SOI-based TFETs is presented. Section 3 introduces a more recent transistor (BET-FET), which combines the TFET with a heterojunction bipolar transistor to amplify the tunneling current. A different device (Z^2-FET) uses band modulation and positive feedback. The Z^2-FET has impressive characteristics (abrupt switching, low leakage, high I_{ON}, gate-controlled hysteresis) described in Section 4. Typical applications include capacitor-less DRAM and 1T-SRAM memories, fast logic, sensing, and ESD protection.

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Tunneling FET

The TFET is a gate-controlled reverse-biased *PIN* diode ($V_D > 0$) illustrated in Fig. 1(a). At $V_G = 0$, no band-to-band tunneling (BTBT) occurs between the valence and conduction bands because the source (P^+) and drain (N^+) terminals are far apart, separated by the fully depleted body. In the thin and undoped SOI body, the leakage current is very low. For positive V_G, the electron inversion layer starts forming under the gate. This field-effect-induced N^+ region acts as an extended drain terminal and BTBT is triggered at the source-channel P^+/N^+ junction near the source corner of the gate. The tunneling current I_{ON}, exponentially dependent on the junction field, increases with V_G. Since the BTBT is not limited by the carrier diffusion as in a MOSFET, there is a limited bias range where $SS < 60$ mV/decade. As tunneling occurs in a narrow localized region, the TFET has in theory superior short-channel immunity compared to a MOSFET.

Several variants of SOI TFETs have been fabricated (1–4) but, in general, the I_{ON} has been modest, 3–5 decades lower than in MOSFETs (Fig. 1(b)). A sharp swing was observed only in a limited bias range due to the low BTBT rate. For example, Mayer *et al.* reported $I_{ON} = 1$ µA/µm and $SS = 42$ mV/decade over 2 decades of current (4).

The characteristics of typical TFETs, as in Fig. 1(a), are 'symmetric' for positive and negative gate bias. For $V_G < 0$, holes accumulate in the body and the BTBT is transferred to the drain-channel junction, resulting in a detrimental leakage current. This issue of ambipolar tunneling is solved with asymmetrical architectures: different doping concentrations in source and drain, lateral heterojunctions or asymmetric strain (5–10). A practical solution is to design a gate underlap on the drain side, see L_{IN} in Fig. 2(a) (9). For $V_G > 0$ (on-state), BTBT still occurs at the source-channel junction. The maximum field is hardly affected by the presence of the intrinsic region L_{IN}, where the potential drop is negligible. In contrast, for $V_G < 0$ (off-state), tunneling at the drain side is strongly reduced by L_{IN} and totally suppressed for $L_{IN} = 50$ nm (Fig. 2(b)).

In order to increase the I_{ON} tunneling current, the area of the tunneling junction may be enlarged. An interesting idea is to extend virtually the source and drain regions into the body. In Fig. 1(a), a positive gate bias induces a surface electron channel, while a

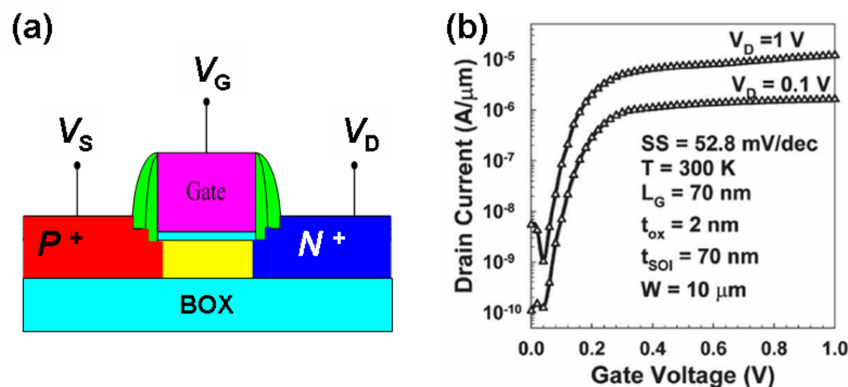

Figure 1. (a) Schematics of *N*-type TFET on SOI and (b) transfer characteristics reported by Choi *et al.* (3).

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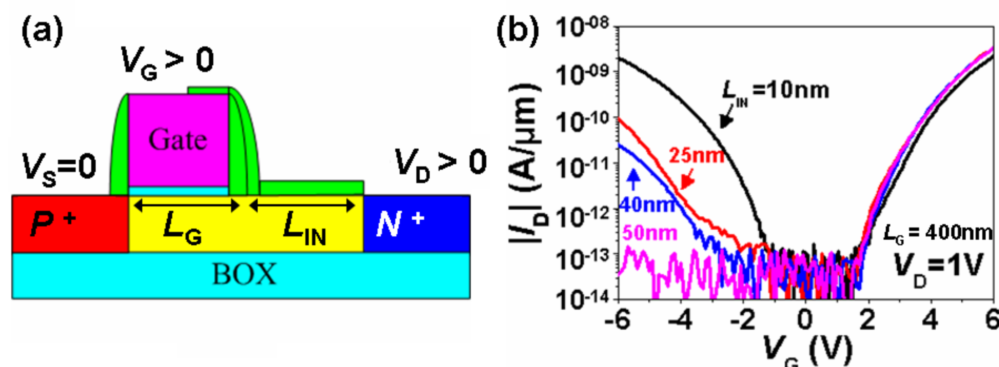

Figure 2. (a) Asymmetric N-type SOI TFET with undoped L_{IN} spacer on the drain side and (b) transfer characteristics demonstrating the suppression of the leakage current by increasing L_{IN} (9).

negative back-gate bias accommodates holes in the back channel. Then, BTBT is expected to occur in the vertical P^+/N^+ quasi-junction, which covers the entire body area, replacing the narrow source-body junction (11). Interband tunneling requires the field-induced P^+ and N^+ layers to be very close to each other, which implies an ultrathin film. Unfortunately, our measurements cast doubt on this attractive concept because the super-coupling effect prohibits the formation of electron and hole channels facing each other in sub-10-nm thick films for reasonable front/back gate voltages (12).

Another solution for high I_{ON} is to shift from Si to narrower gap semiconductors (SiGe, Ge) where the tunneling rate increases exponentially (13,14). The Ge content can be locally enriched in SGOI by the condensation technique, producing 100% GeOI islands. Increased tunneling rate and I_{ON} current were demonstrated in planar GeOI TFETs (6,14) and Ge nanowires (10,15–17). At the same time, high-κ dielectrics reduce the effective oxide thickness, which enables a stronger effective field at the tunneling junction. SOI TFETs with HfO_2 gate oxide exhibit much higher I_{ON} and reduced SS compared to SiO_2-based devices (9).

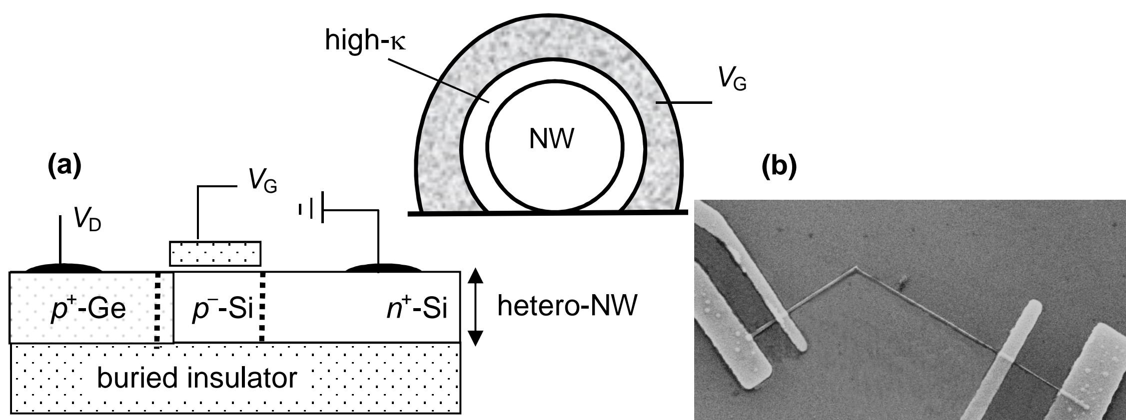

Figure 3. Ge/Si heteronanowire TFET with 50 nm diameter; dashed lines indicate planes of maximum field in Ge (on-state) and in Si (off-state). The gate wraps around the hetero-NW on three sides. (b) SEM image. Inset shows a schematic of the gated NW cross-section [after Zaslavsky *et al*. (18)].

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A heterostructure TFET has the tunneling junction in the lower bandgap material when the device is turned on and in the wider bandgap material when the device is off. Figure 3 shows a Si/Ge heteronanowire TFET with 50 nm diameter and trigate geometry. At $V_G > 0$, the P^- Si body is inverted, creating a tunneling junction in the P^+ Ge section on the drain side of the gate. Conversely, at $V_G = 0$, the tunneling junction is shifted to the source side of the gate and for the same V_D the maximum field occurs in Si, where BTBT is strongly attenuated. Measurements indicate very low leakage current (20 pA/μm), high I_{ON}/I_{OFF} ratio (10^5), and 140 mV/decade average subthreshold swing (with $SS < 60$ mV/decade over 2 orders of magnitude in current) (18).

Record I_{ON} was recently measured in TFETs fabricated with advanced technology modules: high-κ dielectric, metal gate and raised SiGe source/drain terminals. The device featured 5-nm-thick channel stack (Si cap, strained SiGe and Si) where tunneling is enhanced. Figure 4 shows impressive $I_{ON} = 0.4$ mA/μm in *P*-TFET and 0.04 mA/μm in *N*-TFET (19). The subthreshold swing is still too high (> 100 mV/decade) and requires further optimization.

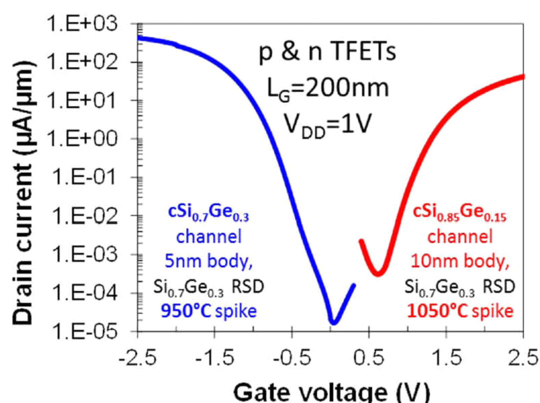

Figure 4. Transfer characteristics of *N*-type and *P*-type TFETs featuring high I_{ON} current [after Villalon *et al*. (19)].

Since none of the TFETs fabricated so far exhibited high I_{ON} and sub-60 mV/dec swing simultaneously, the question is whether BTBT is the primary mechanism. Our low-temperature measurements show weak temperature dependence of characteristics and corroborate the tunneling model (16). Further confirmation was obtained from low-frequency noise measurements. In MOSFETs, the carrier trapping by slow oxide traps results in $1/f$ noise. Only a few slow traps exist in ultra-small MOSFETs, so the $1/f$ noise transforms into random telegraph noise (RTN) with $1/f^2$ Lorentzian spectrum. The noise signature is completely different in TFETs, where $1/f^2$ spectra and RTN signals with discrete trapping-detrapping events are observed even in large devices (20). Only the tunneling junction, which is much shorter (~10 nm) than the gate length and contains just a discrete numbers of traps, acts as the noise-generating area (similar to a very small MOSFET).

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Bipolar-enhanced TFET

Since the tunneling current is modest, why not try to amplify it? This question has led to a new member in the TFET family. The bipolar-enhanced TFET (BET-FET) is a gate-controlled TFET combined, in a single device, with a $Si/Si_{1-x}Ge_x$ heterojunction bipolar transistor (HBT) (21). When the TFET is turned on by V_G, the interband tunneling supplies the base current to the HBT and is multiplied by the bipolar gain β, enabling high I_{ON}.

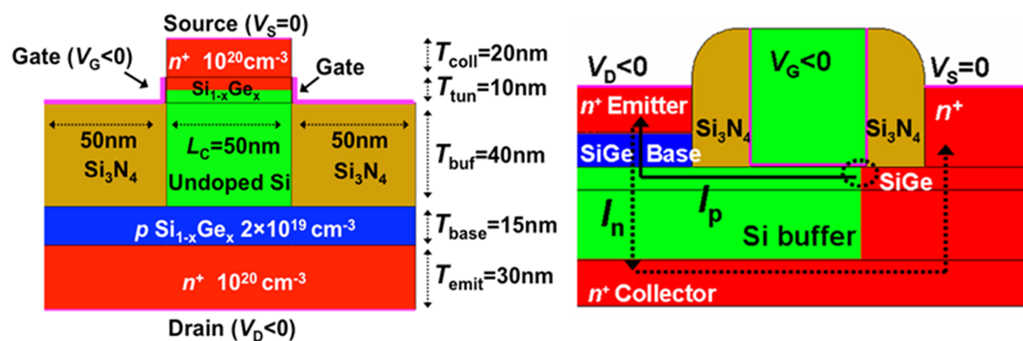

Figure 5. (a) Vertical and (b) planar variants of the BET-FET [after Zaslavsky *et al.* (18)].

In the BET-FET variant shown in Fig. 5(a), the tunneling base current is provided by a gated TFET located in the reverse-biased collector-base junction of an *NPN* $Si/Si_{0.7}Ge_{0.3}$ HBT. When $V_G < 0$ and the TFET is on, the tunneling-generated holes flow to the emitter-base Si/SiGe junction, forward-biasing it and leading to effective electron injection from the emitter. The device has a short sidewall gate close to the source. The source and drain are N^+-Si doped 10^{20} cm^{-3} and used as collector and emitter, respectively. A floating P^+-SiGe layer of 15 nm thickness, doped 2×10^{19} cm^{-3}, is placed above the drain. The vertical N^+-Si source/P^+-SiGe base/N^+-Si drain structure forms an HBT. The source is grounded and $V_D < 0$. The reverse-biased collector-base junction is used as a TFET controlled by the sidewall gates through a 1 nm thick equivalent oxide. The tunneling layer beneath the gate is 10 nm SiGe, of which the upper 5 nm layer is heavily doped. It is separated from the base by a 40-nm-thick undoped Si buffer layer for reducing the ambipolar tunneling leakage, as in optimized asymmetric TFETs of Fig. 2(a). The total thickness of the strained $Si_{0.7}Ge_{0.3}$ layers is 25 nm (21).

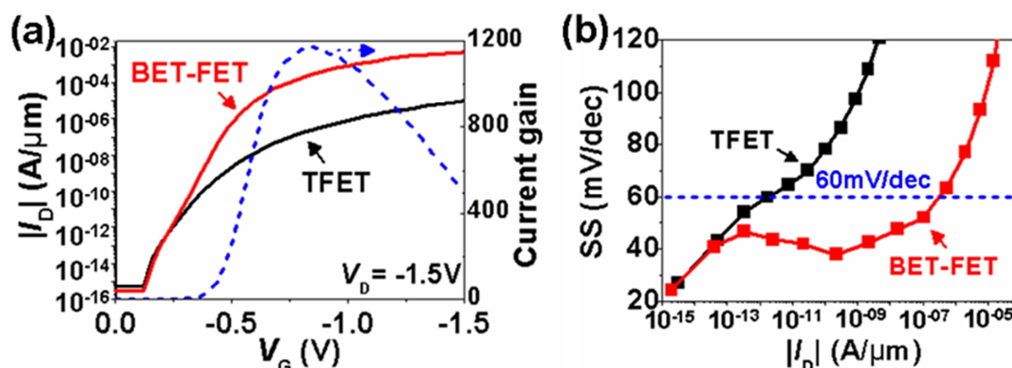

Figure 6. Comparisons of (a) current and (b) *SS* between BET-FET and conventional TFET. Dashed line in (a) denotes the bipolar current gain that enables the superior performance of the BET-FET [after Zaslavsky *et al.* (18)].

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In the off-state (at $V_G = 0$), there is no TFET tunneling current and hence no base current, leading to a negligible emitter-collector current as in a floating-base HBT. At $V_G < 0$, with the TFET current flowing, due to the bipolar amplification, our simulated device shows both high $I_{ON} > 4$ mA/μm (the TFET current multiplied by the HBT current gain $\beta \sim 10^3$) and sub-60 mV/dec swing over a much wider range of current (7 decades) than a standard TFET – see Fig. 6(b). Figure 6(a) compares the $I_D(V_G)$ characteristics of the BET-FET (21) and of a conventional all-Si TFET. The difference due to the bipolar current gain is remarkable. The BET-FET is also scalable down to at least 10 nm source stripe width and the performance can be further improved by enriching the Ge content.

Z^2-FET: Operation Mechanisms and Performance

The feedback-based Z^2-FET, shown in Fig. 7(a), is an astonishing device which features "*zero*" subthreshold swing (< 1 mV/decade) and "*zero*" impact ionization (hence the Z^2) (22). The tremendous switching capability of this compact SOI device outperforms all other sharp-switching devices (23–26). The Z^2-FET is actually a *PIN* diode with undoped channel partially covered by the front gate, exactly as the TFET shown in Fig. 2(a), together with a back gate under the channel. The crucial difference comes from the biasing in forward mode and operation principles. For the *P*-type Z^2-FET, the P^+ source is grounded and the N^+ drain is negatively biased. Nevertheless, the double injection mechanism of the forward *PIN* diode is inhibited by negative bias on the front gate ($V_G < 0$) and positive bias on the back gate ($V_{BG} > 0$). The current is zero because electron and hole injection barriers are formed in the gated and ungated regions of the body.

The $I_D(V_G)$ characteristics feature extremely abrupt switching with 8 decades of current gain in a narrow $\Delta V_G = 1$ mV range, see Fig. 7(b). The switching voltage acts as threshold voltage and can be tuned by adjusting the drain ($V_D < 0$) or source ($V_S > 0$) bias. The output $I_D(V_D)$ curves in Fig. 8(a) show that the device is initially off and switches on sharply as $/V_D/$ increases beyond the turn-on voltage $/V_{ON}/$. As $/V_D/$ sweeps back to 0, the device remains in the high-current on-state until $/V_D/ = 0.8$ V. The hysteresis window is

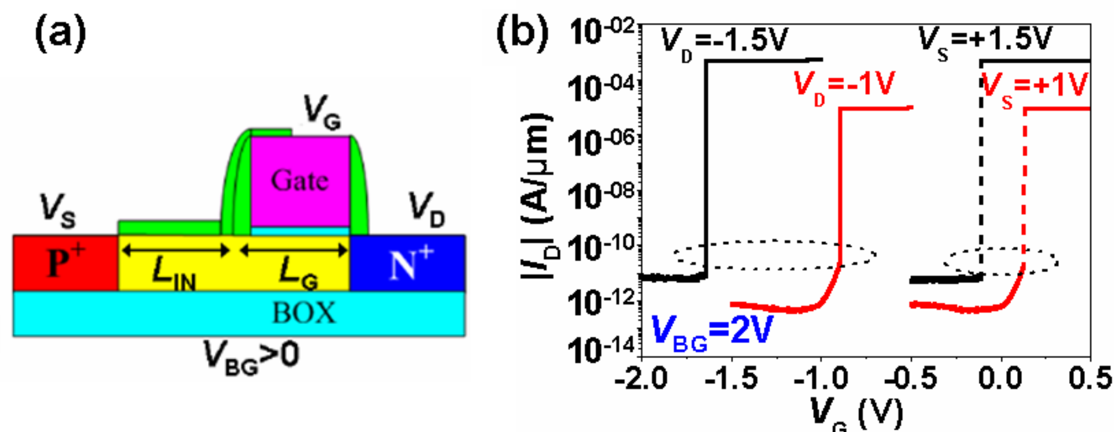

Figure 7. *P*-type Z^2-FET: (a) configuration and (b) experimental transfer characteristics. $V_{BG} = 2$ V, 20 nm thick Si film, 145 nm thick BOX, $L_G = 400$ nm and $L_{IN} = 500$ nm [adapted from Wan *et al.* (22)].

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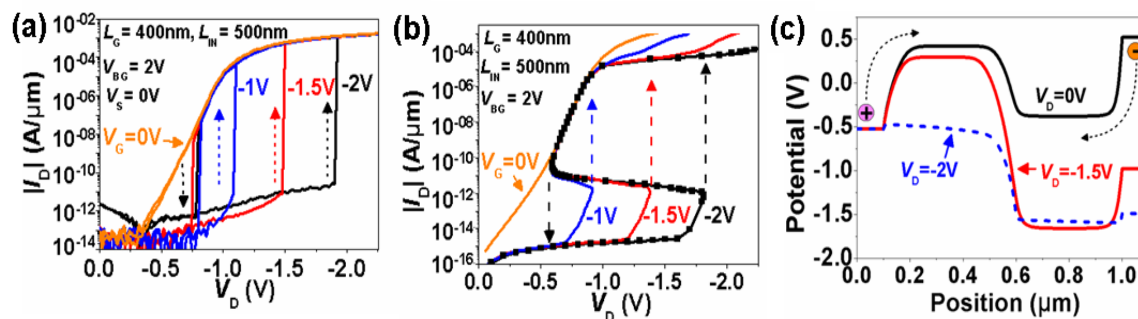

Figure 8. Output characteristics of *P*-type Z^2-FET: (a) experiment; (b) TCAD simulations; (c) evolution of the electron and hole injection barriers with V_D [from Wan *et al.* (22)].

adjustable because V_{ON} is linearly dependent on V_G. The simulated curves in Fig. 8(b) indicate that the $I_D(V_D)$ characteristics are S-type but impact ionization has no effect (dotted curve). Although the gate bias emulates a virtual *PNPN* thyristor-like structure, the Z^2-FET operation principles are different.

The key mechanism is band modulation by injected carriers. Electron and hole barriers are formed by V_G and V_{BG} biases, blocking the carrier flow at low drain bias – see $V_D = -1.5$ V curve in Fig. 8(c). As $/V_D/$ approaches V_{ON}, the drain injection barrier is slightly lowered and enables the injection of a few electrons from the drain into the channel. They flow to the source, where they reduce marginally the hole barrier, permitting the injection of a few holes into the body. The holes flow to the drain, further reducing the electron barrier. This positive feedback suppresses both injection barriers (see $V_D = -2$ V curve in Fig. 8(c)), hence the I_{ON} current reaches the high level of a forward-biased *PIN* diode with double injection.

Other feedback devices use for band modulation two adjacent top gates (25) or surface charge in the gate spacers (26). The Z^2-FET is more compact and simpler because it has a single top gate and uses the thin BOX and ground-plane bias, already available in FDSOI CMOS technology, for generating the second potential barrier. Z^2-FET with 8–10 nm BOX can even be operated without a back-gate bias: the potential difference between the highly-doped ground plane and the intrinsic channel is strong enough to form the barrier in the underlap region. The Z^2-FET is scalable down to at least 20 nm gate length, where sufficiently high injection barriers can still be maintained by using very thin layers (gate oxide, film and BOX). In general, V_{ON} drops if V_G and V_{BG} lose control of the injection barriers in very short gate length devices. Finally, the reliability of both *N*-type and *P*-type Z^2-FETs is very good as shown by high temperature and cycling tests.

In the following, we discuss several straightforward applications.

Capacitorless 1T-DRAM

The Z^2-FET hysteresis is a memory effect, ideal for single-transistor DRAM (1T-DRAM) (27). The idea is to store holes at the front gate by setting $V_G = -1.7$ V, see Fig. 9(a). The detailed biasing sequence for writing and reading the memory is given in Fig. 9(b). The memory is programmed by pulsing V_G to zero. For state '1', a simultaneous drain pulse (V_D from zero to –1.3 V) is applied to turn on the Z^2-FET. This leads to

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carrier injection and some of the holes remain under the front gate when V_G returns to the –1.7 V hold voltage. For state '0', $V_D = 0$ when V_G is pulsed to zero, so no holes are available for storage under the front gate.

The two logic states are read out by short negative pulses on the drain, smaller than V_{ON} (V_D switched from 0 to –1.3 V). The discharge of stored holes through the forward-biased drain triggers the feedback to turn on the device. This results in a high current (~100 μA/μm) defining the '1' state. Instead, for state '0', not only is $|V_D| < |V_{ON}|$ but also there is no discharge current, so the device remains blocked. The difference between '1' and '0' currents is many orders of magnitude, resulting in an excellent memory margin. While state '1' is unconditionally stable, state '0' limits the retention time to about 1 s, due to the gradual recharging of the accumulation layer under the gate via the reverse-biased drain junction. Since the readout sequence automatically refreshes the '0' state by eliminating the parasitic hole charges, frequent reading of the memory extends the retention time to over 5 s.

The Z^2-FET 1T-DRAM has a fundamental advantage compared to other types of SOI 1T-DRAMs (28). The memory state is defined not by the stored charge ΔQ_G but by the transient current $\Delta Q_G/\Delta t$. A relatively small ΔQ_G is sufficient for state discrimination using the internal feedback amplification if the access time is short enough (Δt ~ 1 ns). Fast readout is exactly what memory end-users are always seeking.

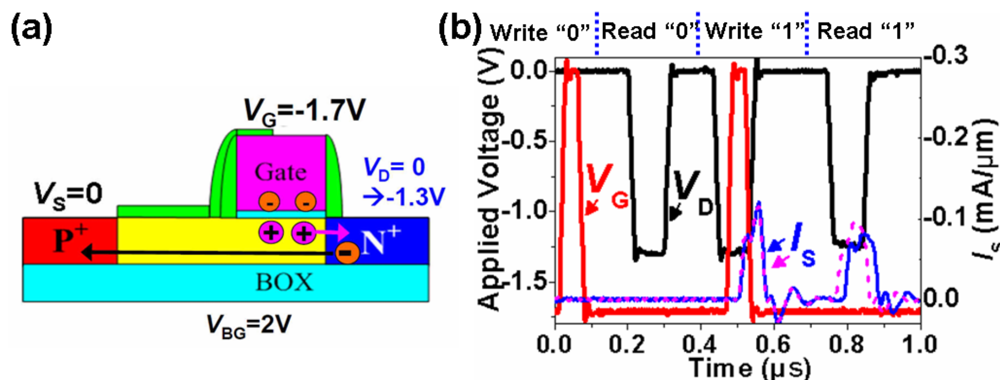

Figure 9. (a) Schematic of the Z^2-FET 1T-DRAM; (b) biasing sequence and read current [adapted from Wan *et al.* (27)].

Single-transistor SRAM

The Z^2-FET can replace static random access memory (SRAM) composed of six transistors. Using the hysteresis in $I_D(V_D)$ domain (Fig. 8(a)), the memory is programmed with $V_G = 0$ and either $V_D = 0$ (logic '0') or $V_D = –2.5$ V (logic '1'). Negligible '0' current and moderate '1' current are achieved in the hold state ($V_G = –1.7$ V and $V_D = –0.9$ V). To further increase the '1' current, the 1T-SRAM memory is read by pulsing V_D to –1.3 V. Logic '0' and '1' have an infinite retention time and are read out correctly after 100 s. The power consumption for holding logic '1' is a disadvantage, which can be mitigated by using a heterojunction device. According to simulations, the static current can be markedly reduced if the channel is made of $Si_{0.7}Ge_{0.3}$ while source/drain regions are Si.

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Logic circuits and ESD protection

The design of fast logic circuits can take advantage of the sharp switching of Z^2-FETs if the hysteresis effect, which prevents prompt turn-off, can be suppressed. The solution is to use gate pulses with very short fall time. Our simulations show that for 1 ns fall time, the current switches from on- to off-state, where the current is 7 orders of magnitude smaller. This means that the Z^2-FET can replace the MOSFET as the building block for logic circuit design, but only for extremely fast V_G switching, which is again what the consumer wants.

The protection of FDSOI circuits against electrostatic discharge (ESD) requires a device with S-type characteristics, low I_{OFF} and fast switching to high I_{ON} at voltages exceeding the nominal supply voltage by 10%. The Z^2-FET meets all these criteria with the additional advantage that the turn-on voltage V_{ON} can be fine-tuned by adjusting the gate bias. The performance of Z^2-FET as an ESD protection device has recently been confirmed in advanced 28 nm FDSOI technology. The ultrathin film (< 10 nm), thin BOX and ground plane enable low-voltage operation (1.5–2 V on both gates) and attractive triggering capability: $I_{OFF} \sim 1$ fA and $V_{ON} > 1.1$ V (29).

Surface-charge sensor

The injection barrier in the gate underlap region can also be formed by replacing the back-gate bias with a positive surface charge Q_S on the ungated region as shown in Fig. 10(a). In our Z^2-FETs, the charge ($Q_S \sim 10^{12}$ cm^{-2}) was induced by the chemical vapor deposition of SiO_2. Measurements show similar $I_D(V_D)$ and $I_D(V_G)$ sharp-switching characteristics as in Figs. 7 and 8 (27). The impact of Q_S density on V_{ON} is simulated in Fig. 10(b). Note the region where V_{ON} varies rapidly with Q_S, before reaching saturation. This sensitivity is promising for sensing charges attached to the surface (liquids, DNA, gold nanoparticles, *etc*.). The Z^2-FET is more flexible than standard ISFETs because the sensitive region can be tuned to match various applications by varying the underlap length (Fig. 10(b)), or by modulating the barriers with V_{BG} and V_G.

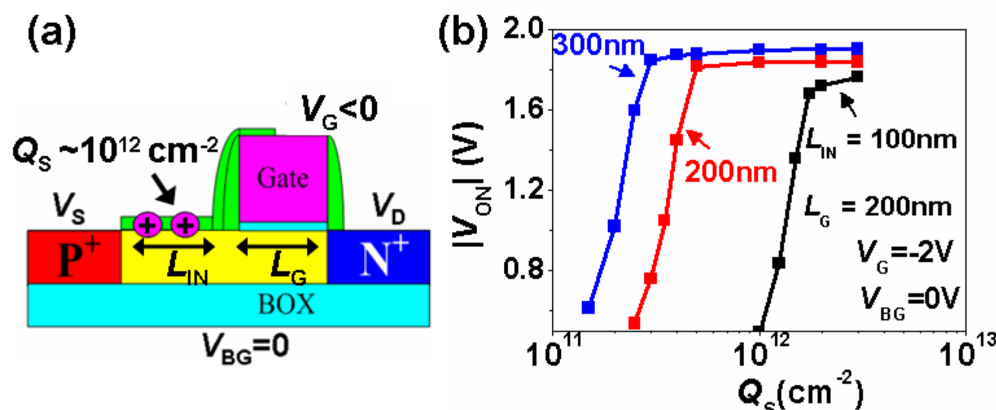

Figure 10. (a) Z^2-FET operated with positive surface charge Q_S ($V_{BG} = 0$, $L_G = 200$ nm). (b) Simulated variation of the turn-on voltage versus surface charge Q_S.

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Conclusions

The context and future trends of tunneling transistors have been discussed. Innovative solutions based on ultrathin films, nanowires, and heterostructures enable increasing the drive current from modest to reasonable values. A more challenging task is to achieve simultaneously sub-60 mV/decade subthreshold swing over a wide range of gate bias. Adding internal bipolar amplification of the tunneling current, as in the recent BET-FET device, is an attractive concept requiring experimental validation.

The best option for super sharp-switching transistors is the feedback band-modulation mechanism. We have reviewed the Z^2-FET configuration and experimental data. The Z^2-FET is compact, scalable and fully compatible with SOI CMOS fabrication. The modulation of injection barriers, created by the front and back gates, results in abrupt switching: near-zero subthreshold swing (< 1mV/decade) and very high I_{ON}/I_{OFF} ratio (> 10^8). The hysteresis in the $I_D(V_D)$ domain is adjustable by gate voltage and useful for high-speed 1T-DRAM with low operating voltage, long retention (seconds), and fast access time (1 ns), as demonstrated by experimental measurements. Other Z^2-FET applications include ESD protection for FDSOI circuits, compact single-transistor SRAM, chemical sensor and high-speed logic circuits.

Acknowledgments

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