Novel Bipolar-Enhanced Tunneling FET With Simulated High On-Current

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***Abstract*—We propose and simulate a new device combining a tunneling field-effect transistor (TFET) with a heterojunction bipolar transistor (HBT). The carriers generated in the tunneling junction are used as base current to drive the HBT and obtain a high bipolar current. Owing to the sharp switching of the TFET and high HBT current gain, the CMOS-compatible Si/$Si_{1-x}Ge_x$ device shows a subthreshold swing of < 60 mV/dec over seven decades of current, a high ON current, and scaling capability down to 10 nm.**

***Index Terms*—Bipolar-enhanced tunneling field-effect transistor (TFET) (BET-FET), FET, heterojunction bipolar transistor (HBT), sharp switch, tunneling.**

I. Introduction

THE tunneling field-effect transistor (FET) (TFET) utilizing band-to-band tunneling (BTBT) has been proposed to tackle the limitations of conventional metal–oxide–semiconductor FETs (MOSFETs) and achieve subthreshold swing (SS) lower than 60 mV/dec at room temperature [1]–[3]. However, the ON-state current $I_{\rm ON}$ of TFETs has been much lower than that of MOSFETs, and the small SS is only obtained over a restricted current range, although materials with low bandgap $(E_{\rm G})$ have been used [2], [4]–[8].

The heterojunction bipolar transistor (HBT) has been widely used as a high-frequency current amplifier [9]. A multi-emitter HBT with an Esaki tunnel diode supplying the base current has been demonstrated previously for enhanced logic functionality [10]. In this letter, we propose a high-performance device named the bipolar-enhanced TFET (BET-FET), where the HBT is combined with a $V_{\rm G}$-controlled tunneling junction. The holes are generated in the collector–base (CB) tunneling junction, operated as a TFET. These holes flow to the base–emitter (BE) junction, leading to high electron injection from the emitter. Our simulated device shows both high $I_{\rm ON}$ and low SS over a much wider range of current than a TFET. The BET-FET has a certain similarity with the insulated-gate bipolar transistor (IGBT) [11] in the sense that they both use a switching device to trigger the bipolar transistor. However, the BET-FET triggered by a TFET has sharper switching and simpler structure than the IGBT.

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II. Structure, Operating Principle, and Performance

The 2-D TCAD simulations are performed with the "Sentaurus" device simulator using the dynamic nonlocal tunneling model for BTBT, where the tunneling rate depends on the band-diagram profile along the tunneling path [12]. Our simulation included Shockley–Read–Hall recombination, doping-dependent bandgap narrowing, and electric field- and doping-dependent mobility models.

Fig. 1(a) shows the simulated vertical BET-FET device structure, which is symmetrical and has a short sidewall gate close to the source. Analogous vertical device structures with either one or two independent sidewall gates have already been implemented in standard MOSFETs and TFETs [7], [8], [13], [14], so the fabrication of the vertical BET-FET should pose no fundamental challenge. Both source and drain are heavily n^+-doped $(10^{20}$ cm$^{-3})$ and used as collector and emitter, respectively. A p^+-type $Si_{1-x}Ge_x$ layer with doping concentration of 2×10^{19} cm^{-3} is placed above the drain and used as the base, albeit without any direct base contact. The vertical n^+ Si source/p^+-$Si_{1-x}Ge_x$ base/n^+ Si drain structure forms an HBT, biased in the conventional way with the source grounded and the drain negatively biased $(V_{\rm D} < 0)$. The reverse-biased CB junction is used as tunneling junction controlled by the sidewall gates through a 1-nm equivalent oxide [4]. The tunneling layer beneath the gate is 10-nm $Si_{1-x}Ge_x$ with 5-nm overlap and separated from the base by an undoped Si buffer layer for reducing the ambipolar tunneling leakage as in a conventional TFET [3].

The operating principle of the BET-FET is shown in Fig. 1(b). In the OFF state, at $V_{\rm G} = 0$, the tunneling gap in the reverse-biased CB junction is large. This suppresses the tunneling current (the HBT base current), leading to negligible emitter-collector current as in a floating-base HBT [10]. In the ON state, at large $|V_{\rm G}|$, the tunneling gap at the CB junction becomes very small [see Fig. 1(c)]. This allows electrons to tunnel to the collector and leaves holes in tunneling region. The hole current $(I_{\rm p})$ flows to the BE junction and forward biases it, like a standard base current. A high electron current $(I_{\rm n})$ is then injected from the emitter into the base and subsequently drifts to the collector as in an HBT [see Fig. 1(b) and (c)]. Note that the hole injection barrier formed by the valence-band offset ($\sim$0.21 eV) at $T_{\rm tun}/T_{\rm buf}$ interface is much lower than the tunneling bandgap ($\sim$0.86 eV). Therefore, the hole current is governed by the tunneling junction. Further, a graded $Si_{1-x}Ge_x$

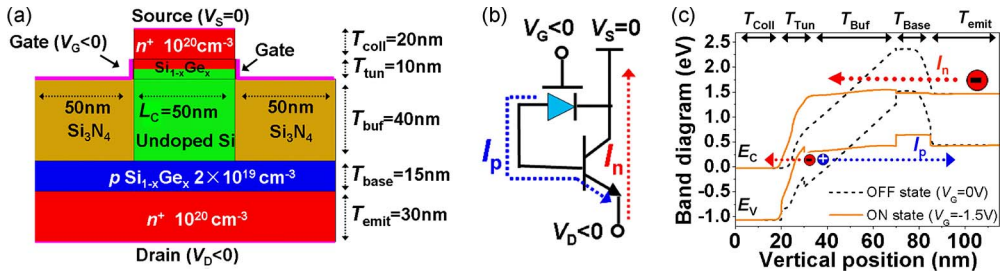

Fig. 1 (a) Simulated device structure has the following layer sequence: n^+-doped Si collector: $T_{\rm coll} = 20$ nm; $Si_{1-x}Ge_x$ tunneling layer: $T_{\rm tun} = 10$ nm of which 5 nm is n^+ doped and 5 nm is undoped; undoped Si buffer layer: $T_{\rm buf} = 40$ nm; p-doped $Si_{1-x}Ge_x$ base: $T_{\rm base} = 15$ nm; and n^+-doped Si emitter: $T_{\rm emit} = 30$ nm. The source stripe width $L_C = 50$ nm. (b) Equivalent circuit of the BET-FET in the ON state; dashed arrows denote hole (I_p) and electron (I_n) currents. (c) Band diagrams along the vertical surface of the device in (dashed curve) OFF and (solid curve) ON states. Arrows denote ON-state electron and hole currents.

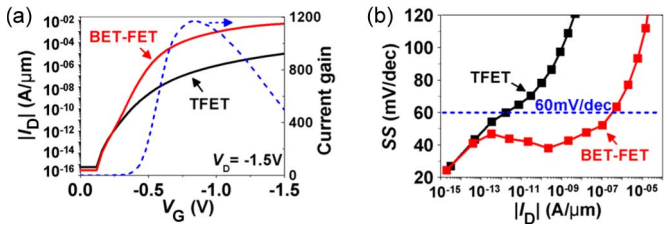

Fig. 2. Comparisons of (a) current and (b) SS between BET-FET and conventional TFET. Dashed line in (a) denotes the bipolar current gain that ensures the superior performance of the BET-FET.

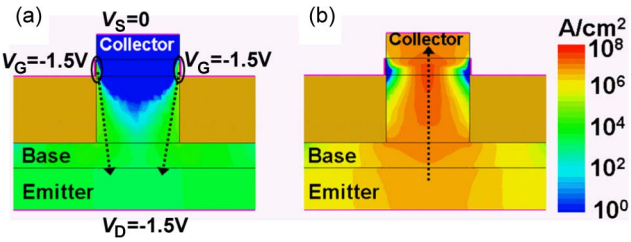

Fig. 3. (a) Hole and (b) electron current densities in the BET-FET biased at $V_D = V_G = -1.5$ V. Dashed arrows show the directions of hole and electron flows.

transition at the $T_{\rm buf}$ boundary can be used to smooth out the hole injection barrier. Bipolar-enhanced tunneling has been studied previously as a leakage-causing effect in silicon-on-insulator MOSFETs [15], but here, it provides a mechanism for a sharp-switching device with high $I_{\rm ON}$—the BET-FET.

Fig. 2(a) shows the I_D–V_G characteristics of the BET-FET at $V_D = -1.5$ V with Ge content $x = 0.3$ in both base and tunneling layer and the gate work-function set to 5 eV. For comparison, a conventional TFET with the same tunnel layer as in Fig. 1(a), but a p^+ Si-doped drain was also simulated. The difference between the BET-FET and the TFET results from the bipolar amplification.

Compared to the conventional TFET, the BET-FET has much higher $I_{\rm ON} > 4$ mA/μm at $V_G = -1.5$ V. The bipolar current gain of BET-FET, referenced to the TFET, is low under low I_D due to the carrier recombination in BE junction and ramps up as I_D increases. The highest current gain is achieved at $I_D \sim 0.1$ mA/μm and then decreases due to high injection, as in a standard HBT [16]. Fig. 2(b) compares the SS values in BET-FET and TFET. As usual, the conventional TFET exhibits SS $<$ 60 mV/dec over a limited two-decade range of I_D, whereas the BET-FET has SS $<$ 60 mV/dec over seven decades of current.

III. Scalability

The carrier flows in the BET-FET biased at $V_D = V_G = -1.5$ V are shown in Fig. 3. The holes are generated by BTBT in the gated $Si_{1-x}Ge_x$ tunneling layer on both sides of the collector stripe L_C and flow to the BE junction, spreading over the entire L_C, as shown in Fig. 3(a).

The electrons are injected over the entire BE junction area, diffuse across $T_{\rm base}$, and then drift through the undoped buffer region to the collector, as shown in Fig. 3(b). Due to the high gain of the Si/$Si_{1-x}Ge_x$ HBT, the electron current density is much higher than the hole density everywhere except near the negatively biased gates.

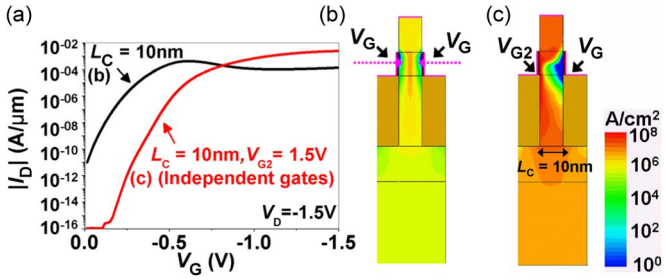

Fig. 4. (a) Comparison of I_D–V_G between scaled $L_C = 10$ nm BET-FETs with and without independent gate control. (b) When the same V_G is applied to both gates, $I_{\rm ON}$ is reduced due to pinchoff of electron current. (c) With independent $V_{G2} = 1.5$ V, electron current is restored, leading to high $I_{\rm ON}$.

The scaling capability of the BET-FET is studied by reducing the collector stripe width L_C from 50 to 10 nm. With $L_C =$ 10 nm, the threshold voltage is markedly reduced, due to the enhancement of electric field at the tunneling junction [see Fig. 4(a)] [17]. However, the current at high $|V_G|$ is also reduced, due to the suppression of electron flow by the $V_G < 0$ V at both sidewall gates [see Fig. 4(b)]. In order to restore the electron flow, a BET-FET with two independent gates is simulated in Fig. 4(c), with the gate voltage V_G ramped from 0 to -1.5 V while $V_{G2} = 1.5$ V. The threshold voltage is increased due to the interchannel coupling effect. The negatively biased V_G provides the BTBT hole base current at one sidewall, while positive V_{G2} restores the electron flow at the other, leading to high $I_{\rm ON}$ even with $L_C = 10$ nm. The fabrication of the two independent gates could use the process as in [13] and [18].

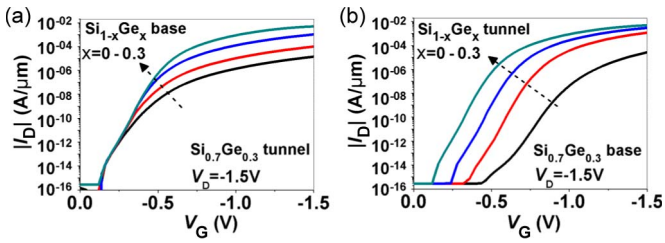

Fig. 5. $I_{\rm D}$–$V_{\rm G}$ of BET-FETs with $L_{\rm C} = 50$ nm versus Ge content x in (a) the base (with $x = 0.3$ in the tunneling layer) and (b) tunneling layer (with $x = 0.3$ in the base).

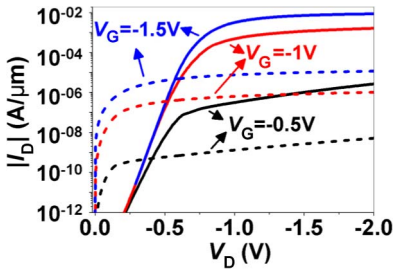

Fig. 6. Comparison of $I_{\rm D}$–$V_{\rm D}$ characteristics between (solid curves) BET-FET and (dashed curves) conventional TFET showing that the BET-FET has higher current at large $|V_{\rm D}|$ and lower current at low $|V_{\rm D}|$.

IV. Discussion

The performance of BET-FET is determined by both the bipolar gain and BTBT current. Fig. 5(a) shows that the increase of x from 0 to 0.3 in the base enhances the current gain and $I_{\rm ON}$. Higher Ge content in the tunneling layer increases the tunneling current and reduces the threshold voltage, owing to lower $E_{\rm G}$, see Fig. 5(b). The TFET current could be further enhanced by increasing the Ge content, but above $x = 0.3$, defect generation due to lattice mismatch may be an issue [19].

Fig. 6 compares the $I_{\rm D}$–$V_{\rm D}$ characteristics of the BET-FET and a conventional vertical TFET with $L_{\rm C} = 50$ nm, showing that the $I_{\rm D}$ in BET-FET is large for $|V_{\rm D}| \geq 0.6$ V but degrades below that, becoming lower than that in a conventional TFET at $|V_{\rm D}| < 0.5$ V. This is due to the fact that the $|V_{\rm D}|$ in a BET-FET needs to be high enough to drive both the reverse-biased tunneling junction and forward-biased BE junction of the HBT. One way to address this issue is to use lower bandgap materials, such as III–V semiconductors [9], which is compatible with the future direction of MOSFET and TFET research.

The operation speed of the BET-FET is expected to be higher than that of a conventional TFET, since it is basically a high-current HBT. The limiting factor for the BET-FET speed will arise from the RC delay of the gate capacitor (same as in a MOSFET).

V. Conclusion

We proposed and simulated a bipolar-enhanced TFET with high $I_{\rm ON}$ of > 4 mA/μm and low SS of < 60 mV/dec in over seven decades of current, which significantly outperforms the conventional TFET. The operation of the BET-FET combines the merits of the TFET's sharp switching with the high-current amplification of an HBT. Although we have focused on CMOS-compatible $Si/Si_{1-x}Ge_x$ materials, the same devices can be built in all of the III–V heterostructures that can sustain a high-gain HBT.

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