Solid-State Electronics 84 (2013) 147–154

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Progress in Z^2-FET 1T-DRAM: Retention time, writing modes, selective array operation, and dual bit storage

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A R T I C L E   I N F O

Article history:
Available online 13 March 2013

Keywords:
Z2-FET
One-transistor DRAM
Capacitor-less DRAM
Retention
Selective array addressing
Dual bit storage

A B S T R A C T

In this paper, we extend our studies on the use of *zero* impact ionization and *zero* subthreshold swing field-effect-transistor (Z^2-FET) as a capacitor-less one-transistor dynamic random access memory (1T-DRAM) through both experiment and TCAD simulation. The data retention time is measured as a function of biasing, temperature and device dimensions, leading to a simple predictive model. An alternative writing method using the source MOSFET is presented, which is potentially more compatible with the conventional DRAM array design. The operation of a Z^2-FET memory array is discussed, in which the write and read signals are adapted from the single cell to achieve selective operation. Finally, we present simulations demonstrating that the Z^2-FET can be used to store multiple bits thanks to the charges on both the top and bottom gate capacitors.

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1. Introduction

The conventional one transistor–one capacitor dynamic random access memory (1T–1C DRAM) has shown good reliability and high integration density for several decades [1]. However, the external capacitor needs to store enough charge to maintain a sufficiently long retention time t_{re}, and thus is not scalable. In order to form this large capacitor, gate-all-around high aspect ratio structures have been adopted, leading to ever greater challenges in fabrication and access speed [1,2].

As a result, the capacitor-less single transistor DRAM (1T-DRAM) is of great interest due to its compact layout that dispenses with the external capacitor [3,4]. A number of demonstrated 1T-DRAMs use the floating body effect, where the stored majority carriers control the flow of minority carriers. Since the electrons and holes need to coexist in the same channel, the scaling of such floating-body memories is limited by the supercoupling effect, which impedes the simultaneous formation of accumulation and inversion layers in the same thin channel [5].

Another interesting 1T memory is based on a thyristor structure (TRAM), which shows reasonable integration density and fast access speed [6,7], but requires precise doping control to obtain stable bipolar characteristics under various temperatures [8]. A related third class of devices is based on the sharp-switching field effect diode (FED) with two front gates, which was originally proposed for electrostatic discharge (ESD) protection [9] and then as a memory device with good simulated scaling capability [9–11].

We previously demonstrated the use of a new feedback device named the Z^2-FET (for *zero* impact ionization and *zero* subthreshold swing field-effect-transistor) [12] as a 1T-DRAM [12–14]. The Z^2-FET has a simple compact layout, with a single front gate and an undoped channel. As reported previously, the Z^2-FET DRAM shows promising performances with supply voltage (V_{DD}) down to 1.1 V, retention time ~5.5 s, simulated access time ~1 ns and non-destructive readout. Here, we present additional experimental and simulation studies on the Z^2-FET DRAM and reveal new and interesting properties. The relations between retention time and drain voltage (V_D), gate voltage (V_G), temperature (T) and gate length (L_G) are studied in detail, leading to a simple predictive model. A different writing method is explored, using the backgate V_{BG}-controlled source MOSFET to charge and discharge the front gate capacitor (C_G), in order to obtain better compatibility with conventional 1T–1C DRAM design. The write and read signals used in the operation of a single device are further adapted for the memory array. In order to achieve selective write and read which are vital for array operation, the C_G is partially charged instead of fully charged for logic "1". Finally, we show that by utilizing the top and bottom capacitors (C_G and C_{BG}), a single Z^2-FET cell is able to store two bits, which can be written using a single write and read out through alternating drain and source signals.

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http://dx.doi.org/10.1016/j.sse.2013.02.010

2. Experimental setup and study of retention time

The Z^2-FET is a forward biased *p-i-n* diode with the intrinsic channel partially covered by the front gate (L_G) and the rest ungated (L_{IN}), schematically shown in Fig. 1a. The operation of Z^2-FET utilizes the feedback between electron and hole currents and the corresponding injection barriers formed by front and back gates, as described in detail elsewhere [12]. The I_D–V_D curves show a hysteresis window linearly controlled by the V_G, see Fig. 1b [12,15]. This property is vital for memory applications.

In order to study its memory functionality, transient measurements were performed on the Z^2-FET, using the experimental setup shown schematically in Fig. 1a. To program and read, voltage pulses were applied to gate and drain, whereas the V_{BG} was fixed at 2 V to form the hole injection barrier. The source current I_S is measured as the output read signal. The "1" and "0" states are differentiated by the storage of positive charge on the front gate capacitor C_G.

Fig. 1c experimentally demonstrates the functionality of the Z^2-FET DRAM. The V_G and V_D pulses are used to write the logic "0" and "1" by discharging and charging the C_G, respectively. Thereafter, a negative V_D pulse is applied to read out the states by inducing a transient discharging current that triggers the internal feedback and turns on the device for logic "1" [13]. Thus, the read pulse outputs high current for logic "1" and low current for logic "0", see Fig. 1c.

As explained in [13], the logic "0" with no charge stored on C_G is not an equilibrium state. The leakage current of the drain junction (I_{DLEAK}) recharges the C_G and eventually turns the "0" into "1", as shown schematically in Fig. 2a. Since the $V_G \neq 0$ and $V_D = 0$ during the hold stage, the I_{DLEAK} only depends on V_G. For simplicity, we assume that the I_{DLEAK} does not change with time in the hold stage. Thus, the quantity of charge replaced by the I_{DLEAK} after a limited retention time (t_{re}) in the hold stage is $Q_{CG} = I_{DLEAK} \times t_{re}$. In the readout stage, some of this charge is evacuated by the V_D pulse: $\Delta Q_G = Q_{CG} - |V_G - V_D| \times C_G$, where $|V_G - V_D| \times C_G$ is the residual charge left on C_G in read stage. If ΔQ_G exceeds a certain threshold value (ΔQ_{Gth}) after long enough time t_0 in the hold stage, it can induce a strong transient current to turn on the device and cause the failure of logic "0", see Fig. 2b for $t_0 = 1.5$ s. Thus, an expression for retention time can be obtained by combining the expressions of Q_{CG} and ΔQ_G:

$$t_{re} = \frac{|V_G - V_D| \cdot C_G + \Delta Q_{Gth}}{I_{DLEAK}(V_G, T)} \quad (1)$$

where the junction leakage I_{DLEAK} depends on V_G and temperature T. From Eq. (1), the retention time is sensitive to the operating voltage, temperature and gate capacitance determined by the device dimensions and gate oxide.

Fig. 3 experimentally shows the dependence of t_{re} on V_G, V_D, T, L_G and L_{IN}. At high $|V_G|$, the junction leakage is dominated by the band-to-band tunneling, which decreases exponentially as $|V_G|$ decreases, prolonging the t_{re}, see Fig. 3a. At low $|V_G|$, tunneling becomes negligible and I_{DLEAK} is dominated by thermal generation, which does not depend on $|V_G|$, so t_{re} saturates. Reducing $|V_D|$ in the readout pulse reduces the transient forward-biased voltage at the drain junction, see Fig. 3a, and hence increases t_{re} according to Eq. (1).

The measurements under various temperatures indicate that t_{re} decreases exponentially as T increases due to higher I_{DLEAK}, as

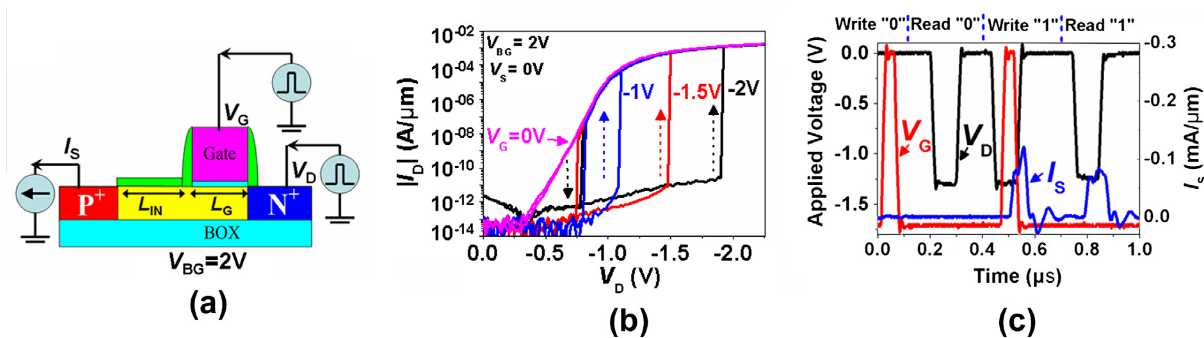

Fig. 1. (a) Schematic device structure of Z^2-FET with the transient measurement setup, (b) the I_D–V_D characteristics of the Z^2-FET showing gate-controlled hysteresis that permits memory operation and (c) Z^2-FET DRAM operation including the write and read sequence of logic "0" and "1" states (device parameters are $T_{ox} = 3$ nm HfO_2, $T_{Si} = 20$ nm, $T_{BOX} = 140$ nm, $L_G = 400$ nm and $L_{IN} = 500$ nm).

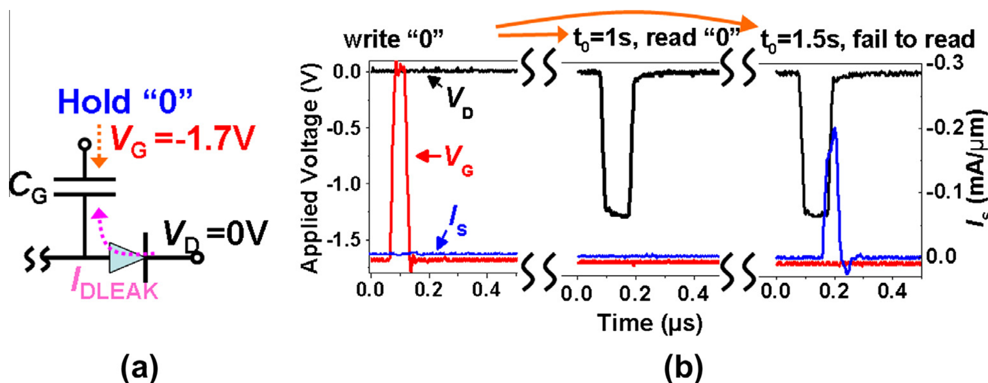

Fig. 2. (a) Equivalent circuit indicating the failure of logic "0" resulting from the recharge of C_G by junction leakage current and (b) transient measurement showing the read of logic "0" at different times. The device is a surface charge (Q_S)-operated Z^2-FET with parameters of $T_{ox} = 6$ nm SiO_2, $T_{Si} = 20$ nm, $T_{BOX} = 140$ nm, $L_G = 400$ nm and $L_{IN} = 200$ nm.

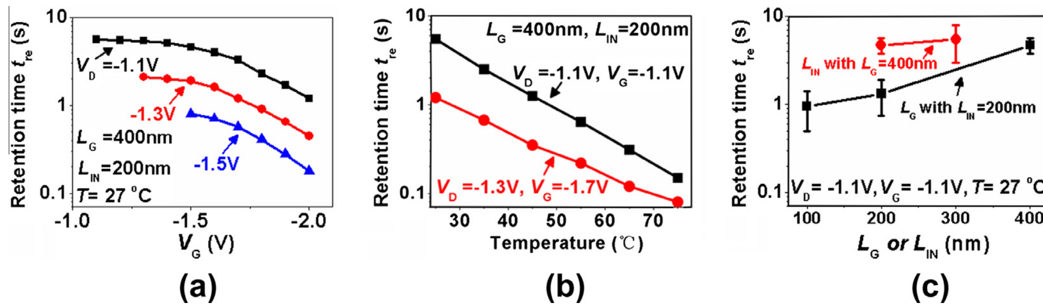

Fig. 3. Dependence of retention time of logic "0" (t_{re}) on the (a) applied V_G and V_D in holding and reading stages, respectively, (b) temperature (T) and (c) dimensions (L_G and L_{IN}). Note that the devices are Q_S-operated Z^2-FET DRAMs, same as in Fig. 2.

shown in Fig. 3b. The t_{re} at lower bias has stronger temperature dependence due to the thermal generation, whereas tunneling-dominated I_{DLEAK} at high $|V_G|$ is less sensitive to temperature.

Reducing L_G reduces the gate capacitance C_G and thus reduces t_{re}, whereas changing L_{IN} does not have a strong impact on t_{re}, see Fig. 3c.

3. Alternative writing mode using the source MOSFET

An alternative operation mode of the Z^2-FET DRAM uses the source-side MOSFET to write to C_G, as illustrated in Fig. 4a. Here, C_G is charged through a transistor, like a standard 1T–1C DRAM, but the stored charge is still read out through the internal feedback, ensuring less required charge and higher speed. This mode is suitable for a device with two independent gates. Here, we use the V_{BG}-operated Z^2-FET for experimental demonstration, shown in Fig. 4b, where the C_G is initially discharged through the drain junction (write "0"), and then recharged (write "1") by the negative V_{BG} pulse turning on the source-side p-channel MOSFET. We note that the charging/discharging of the gate does not require drain bias, which is important for low-power applications. In the hold state, the holes are retained on C_G by the negatively biased front-gate $V_G = -1.7$ V, as in the standard Z^2-FET operation above. The memory state is correctly read out with the same V_D pulse via internal feedback, as discussed above. The full simulated memory cycle is shown in Fig. 4c, with constant $V_G = -1.5$ V, $V_S = -1.5$ V and 0 for discharging and charging C_G as V_{BG} is pulsed to -1.5 V, and both logic states correctly read out using V_D pulses. It also demonstrates the access time down to 1 ns which is not achieved in our experiment due to equipment limitations. The TCAD simulation is performed in Silvaco [16] using the bipolar model with 10 ns carrier lifetime.

This mode may be advantageous because of design rules analogous to the conventional 1T–1C DRAM, with different terminals used to write and read the logic states. Another advantage of this mode is that the device stays in the OFF state during the writing of logic "1", see Fig. 4b, consuming less power compared to the previous writing method which needs to turn on the device [13].

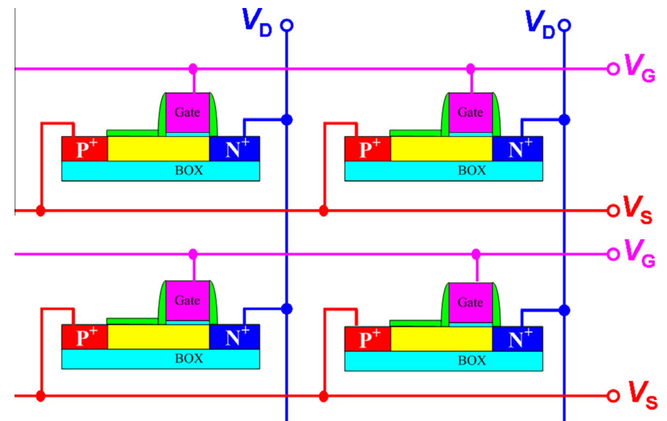

Fig. 5. Schematic view of a 2 × 2 1T-DRAM array using Z^2-FET devices.

4. Selective read/write for memory array operation

So far, Z^2-FET DRAM operation has been demonstrated experimentally on a single device only. However, any practical application of the Z^2-FET DRAM requires successful array operation, with cells connected together as in Fig. 5. In the following discussion, we will assume the V_{BG} of all cells is connected and biased constantly, $V_{BG} = 2$ V. The operation on a selected cell should not cause the failure or disturbance of other cells sharing the same V_D and V_G signal lines.

For example, the writing of a selected cell must not influence the state of other cells. Therefore, the method for writing both logic "0" and "1" to a single device shown in Fig. 2 is likely to be unsuitable, since it uses a V_G pulse switching back to 0. During the writing

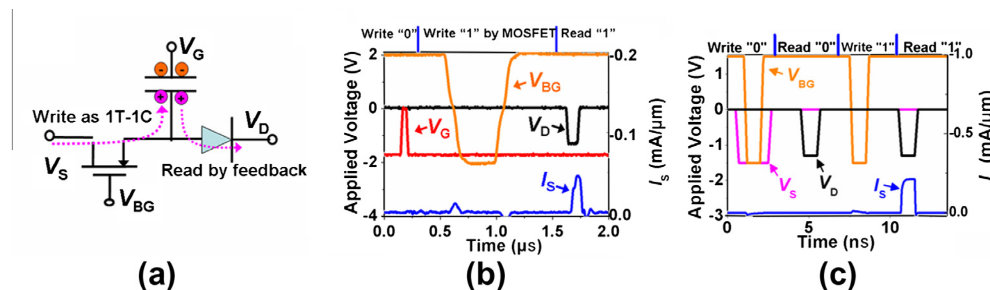

Fig. 4. (a) Schematic view, (b) experimental demonstration and (c) TCAD simulation of the alternative DRAM mode using the source MOSFET for writing and the Z^2-FET feedback for reading. The device has the same parameters as that in Fig. 1.

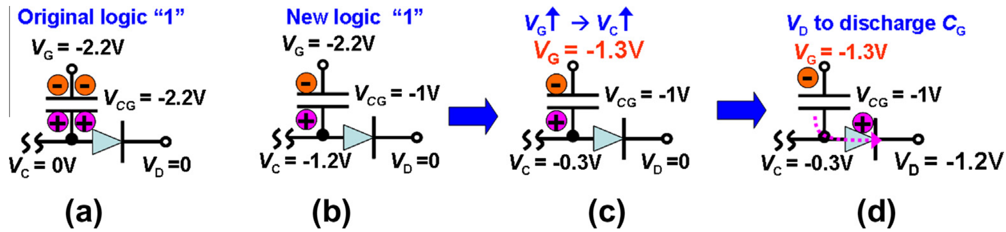

Fig. 6. Schematic view showing: (a) the original, (b) the modified logic "1" with fully and partially charged C_G, respectively, (c) in order to read the state, V_G is first raised to -1.3 V, which increases the V_C from -1.2 V to -0.3 V, after which (d) the negative $V_D = -1.2$ V pulse forward-biases the drain junction and triggers feedback to turn on the device.

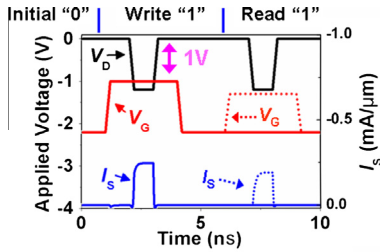

Fig. 7. Transient simulation showing the write and read "1". The logic "1" is read out correctly using both V_D and V_G signals (dashed curve). The read with only V_D cannot discharge the C_G and the device stays in OFF state (solid curve).

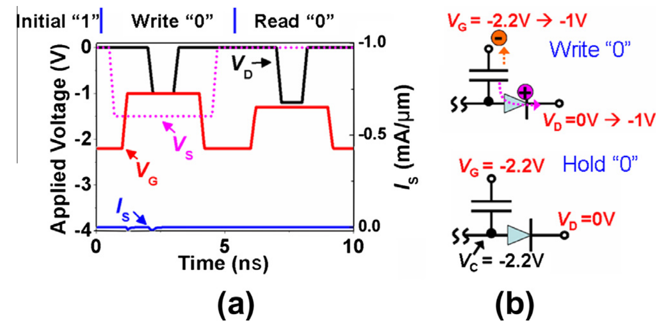

Fig. 8. (a) Simulation showing the new scheme for logic "0" operation and (b) schematic view to explain the write "0" by raising and dropping the V_G and V_D simultaneously to the same -1 V value, in order to fully discharge the C_G. The V_S is reduced during the write "0" to keep the device in OFF state.

stage, all cells sharing the same $V_G = 0$ signal would be fully discharged and their logic states erased, as is evident from Fig. 5. Further, readout using a V_D pulse only is also nonselective: in all logic "1" cells C_G is fully charged and channel voltage (V_C) is 0 V, so the readout V_D pulse forward-biases the drain junctions and turns on all logic "1" cells sharing the same V_D line.

This problem can be solved by revising the logic state biasing, as illustrated in Fig. 6a. Compared to the fully charged C_G in the original logic "1", see Fig. 6a, the C_G is only *partially* charged in the modified logic "1" state, as in Fig. 6b. Suppose $V_G = -2.2$ V and voltage drop V_{CG} on the partially charged C_G is $V_{CG} = -1$ V. This leaves the channel potential $V_C = -1.2$ V, reverse-biasing the drain junction. During the readout, which still uses a negative V_D pulse from 0 to -1.2 V, the C_G is not discharged to turn on the device since the $V_C = -1.2$ V which counteracts the applied V_D pulse.

In order to read out the modified logic "1" in a selected Z^2-FET, the V_G is first raised to -1.3 V, which raises the V_C to ~ -0.3 V, as shown in Fig. 6c. The subsequent negative $V_D = -1.2$ V pulse induces ~ 0.9 V forward bias on the drain junction and discharges the C_G, see Fig. 6d. The discharging current triggers the feedback and turns on the device.

Fig. 7 shows the simulation of selective operation of logic "1", where the C_G is partially charged in write "1". During write "1", $V_D = -1.2$ V and $V_G = -1$ V, so that the Z^2-FET is turned on due to $|V_D| > |V_G|$ with both electrons and holes injected into the channel [12,13,15]. Thereafter, V_D is switched back to 0 to turn off the device and partially charge the C_G due to $V_G = -1$ V. The readout using only a V_D pulse down to -1.2 V does not turn on the device (solid lines in Fig. 7). The dashed curve in Fig. 7 shows that the device is turned on if both V_G and V_D pulses are used simultaneously, corresponding to a "selective" read.

The biasing for writing logic "0" can also be modified to accommodate selective operation for a DRAM array. Instead of raising the V_G up to 0 and erasing all cells on the same V_G line, the new method switches both the V_G and V_D to -1 V, see Fig. 8a. Meanwhile, the V_S is reduced to -1.5 V to keep the device in the OFF state. This can fully discharge the C_G, as indicated in Fig. 8b, without affecting other logic "1" cells sharing the same V_G or V_D signals. Again, the key point is that the C_G is partially charged in logic "1", so V_C = - -1.2 V and the V_G and V_D pulses during the write "0" sequence

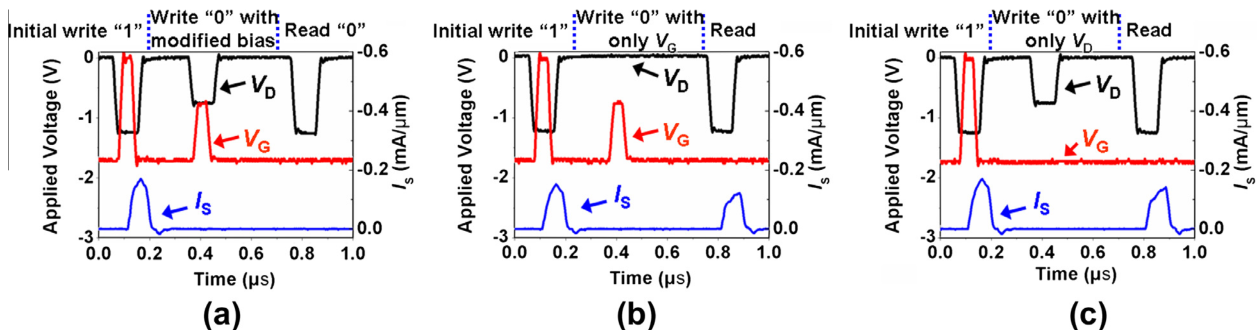

Fig. 9. Experimental results demonstrate that (a) the write "0" succeeds using both the V_G and V_D pulses, whereas the use of only (b) V_G or (c) V_D does not change the original logic "1" state.

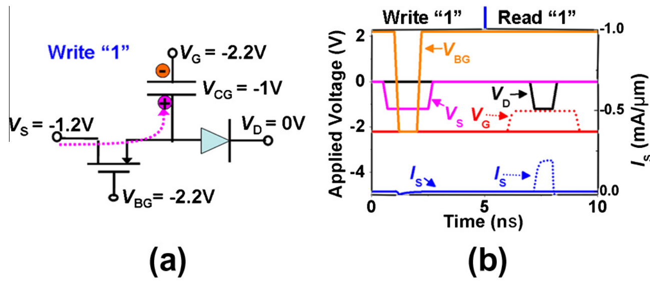

Fig. 10. (a) Schematic view and (b) simulation showing the selective operation of the Z^2-FET DRAM using the source MOSFET for the write. The logic “1” can only be read out by simultaneously applying the V_G and V_D pulses, as indicated by the dashed curves.

are not high enough separately to forward-bias the drain junction and discharge the C_G in the unselected cell.

Preliminary experimental demonstration of the selective operation is shown in Fig. 9. The device is initially written to logic “1” using the same method as in [13]. Then the V_G and V_D signals are applied simultaneously to fully discharge the C_G and write logic “0”, see Fig. 9a. Note that, in order to avoid the use of V_S (not achievable in our measurement set-up), the V_G and V_D in our experiment were pulsed to −0.7 V instead of −1 V to keep the device in OFF state. The read correctly outputs low current, since there is no charge left at the gate for triggering the feedback. Fig. 9b and c show that the write “0” with only V_G or V_D does not change the original “1” state simply because the residual gate charge is large enough to trigger the feedback and turn on the device, correctly maintaining “1” in the unselected cells.

An alternative approach for memory array operation, inspired by Section 3, is to use the source MOSFET for selective writing. This operation mode is analogous to the 1T–1C DRAM. Instead of using $V_S = 0$ in Fig. 4c, which fully charges the C_G, the C_G is partially charged during the write “1” step by setting $V_S = -1.2$ V, see Fig. 10a. Then, as shown in Fig. 10b, only a combination of V_D and V_G pulses can discharge the C_G and read out the state, whereas a V_D pulse alone does not discharge the C_G.

5. Scaling capability and dual bit storage

Fig. 11a shows the schematic structure of a downscaled Z^2-FET with two non-overlapping independent gates. The simulated I_D–V_D curves under various V_G in Fig. 11b demonstrate the ultimate scaling capability of the Z^2-FET down to $L_G = L_{IN} = 25$ nm, thanks to the improved electrostatic control due to ultra-thin $T_{Si} = 5$ nm and $T_{BOX} = T_{ox} = 1$ nm. The DRAM functionality is shown in Fig. 11c,

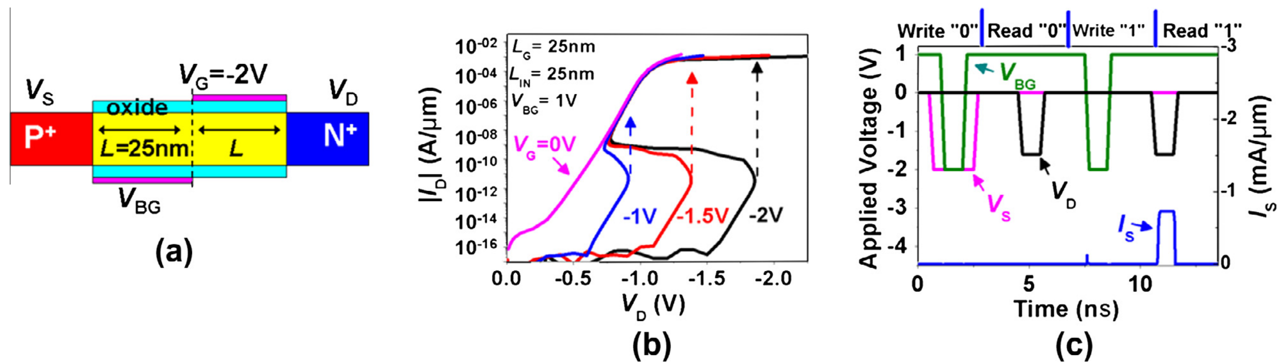

Fig. 11. (a) Schematic view, (b) I_D–V_D simulation of the scaled Z^2-FET where the back gate has no overlap with front gate and (c) transient simulation demonstrating the DRAM functionality using the source MOSFET for write, similar to that in Fig. 4c. The device is scaled down to $T_{ox} = T_{BOX} = 1$ nm, $T_{Si} = 5$ nm, $L_G = L_{IN} = L = 25$ nm.

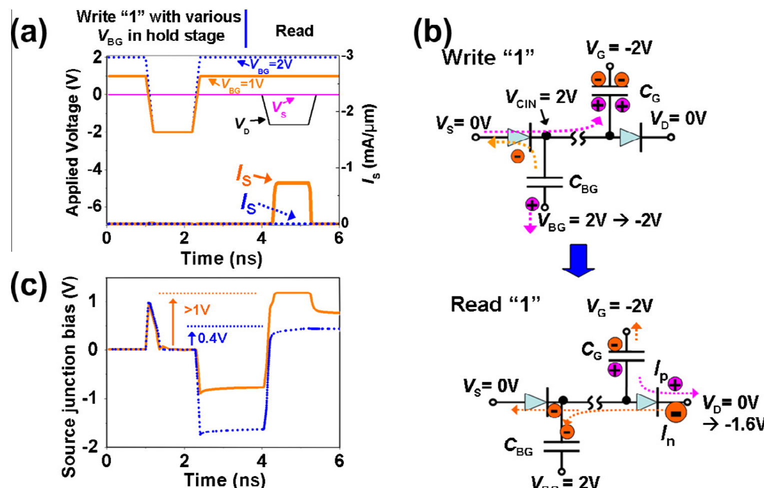

Fig. 12. (a) Simulation showing the write “1”, same as in Fig. 11c, with various V_{BG} in hold stage, (b) equivalent circuit explaining two storage nodes in the Z^2-FET with large C_{BG}, where a part of the electron current (I_n) induced by the discharge of C_G charges the C_{BG} and fails to reach the source junction to trigger the feedback and (c) evolution of the voltage drop on the source junction showing that the high V_{BG} in hold stage can deeply reverse-bias the source junction and impede the feedback.

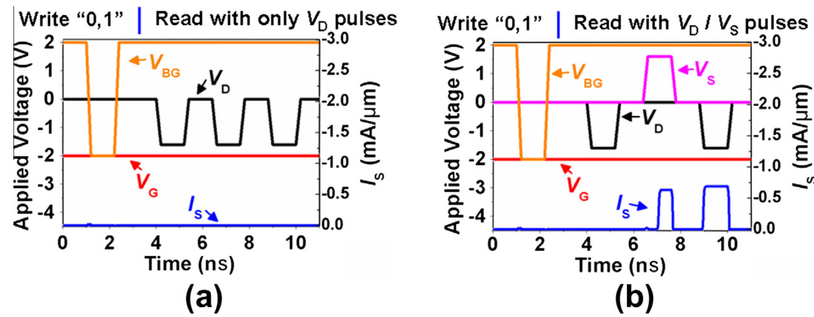

Fig. 13. Simulations demonstrating that the dual logic bits "0,1" (a) cannot be read out through consecutive V_D pulses (b) but it can be read out by alternating V_D and V_S pulses.

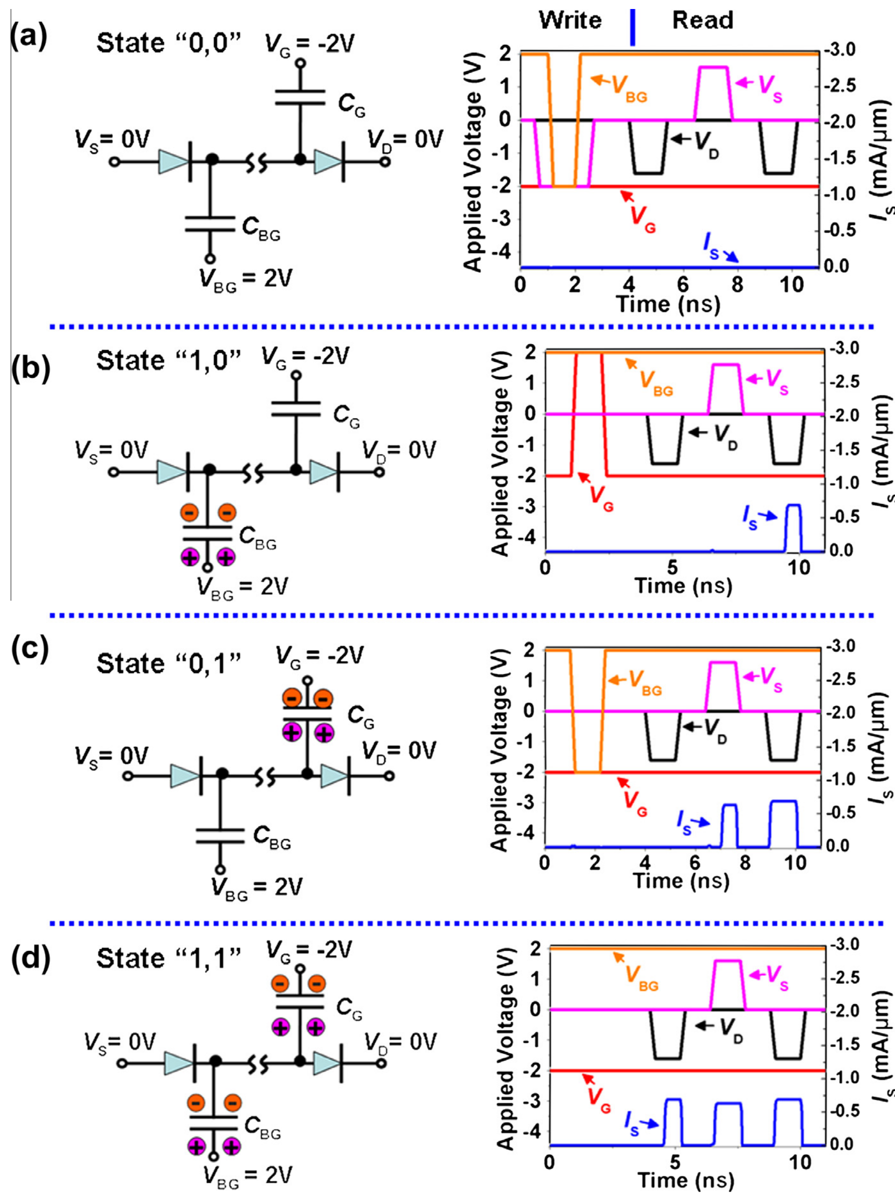

Fig. 14. Schematic view of the stored charges (left panel) and DRAM operation in simulation (right panel) of the logic (a) "0,0", (b) "1,0", (c) "0,1" and (d) "1,1". Note that the initial state is "1,1" and thus there is no write step in (d).

where the source MOSFET is used for writing the state, same as in Fig. 4c.

Unlike the floating body memory [4], the scaling of T_{Si} in the Z^2-FET does not suffer from the supercoupling effect. This is due to the fact that only one type of carriers (holes in this case) is needed to trigger the feedback during the readout stage in the Z^2-FET DRAM, whereas most of the floating-body memories are based on the coexistence of holes and electrons in the channel.

The Z^2-FET with ultra-thin buried oxide (BOX) as in Fig. 11a can be used to store two bits thanks to the large C_{BG} that provides an extra storage node. The storage capacity of the C_{BG} is demonstrated by the simulation in Fig. 12a, where the write "1" is carried out as in Fig. 11c and various V_{BG} are applied in the hold stage. For V_{BG} = +1 V, state "1" (high current) is read. As V_{BG} increases to +2 V, the read pulse outputs low current indicating that the feedback is not triggered though C_G is charged.

This can be explained by considering the schematic charging and discharging of both capacitors shown in Fig. 12b. During the write "1" ($V_{BG} = 2 \rightarrow -2$ V), the C_G is charged by the source MOSFET, whereas the C_{BG} is discharged through the forward-biased source junction. As V_{BG} switches back to 2 V in hold stage, the channel potential in intrinsic region (V_{CIN}) is 2 V since there is no voltage dropped on C_{BG}. This deeply reverse-biases the source junction.

The negative V_D readout pulse ($V_D = 0 \rightarrow -1.6$ V) discharges the C_G and enables transient hole current (I_p) through the drain junction. This hole current induces high electron injection from drain, which normally should flow to source and trigger the feedback. However, a large fraction of the injected electrons (I_n) needs to charge the C_{BG} and restore the V_{CIN}. Only the rest of electrons flow to source, forward-bias the source junction and trigger the feedback. If V_{BG} is too high, e.g. V_{BG} = 2 V, most of the injected electrons charge C_{BG} and the rest are insufficient to trigger feedback. Fig. 12c shows the evolution of the source junction bias ($-V_{CIN}$), where the junction is reverse-biased after write "1". The read pulse induces electron injection and raises the source junction bias up to 1 V under V_{BG} = 1 V, which is enough to inject holes from source and trigger the feedback turning on the device. However, under V_{BG} = 2 V, the forward bias of source junction is only 0.4 V, not high enough to trigger the feedback.

Thus, the two-bit logic state in the device is "0,1", with C_{BG} discharged and C_G charged. A series of consecutive V_D pulses cannot read out the dual logic bits, since the C_G would be discharged by the first V_D pulse, see Fig. 13a. Instead, simulations show that an alternating sequence of V_D and V_S pulses can turn on the device as shown in Fig. 13b. This is due to the fact that the first V_D pulse transfers electrons to C_{BG} and raises the potential of source junction to 0.4 V, as explained in Fig. 12b and c. The following V_S pulse ($0 \rightarrow 1.6$ V) together with the residual 0.4 V induces high 2 V forward bias on the source junction, leading to hole injection from the source that triggers the feedback and turns on the device. Both the C_G and C_{BG} are fully charged by the electron–hole plasma when the device is in the ON state [13] and thus the third V_D pulse also outputs high current, see Fig. 13b.

Fig. 14 shows the equivalent circuits and preliminary simulations of the dual bit operation for logic states including "0,0", "1,0", "0,1" and "1,1". The initial memory state is "1,1". For logic "0,0", both the C_G and C_{BG} are discharged by $V_{BG} = V_S = -2$ V through the source junction. Since there is no charge serving as seed, the readout using alternating V_D and V_S pulses always outputs low current. To write logic "1,0", the V_G is increased up to 2 V while V_{BG} remains constant (+2 V) so that the C_G and C_{BG} are discharged and charged respectively through the drain junction; this mechanism is reciprocal to the source MOSFET programming described in Section 3. During the read, the first pulse (V_D) has no effect since there is no charge stored in C_G. The second pulse (V_S) discharges the C_{BG} and transfers holes to C_G; this operation is similar to the first V_D pulse for logic "0,1" discussed previously in Fig. 13b. Hence, the third V_D pulse can strongly discharge the C_G and trigger the feedback to turn on the device. As for the logic "1,1", since both C_G and C_{BG} are fully charged, the first V_D read pulse can induce feedback and turn on the device.

To summarize, the readout uses a 3-pulse sequence:

- Current detected at first pulse indicates "1,1" state.
- Current detected at second pulse indicates "0,1" state.
- Current detected at third pulse indicates "1,0" state.
- No current detected during the entire three-pulse sequence reflects "0,0" state.

The dual bit operation of the Z^2-FET DRAM can achieve enhanced storage capacity compared to than the single bit, which translates into memory area savings. But it also offers faster writing, as only one step is needed to write two bits, see Fig. 14. However, the use of dual bit storage requires a device structure with ultra-thin BOX and non-overlapping front and back gates, the feasibility of which remains to be validated technologically on planar SOI or FinFET structures.

6. Conclusion

In this paper, we have extended our previous studies on a compact, capacitor-less DRAM device in FD-SOI utilizing the Z^2-FET. The retention time of logic "0" due to the drain junction leakage current has been studied experimentally as a function of V_G, V_D, T, L_G and L_{IN}. The retention time increases as the voltage and temperature are reduced, due to lower leakage. The increase of gate length can also prolong the retention time thanks to the increase in C_G. An alternative logic state writing technique using the source MOSFET has been explored through both experiment and simulation. The selective write/read for DRAM array operation has been achieved by using partially charged gate capacitance in logic "1". Both the selective write and read on logic "1" and "0" have been discussed and demonstrated in simulation, with preliminary experiments to confirm the TCAD results. Next, the Z^2-FET DRAM was demonstrated to be scalable down to 25 nm in an advanced SOI structure with ultra-thin BOX and independent non-overlapping front and back gates. This advanced structure is capable of storing two bits in a single cell by using the charges stored on both the front and back gates and read out through alternating V_D and V_S pulses.

Acknowledgments

The work at Minatec was funded by the RTRA program of the Grenoble Nanosciences Foundation. A. Zaslavsky also acknowledges support by the U.S. National Science Foundation (award ECCS-1068895). Another author (CLR) also acknowledges support by the European STEEPER project (FP7/2007-2013, Grant Agreement No. 257267).

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