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A systematic study of the sharp-switching Z^2-FET device: From mechanism to modeling and compact memory applications

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ABSTRACT

This paper presents a systematic study of a sharp-switching device built in fully-depleted silicon-on-insulator (FD-SOI) that we have called Z^2-FET, as it features zero subthreshold swing (<1 mV/decade of current) and zero impact ionization. The Z^2-FET is a compact device with a single front gate that experimentally demonstrates a current I_{ON}/I_{OFF} ratio >10^8 at low supply voltage, as well as gate-controlled hysteresis. The operating principle of the sharp switching involves the positive feedback between carrier flow and gate-controlled injection barriers, as confirmed by TCAD simulations. We discuss the impact of bias and device dimensions on the experimental performance and simulate the Z^2-FET's ultimate scaling capability to <50 nm channel length. We present a simplified compact model of the Z^2-FET. With good reliability and relative insusceptibility to temperature variation, the envisioned applications of the Z^2-FET include compact, high-speed one transistor DRAM (1T-DRAM), one-transistor SRAM, fast logic and electrostatic discharge (ESD) protection circuits.

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1. Introduction

Compact CMOS-compatible devices with sharp switching are of great interest for logic application, and if they feature voltage-controlled hysteresis they are also promising for memory and electrostatic discharge (ESD) protection. Thyristors using the bipolar feedback triggered by impact ionization have been widely studied and used in power switch electronics [1,2]. Recently, the thin capacitively coupled thyristor (TCCT) built on SOI substrate has been used as a 1-transistor memory showing compactness and high access speed [3,4], but it requires accurate doping control in the channel for stable performance [5]. The field effect diode (FED) and feedback field effect transistor (FB-FET) have also been demonstrated for ESD protection, memory and switching applications by using the feedback controlled by two front gates and/or surface charges, respectively [6–9]. Very recently, a Fin-FET device with two adjacent gates has been simulated for use as a 1T-DRAM [10].

In this paper, we present a systematic study of the Z^2-FET, a compact device built on FD-SOI substrate with an undoped channel, a single front gate, and a back gate, that we have previously shown to exhibit ultra-sharp switching (zero subthreshold swing) and gate-controlled hysteresis [11,12] at biasing voltages below 2 V. After summarizing the operating principle, based on the positive feedback between electron and hole channel currents and their respective injection barriers [11], we discuss the impact of various structural parameters on the device performance, the effects of temperature, preliminary reliability tests, and the scaling capabilities of the Z^2-FET. Further, the gate-controlled hysteresis in the drain current–voltage I_D–V_D characteristics makes the Z^2-FET a promising structure for a compact, refreshable 1T-DRAM with high retention time and very fast access [12]. The same I_D–V_D hysteresis can also be used as a 1T-SRAM, where the back gate V_{BG} and heterojunction band engineering make it possible to reduce the standby power consumption.

2. Device structure and static (dc) performance

The Z^2-FET is a forward biased *p-i-n* diode with the intrinsic channel partially covered by the front gate (L_G) and the rest ungated (L_{IN}), schematically shown in Fig. 1a. The device is fabricated in an advanced FD-SOI process with high-*k*/metal gate and raised source/drain [13]. For the *p*-type Z^2-FET, the p^+ source is grounded and the n^+ drain is negatively biased ($V_S = 0$ and $V_D < 0$). The negatively and positively biased front and back gates ($V_G < 0$ and $V_{BG} > 0$) are used to form electron and hole injection barriers in L_G and L_{IN} regions, respectively. The two gate biases actually emulate a lateral *pnpn* thyristor-like structure, but without any channel doping.

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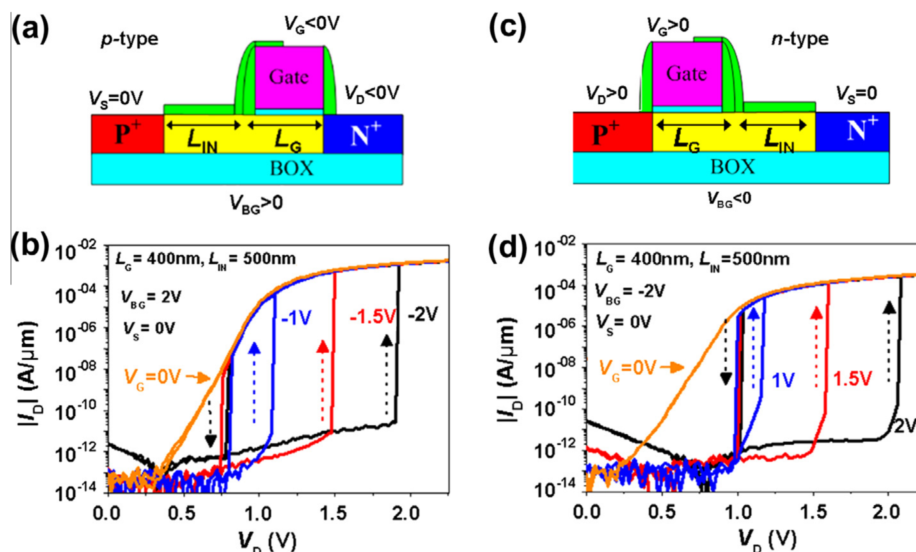

Fig. 1. Schematic structure of the (a) *p*-type and (c) *n*-type Z^2-FETs operating with back gate voltage $V_{BG} > 0$ and $V_{BG} < 0$, respectively. Experimental I_D–V_D curves of (b) *p*-type and (d) *n*-type Z^2-FETs show sharp switching and gate-controlled hysteresis. The device parameters are T_{ox} = 3 nm HfO_2, T_{Si} = 20 nm, T_{BOX} = 140 nm, L_G = 400 nm and L_{IN} = 500 nm.

I_D–V_D measurements show that the device is initially in OFF state at low $|V_D|$ and turned on sharply as $|V_D|$ increases to turn-on voltage $|V_{ON}|$. As $|V_D|$ sweeps back to 0, the device stays in the ON state until $|V_D|$ decreases below 0.8 V, at which point it turns off. Since the V_{ON} is linearly dependent on V_G, large hysteresis is obtained, see Fig. 1b.

Compared to the *p*-type device shown in Fig. 1a, in *n*-type Z^2-FET the gate is adjacent to the p^+ doped drain and positively biased, whereas the back gate is negatively biased, as shown in Fig. 1c. The I_D–V_D curves show similar sharp switching and V_G-controlled hysteresis as the *p*-type device, see Fig. 1d.

The transfer characteristic (I_D–V_G) also shows sharp switching, where the current increases by eight decades within a narrow ΔV_G = 1 mV range at $V_D = -1.5$ V, see Fig. 2a. The switching threshold can be tuned by biasing the V_D with grounded V_S (solid curves) or V_S with grounded V_D (dashed curves). Compared to other sharp-switching devices, such as the FB-FET [8], tunneling FET (TFET) [14] and impact ionization MOS (IMOS) [15], the Z^2-FET shows superior switching performance under reasonably low V_{DD} = 1.5 V supply voltage, see Fig. 2b.

3. Operating principle

The Z^2-FET device operation can be understood via TCAD simulations [16]. The models used in simulation include the doping-dependent carrier lifetime, mobility that depends on electric field and doping concentration, band gap narrowing and Auger recombination. Size quantization in the 5 nm thick Si channel was not considered. Fig. 3 shows the simulated I_D–V_D curves under different V_G reproducing the *p*-type Z^2-FET experimental results. In addition, the simulation allows visualizing the snap-back characteristic, which cannot be observed in conventional quasistatic I_D–V_D measurements as in Fig. 1b. Instead, a sharp vertical transition to a high-current state at the same V_D is seen experimentally, as indicated by arrows in Fig. 3. Including impact ionization has no effect, as shown by the dots in the $V_G = -2$ V curve, indicating that the operation of Z^2-FET does not involve impact ionization, and thus differs from a thyristor.

Fig. 4a shows the band diagrams in the channel of the Z^2-FET under various V_D with $V_G = -2$ V and V_{BG} = 2 V. Electron and hole barriers (V_n and V_p) are formed by V_G and V_{BG} respectively, blocking the carrier flow at low V_D. As $|V_D|$ increases, the channel potential under the front gate is clamped due to the forward-biased channel–drain junction. The holes accumulated under the gate are depleted as $|V_D|$ increases close to $|V_G|$, reducing the electron injection barrier. This enables the injection of electrons from the n^+ drain into the channel, which flow to the p^+ source and induce a potential drop at source–channel junction, thereby reducing the injection barrier for holes and initiating positive feedback. Strong positive feedback turns on the device sharply, see the V_D = -

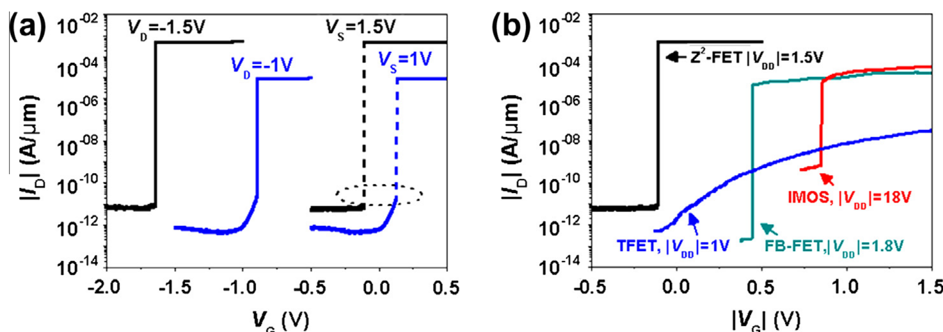

Fig. 2. Experimental I_D–V_G curves of the *p*-type Z^2-FET show sharp switching with subthreshold swing below 1 mV/decade. The I_{ON} exceeds 500 μA/μm at $V_D = -1.5$ V. The threshold voltage is determined by the relative bias of drain and source. (b) Comparison between Z^2-FET and other sharp-switching devices including the FB-FET [8], TFET [14] and IMOS [15].

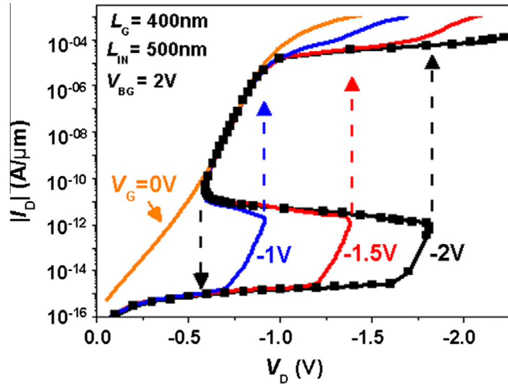

Fig. 3. Simulated I_D–V_D curves reproducing the experimental results in Fig. 1b.

−2 V band diagram in Fig. 4a, where both injection barriers have been suppressed by the electron and hole carrier densities that make up the high I_D once the device switches to the ON state.

Fig. 4b shows in more detail the evolution of V_n and V_p as $|V_D|$ increases towards $|V_{ON}|$. At low $|V_D|$, the channel under the gate is strongly accumulated with holes due to $V_G = -2$ V, forming a high V_n barrier and thus blocking the electron injection. As V_D becomes more negative, the channel potential (φ_C) is set by forward-biased channel–drain junction. When V_D decreases below the clamping voltage (V_C), holes in L_G region are depleted, and thus φ_C is pinned by the gate voltage V_G. Any further decrease of V_D reduces the V_n linearly, since V_n is determined by the potential difference between the channel and drain. Accordingly, the electrons are injected into the channel and flow to the source, initiating the positive feedback, which accelerates the reduction of barriers and increase of current, shown schematically in the close-up of Fig. 4c. The feedback is strong enough to sharply turn on the device at $V_D = V_{ON}$.

4. Alternative Z^2-FET variant operating with surface charge (Q_S)

The Z^2-FET can also operate with surface charge (Q_S) instead of V_{BG}, as shown in Fig. 5a. In this mode, one of the barriers is established by Q_S as in the FB-FET [8,9], whereas the other injection barrier is still set by the front gate ensuring good controllability of the switching point V_{ON}. The positive surface charge ($Q_S \sim 10^{12}$ cm^{-2}) in the p-type device of Fig. 5 is promoted by the chemical vapor deposited SiO_2 on the L_{IN} region.

Figs. 5b and c show the I_D–V_D and I_D–V_G curves respectively, featuring sharp switching and V_G-controlled hysteresis, similar to the corresponding V_{BG}-operated device shown in Figs. 1 and 2. The device parameters are T_{ox} = 6 nm SiO_2, T_{Si} = 20 nm, T_{BOX} = 140 nm, L_G = 200 nm and L_{IN} = 200 nm.

5. Scaling capability: experiment and simulation

The scaling of the Z^2-FET depends on the control of the relevant injection barriers by V_G and either Q_S or V_{BG}, respectively. Fig. 6a shows the I_D–V_D measurements on Q_S-operated Z^2-FET with L_G scaling from 400 nm down to 100 nm at constant L_{IN} = 200 nm. The $|V_{ON}|$ decreases only slightly, thanks to the strong control of L_G region by V_G. However, the $|V_{ON}|$ drops abruptly as L_{IN} scales down to 100 nm with L_G = 400 nm, see Fig. 6b. This is due to the fact that the Q_S has weaker control over the L_{IN} region.

To go beyond the experimentally available device parameters, we have studied the impact of Q_S density on the device scaling by TCAD simulation. Fig. 7 shows the simulated relation between V_{ON} and the amount of Q_S for Z^2-FET with various L_{IN}. In low Q_S region, V_{ON} is very sensitive to the precise value of Q_S. The sensitivity is higher for devices with longer L_{IN}, a property that may prove interesting for sensor applications. However, at sufficiently high Q_S, V_{ON} saturates and is only controlled by V_G, see Fig. 7. A value of $Q_S \sim 10^{12}$ cm^{-2} is enough for our experimental devices with $L_{IN} \geqslant 200$ nm. For devices with shorter L_{IN}, higher surface charge density is needed, which is difficult to control precisely. For this

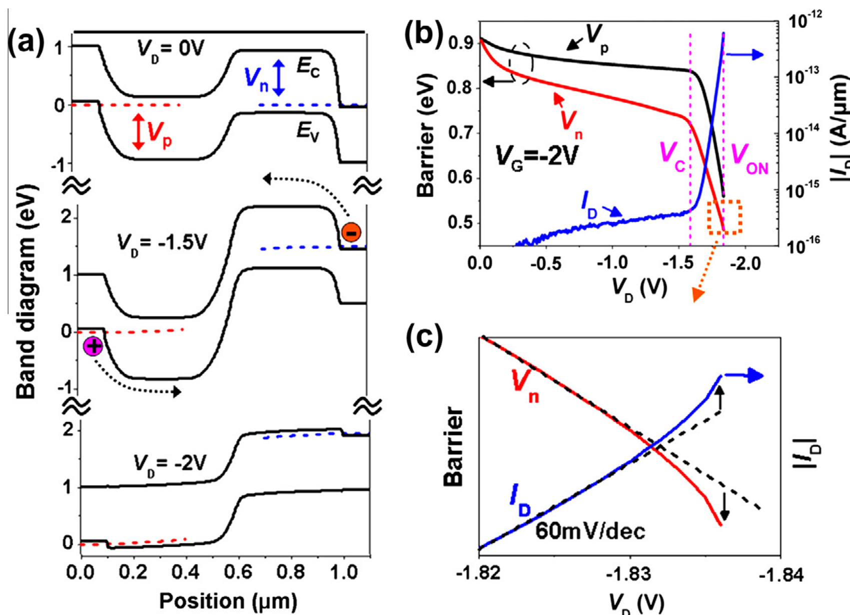

Fig. 4. (a) Self-consistent simulated band diagrams in a p-type Z^2-FET vs. V_D at V_G = −2 V and V_{BG} = 2 V, showing how the electron and hole injection barriers (V_n and V_p) are eliminated at V_D = −2 V. (b) Evolution of V_n, V_p and I_D as V_D decreases from 0 to V_{ON}. (c) Close-up of the V_{ON} region showing schematically how the feedback reduces the barrier and increases the current.

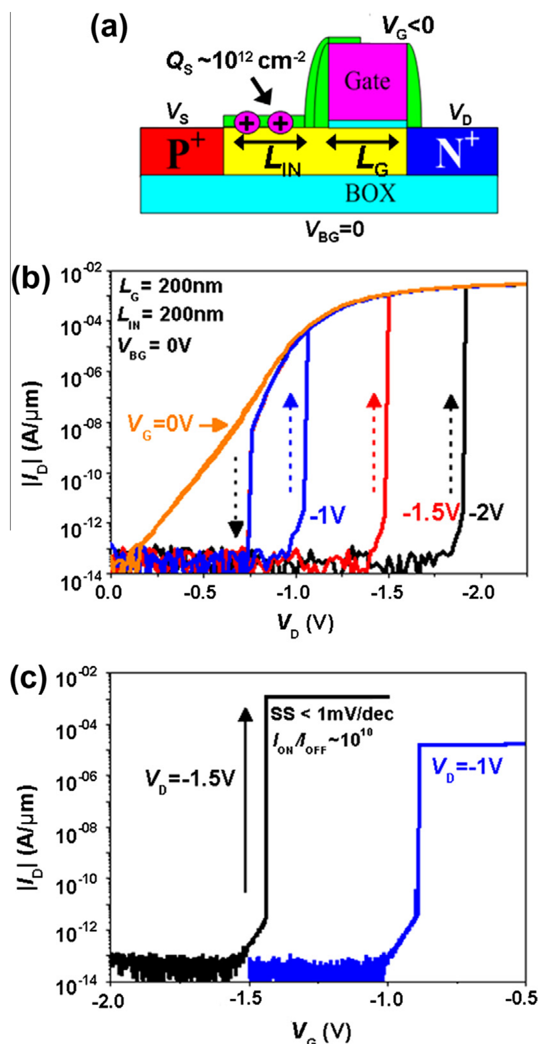

Fig. 5. (a) Schematic structure of the *p*-type Z^2-FET operating with surface charge density Q_S instead of V_{BG}. (b) its I_D–V_D and (c) I_D–V_G characteristics show sharp switching and gate-controlled hysteresis similar to the V_{BG} controlled device as in Figs. 1 and 2.

reason, downscaling of the Z^2-FET further, below 100 nm, requires using V_{BG} operation.

In order to establish the ultimate scaling limit of the Z^2-FET, we carried out simulations of the V_{BG}-operated device in a more advanced SOI structure, by studying the impact of T_{ox}, T_{Si} and T_{BOX} while keeping the V_G and V_{BG} fixed and setting L_G equal to L_{IN} (so $L_G = L_{IN} = L$). The effects of varying T_{ox}, T_{Si} and T_{BOX} are shown

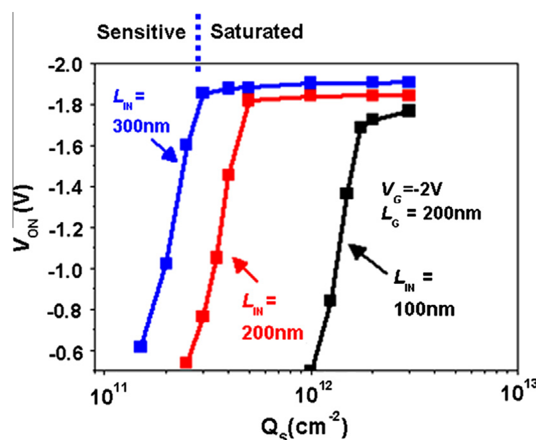

Fig. 7. Simulated dependence of V_{ON} on the density of surface charge Q_S for Z^2-FET with various L_{IN}.

respectively in Fig. 8a–c. The general trend in Fig. 8 is that as $L_G = L_{IN} = L$ decreases, the V_{ON} is initially stable and then drops abruptly when V_G and V_{BG} lose control of the injection barriers in the L_G and L_{IN} regions, respectively. With thinner T_{ox}, the control of the L_G region by the front gate is stronger and the V_{ON} is less affected by the coupling from the back gate, resulting in better scaling capability and higher saturated $|V_{ON}|$, as shown in Fig. 8a where T_{ox} = 1 and 3 nm are compared. Similar behavior is observed for the scaling of T_{Si}, see Fig. 8b where the device with T_{Si} = 5 nm has better scalability and higher saturated $|V_{ON}|$ than that with T_{Si} = 7 nm. Thinner BOX also results in better scalability thanks to the stronger control of V_{BG} on L_{IN} region, see the curve with T_{BOX} = 15 nm as opposed to 20 nm in Fig. 8c. However, the saturated $|V_{ON}|$ is slightly reduced due to the stronger coupling from back gate in the L_G region.

Fig. 9 shows that the Z^2-FET with advanced SOI structure of T_{ox} = 1 nm, T_{Si} = 5 nm and T_{BOX} = 15 nm is scalable down to $L_G = L_{IN}$ = 30 nm without significant degradation. If T_{BOX} is scaled even further, below 10 nm, the back gate can be replaced by a highly-doped unbiased ground plane (GP), commonly used in FD-SOI MOSFETs [17].

Fig. 10a schematically shows the *p*-type Z^2-FET using a *grounded* 20 nm n^+-doped GP layer under an ultra-thin buried oxide T_{BOX} = 8 nm. The potential difference between the highly doped GP layer and the intrinsic channel is strong enough to form the carrier injection barrier in the L_{IN} region. The I_D–V_D simulation shows the same sharp switching and hysteresis as before, see Fig. 10b, where we also show the opposite case of an *n*-type Z^2-FET with a p^+-doped GP layer. Even greater scalability, down to L = 20 nm, is possible if the Z^2-FET is simulated as having non-overlapping front and back gates, see Fig. 10c. Evidently such a structure would be

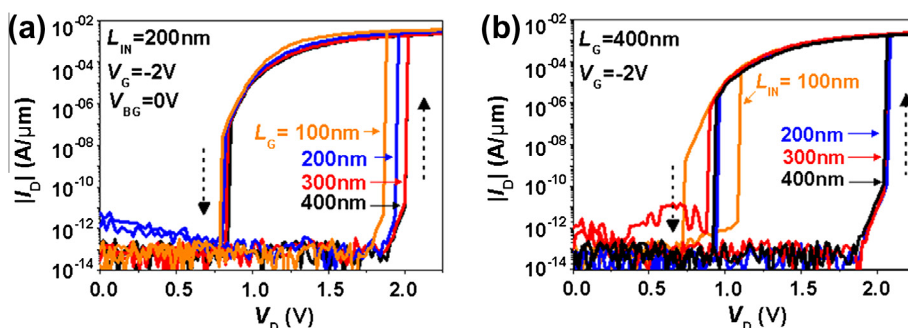

Fig. 6. Experimental I_D–V_D measurements on Q_S-operated Z^2-FET with (a) L_G and (b) L_{IN} scaling from 400 to 100 nm. V_G = –2 V for all curves.

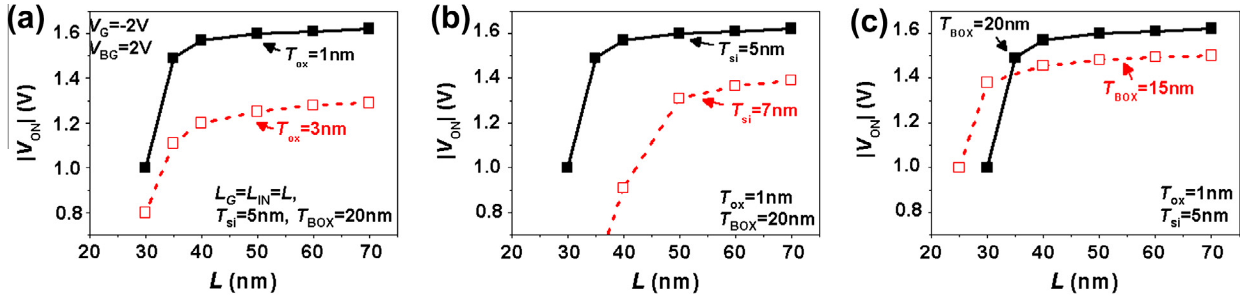

Fig. 8. Comparison of scaling capability between V_{BG}-operated Z^2-FETs with various (a) T_{ox}, (b) T_{Si} and (c) T_{BOX} at fixed $V_G = -2$ V and $V_{BG} = 2$ V. The reference device (solid symbols) has $T_{ox} = 1$ nm, $T_{Si} = 5$ nm and $T_{BOX} = 20$ nm.

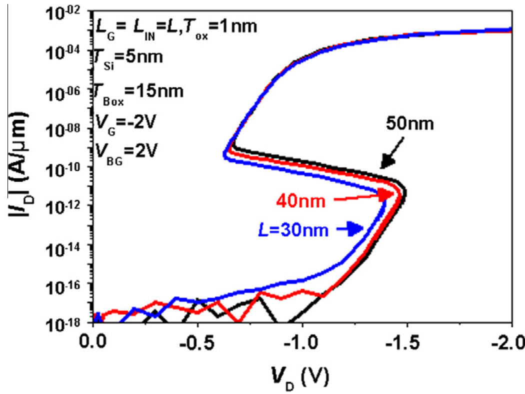

Fig. 9. Simulated I_D–V_D curves of V_{BG}-operated Z^2-FET with $L_G = L_{IN} = L$ scaling from 50 nm to 30 nm at fixed $V_G = -2$ V. The simulated device has advanced SOI structure of $T_{ox} = 1$ nm SiO_2, $T_{Si} = 5$ nm and $T_{BOX} = 15$ nm.

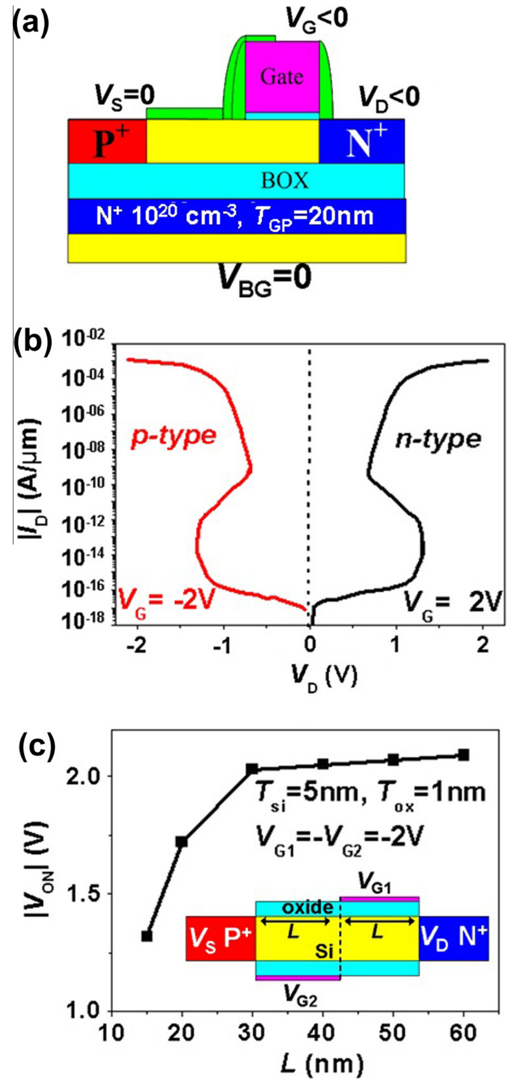

Fig. 10. (a) Schematic view of the p-type Z^2-FET using n^+-doped ground plane (GP) replacing V_{BG}; (b) simulated I_D–V_D curves of the p-type and n-type devices with $L_G = L_{IN} = 50$ nm, $T_{ox} = 1$ nm SiO_2, $T_{Si} = 5$ nm and $T_{BOX} = 8$ nm at fixed $V_G = -2$ and 2 V, respectively; (c) V_{ON} vs. L_G of idealized Z^2-FET with non-overlapping gates, showing scalability down to 20 nm.

more difficult to fabricate, but a local GP in the L_{IN} region only, a planar double-gate process [18], or a Fin-FET implementation can be envisaged.

6. Reliability

The Q_S-operated Z^2-FET has been measured under temperatures ranging from 25 °C to 105 °C, see Fig. 11a. The hysteresis window is hardly changed and the $|V_{ON}|$ decreases by only 0.12 V. Compared to the normal thyristor using bipolar action triggered by impact ionization [5], the Z^2-FET is relatively insensitive to temperature variation, thanks to the stable feedback process. We have also carried out preliminary reliability measurements by repeatedly cycling the device through the hysteretic loop: $|V_{ON}|$ decreases only slightly after 12,000 sweeps lasting for over 50 h, as shown in Fig. 11b, demonstrating good reliability for the prototype device.

7. DC model of Z^2-FET

We have developed a model of the feedback process in the Z^2-FET. The model uses a similar approach as standard thyristor modeling [19], except that impact ionization is not a factor and the doping-related bipolar action is replaced by the field-effect controlled diffusion. Fig. 12a schematically shows a simplified Z^2-FET structure without including the BOX. The device structure is similar to a p^+-n-p-n^+ thyristor, however the virtual doping in the L_G and L_{IN} regions is induced by the applied V_G and V_{BG} (or Q_S), respectively. Thus, the applied V_D drops at drain (V_{dj}), source (V_{sj}) and channel (V_{cj}) junctions. In the OFF state, the drain and source junctions are forward-biased, whereas the channel junction is reverse-biased.

Fig. 12a explicitly shows the feedback process, where the electron diffusion current (I_n) is controlled by the drain junction voltage (V_{dj}). The I_n flows into the source and induces a source junction voltage (V_{sj}). The V_{sj}, in turn, controls the hole injection current (I_p), which flows into the drain and induces V_{dj} affecting

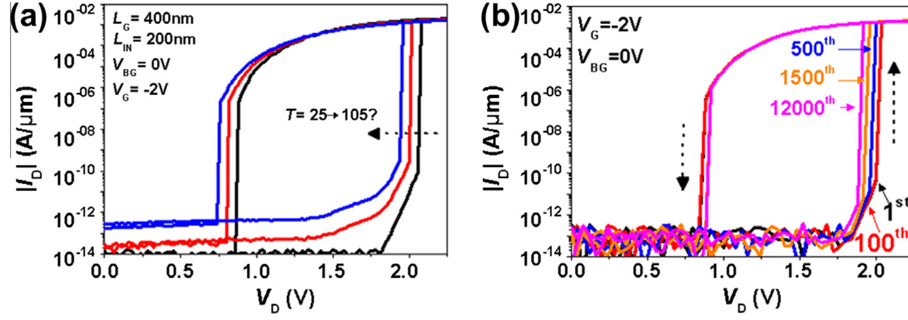

Fig. 11. Experimental I_D–V_D measurements on the Q_S-operated Z^2-FET under (a) temperature in the 25–105 °C range and (b) repeated sweeping through the hysteretic loop through 12,000 cycles lasting for over 50 h. The prototype device has parameters of L_G = 400 nm, L_{IN} = 200 nm, T_{ox} = 6 nm SiO_2, T_{Si} = 20 nm and T_{BOX} = 140 nm at fixed V_G = −2 V.

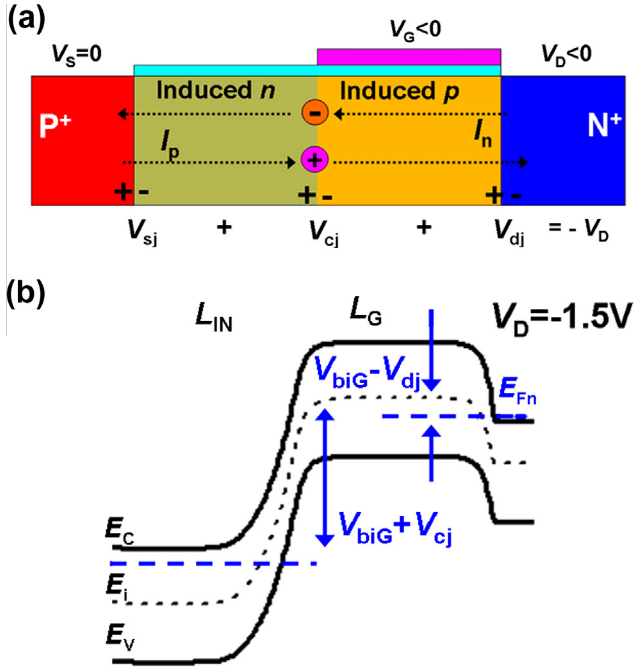

Fig. 12. (a) Simplified schematic view of the Z^2-FET without BOX. The applied drain voltage V_D drops at three junctions formed by field-induced carrier accumulation in L_G and L_{IN} regions; (b) simulated band diagram of the V_{BG}-operated Z^2-FET at V_D = −1.5 V.

the I_n. This forms a feedback loop which is modeled by four main equations including the generation of I_n and I_p by the V_{dj} and V_{sj}, respectively, and the formation of V_{dj} and V_{sj} by the I_p and I_n, respectively.

The diffusion current flow is controlled by the field effect due to the difference of Fermi levels in the channel, see Fig. 12b. It is modeled similarly to the subthreshold current in a MOSFET [20]. The I_n and I_p per unit gate width are given by:

$$I_n = I_{SG} \cdot \exp\left(\frac{V_{biG}}{V_T}\right) \cdot \left[\exp\left(\frac{V_{dj}}{V_T}\right) - \exp\left(-\frac{V_{cj}}{V_T}\right)\right] \quad (1)$$

$$I_p = I_{SI} \cdot \exp\left(\frac{V_{biI}}{V_T}\right) \cdot \left[\exp\left(\frac{V_{sj}}{V_T}\right) - \exp\left(-\frac{V_{cj}}{V_T}\right)\right] \quad (2)$$

where V_T is the thermal voltage defined by $V_T = kT/q$. Since both L_G and L_{IN} are small, the saturation currents I_{SG} and I_{SI} can be expressed by:

$$I_{SG} = \frac{q \cdot n_i \cdot D \cdot T_{si}}{L_G} \text{ and } I_{SI} = \frac{q \cdot n_i \cdot D \cdot T_{si}}{L_{IN}} \quad (3)$$

where n_i is the intrinsic carrier density and D is the appropriate diffusion coefficient. The V_{biG} and V_{biI} in Eqs. (1) and (2) are the built-in potentials that represent the field-induced equivalent doping in L_G and L_{IN} regions, respectively. They can be obtained using sheet charge approximation [21] as:

$$2 \cdot q \cdot T_{si} \cdot n_i \cdot \sinh\left(\frac{V_{biG}}{V_T}\right) = C_{ox} \cdot (V_G - V_D - V_{dj} - V_{biG}) + C_{BOX} \cdot (V_{BG} - V_D - V_{dj} - V_{biG}) \quad (4)$$

$$2 \cdot q \cdot T_{si} \cdot n_i \cdot \sinh\left(\frac{V_{biI}}{V_T}\right) = C_{BOX} \cdot (V_{BG} - V_{sj} - V_{biI}) \quad (5)$$

Given the currents in Eqs. (1) and (2), the junction voltage drops, V_{dj} and V_{sj}, induced by the flow of hole and electron into the drain and source, respectively, can be modeled as in a normal diode [20]:

$$V_{dj} = V_T \cdot \ln\left(\frac{I_p - I_{Rd}}{I_{Sd}} + 1\right) \quad (6)$$

$$V_{sj} = V_T \cdot \ln\left(\frac{I_n - I_{Rs}}{I_{Ss}} + 1\right) \quad (7)$$

where the I_{Rd} and I_{Rs} are the recombination currents in the drain and source junctions, respectively. They are determined by the trap density and energy level. For simplicity, the trap energy is assumed to lie at the middle of the bandgap, so they are approximated by [16]:

$$I_{Rd} = I_r \cdot \exp\left(\frac{V_{dj}}{2 \cdot V_T}\right) \text{ and } I_{Rs} = I_r \cdot \exp\left(\frac{V_{sj}}{2 \cdot V_T}\right) \quad (8)$$

The pre-factor I_r of the recombination current in Eq. (8) is defined as:

$$I_r = \frac{q \cdot n_i \cdot W_{dep} \cdot T_{si}}{\tau} \quad (9)$$

where the W_{dep} is the depletion width in source and drain junctions and τ is the carrier lifetime. The saturation current I_{Sd} and I_{Ss} in Eqs. (6) and (7), respectively, are expressed by:

$$I_{Sd} = \frac{q \cdot p_{n0} \cdot D \cdot T_{si}}{L_d} \text{ and } I_{Ss} = \frac{q \cdot n_{p0} \cdot D \cdot T_{si}}{L_s} \quad (10)$$

where the p_{n0} and n_{p0} are the equilibrium hole and electron concentration, L_d and L_s are the effective hole and electron diffusion lengths in drain and source, respectively, limited by the distance from junctions to source/drain electrodes.

Numerical methods can be used to solve the four main equations – Eqs. (1), (2), (6), and (7) – with the built-in potentials determined by Eqs. (4) and (5) for the V_{BG}-operated device. For the Q_S-operated device, the V_{biI} is taken to be 0.55 V, corresponding to

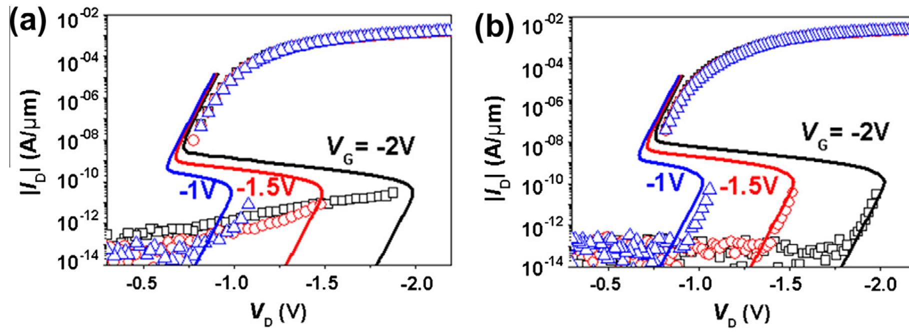

Fig. 13. Comparison between experimental data (open dots) and model (solid curves) for the p-type Z^2-FETs operating with (a) V_{BG} = 2 V and (b) Q_S.

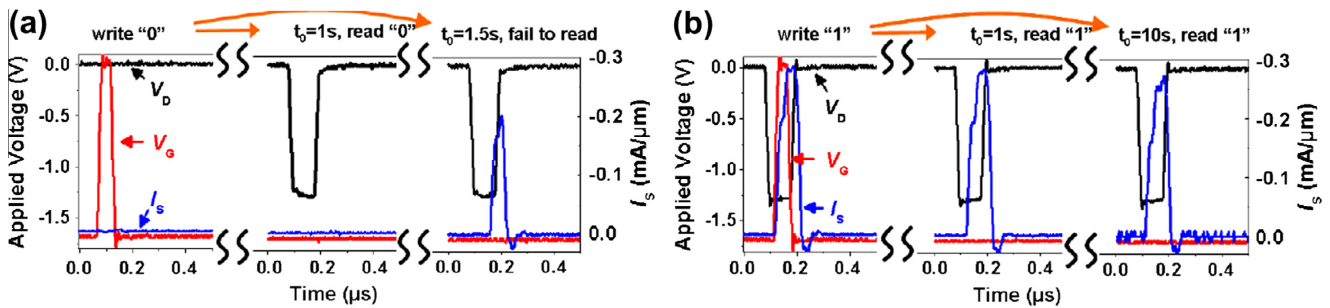

Fig. 14. Transient measurements show the DRAM operation of the Q_S-operated Z^2-FET. The device parameter is L_G = 400 nm, L_{IN} = 200 nm, T_{ox} = 6 nm SiO_2, T_{Si} = 20 nm and T_{BOX} = 140 nm. (a) The logic "0" is written by a V_G pulse and read out correctly by a V_D pulse after a delay of t_0 = 1 s, but not after t_0 = 1.5 s, due to limited retention time. (b) The logic "1" is written by simultaneous V_G and V_D pulses and read out correctly by V_D pulse after t_0 = 1 and 10 s (retention time is unlimited in logic "1").

strong electron accumulation in L_{IN} region. The saturation currents $I_{SG} = I_{SI}$, $I_{Sd} = I_{Ss}$ and I_r are used as fitting parameters. Fig. 13 compares the solution of the model with the experimental data on Z^2-FETs operating with V_{BG} (same device as Fig. 1) and Q_S (identical to Fig. 5, except with L_G = 400 nm). The model reproduces the V_G-controlled hysteresis very well. It also reproduces negative resistance region, agreeing with simulation in Fig. 3.

The feedback loop is initiated by the field-effect induced electron injection instead of impact ionization. The device is initially in OFF state, then as $|V_D|$ increases to around $|V_G|$ the L_G region is depleted, and thus the built-in potential V_{biG} increases almost linearly, according to Eq. (4). This exponentially increases the electron current from Eq. (1), which is captured by our model compared with the experimental Q_S-device, see Fig. 13b. This phenomenon is concealed by the gate leakage current in the V_{BG}-operated device, shown in Fig. 13a.

The developed model can be used for not only the Z^2-FET but also other field-effect controlled feedback devices, such as FED and FB-FET [6–9].

8. Z^2-FET applications: 1T-DRAM and 1T-SRAM

The conventional dynamic random access memory (DRAM) using an external capacitor for charge storage has been a successful technology for several decades, exhibiting high integration density and good reliability, but suffering from low access speed and difficult capacitor scaling [22]. The static random access memory composed of six transistors, on the other hand, has high access speed but low integration density [23]. Memory devices that can provide both high integration density and high speed are thus of great interest. Thanks to the good reliability and V_G-controlled hysteresis, Z^2-FET is suitable for 1T-DRAM application using the transient feedback effect. The device has no external capacitor and the fabrication is compatible with the SOI process [12].

The charge is stored on the front gate capacitor (C_G) to represent the logic states, with logic "1" corresponding to high charge storage. The logic state is read out by a negative V_D pulse with short rise/fall time (t_f = 15 ns in the experiment, limited by our equipment), which, for logic "1", discharges the holes stored in C_G through the forward-biased drain junction and triggers the feedback to turn on the device. No charge is stored in logic "0", and thus after the V_D pulse the device remains in the OFF state. The writing of "0" and "1" uses V_G and V_D pulses to discharge and recharge the C_G, respectively, as described in detail in [12]. Fig. 14 shows the operation waveform of the Z^2-FET DRAM. The V_G is pulsed from −1.7 V to 0, with V_D kept at 0, to discharge the C_G. The reading pulse correctly outputs low current after 1 s, see Fig. 14a. However, due to the recharging of the C_G through the leakage current of the reverse-biased drain junction, the read outputs high currents after 1.5 s indicating the limited retention time of logic "0". Conversely, for logic "1", V_G and V_D are pulsed simultaneously to turn on the device and store charge on C_G. This logic "1" state is stable and requires no refreshing, as shown in Fig. 14b for a reading pulse after 10 s.

The Z^2-FET DRAM can operate with the supply voltage down to 1.1 V, lower than the conventional 1T-1C DRAM and floating body memories [24], see Fig. 15. The scaling of V_G and V_D also reduces the leakage current in drain junction, and thus prolongs the retention time to 5.5 s, albeit with reduced read-out current (∼100 μA/μm) for logic "1", see Fig. 15b.

The V_{BG}-operated device can also be used as 1T-DRAM with the same operating principle, shown in Fig. 16a. Using V_{BG} instead of Q_S may be advantageous in reliability. The dashed curve in Fig. 16a shows the preliminary reliability test, where no significant degradation in output current is observed after 6×10^{10} write/read cycles. Since the reliability of the V_{BG}-operated Z^2-FET is only limited by the degradation of gate oxide, the Z^2-FET should, in principle, be as reliable as a conventional MOSFET with a comparable gate stack and low-voltage operation.

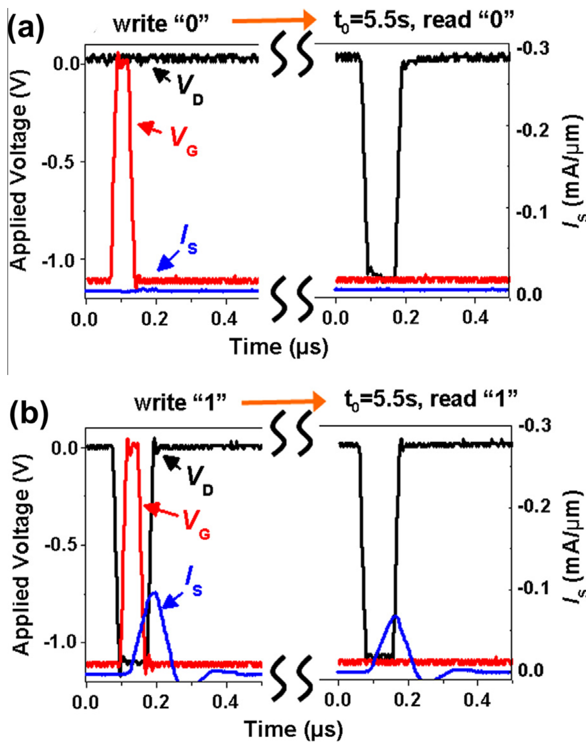

Fig. 15. Transient measurements show the Z^2-FET DRAM in Fig. 14 operates under $|V_{DD}|$=1.1 V with retention prolonged to 5.5 s, albeit with lower current for logic "1".

The access time of the logic "1" in Z^2-FET DRAM is limited by the establishment of the electron–hole plasma in the channel. Conversely, the speed of writing logic "0" depends on the discharging of the front gate capacitor through the forward-biased drain junction and is limited by the *RC* time constant, which is <1 ns for our device geometry. Compared to the 1T-1C DRAM, where large amount of charge is required to drive the external amplifier, the Z^2-FET DRAM needs less charge storage ΔQ_G because of its internal feedback amplification. Basically, the memory effect is triggered not by ΔQ_G as in SOI 1T-DRAMs [24–27] but by the induced discharge current $\Delta Q_G/\Delta t$. This way, we can decrease the stored charge ΔQ_G simply by reducing the readout time Δt. This enhances the access speed and reduces the dynamic power consumption. In simulation the Z^2-FET DRAM operates with read/write times as short as 1 ns, outperforming 1T-1C and floating body DRAMs [22,24], see Fig. 16b.

The Z^2-FET can be directly used as static random access memory (SRAM) using the V_G-controlled hysteresis in I_D–V_D domain (Fig. 1). Fig. 17 shows the operation waveform of the SRAM using the same Z^2-FET as in Fig. 14. Both logic "0" and "1" have an infinite retention time and are read out correctly after 100 s. Compared to DRAM operation shown in Fig. 14, the logic states in SRAM mode are held at $|V_D|$ = 1 V and read out at $|V_D|$ = 1.3 V.

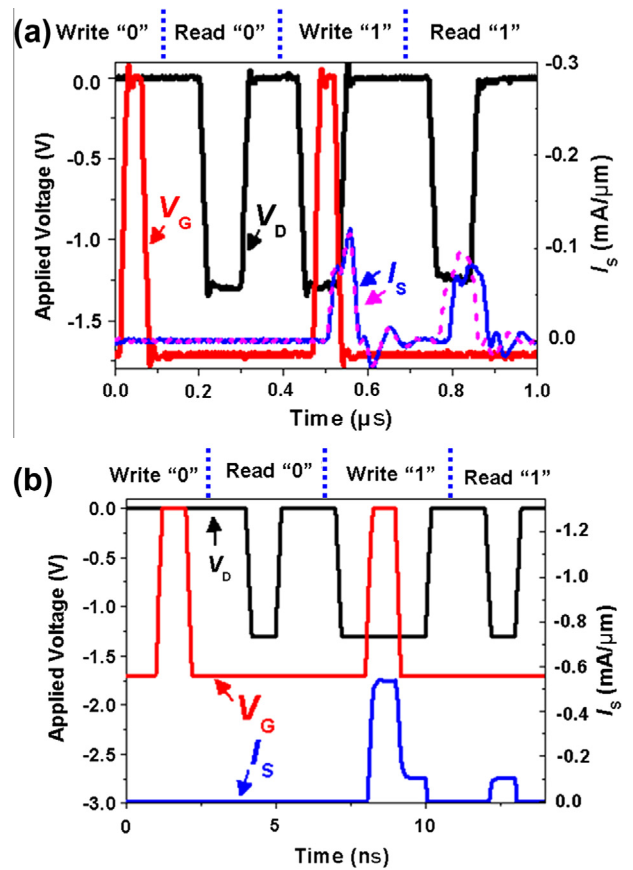

Fig. 16. (a) Experimental operation waveform of the DRAM using V_{BG}-operated Z^2-FET. The dashed curve shows the output current after 6×10^{10} write/read cycles. The device has the same dimension as in Fig. 1b; (b) simulated operation of Z^2-FET DRAM demonstrating read/write time down to 1 ns.

The disadvantage of the 1T-SRAM is the significant static current and power consumption for holding logic "1", see Fig. 17b. To reduce the hold current for logic "1", two different methods can be envisaged. Fig. 18a shows the I_D–V_D hysteresis of the Q_S-operated Z^2-FET as a function of V_{BG}. Compared to V_{BG} = 0, $|V_{ON}|$ increases with $V_{BG} = -10$ V due to the interchannel coupling in the L_G region. The negative V_{BG} also reduces the hole injection barrier in the L_{IN} region, and thus provides large feedback gain even under relatively low current. The resulting hold current, denoted I_h in Fig. 18a, is reduced from 10^{-6} A/μm to 10^{-10} A/μm.

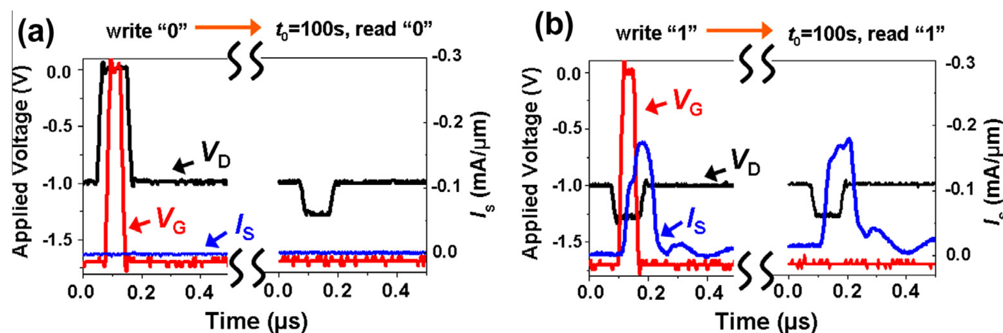

Fig. 17. Operation waveform of the SRAM using Q_S-operated Z^2-FET for (a) "0" and (b) "1" logic states. Compared to the DRAM, the SRAM logic states need no refreshing.

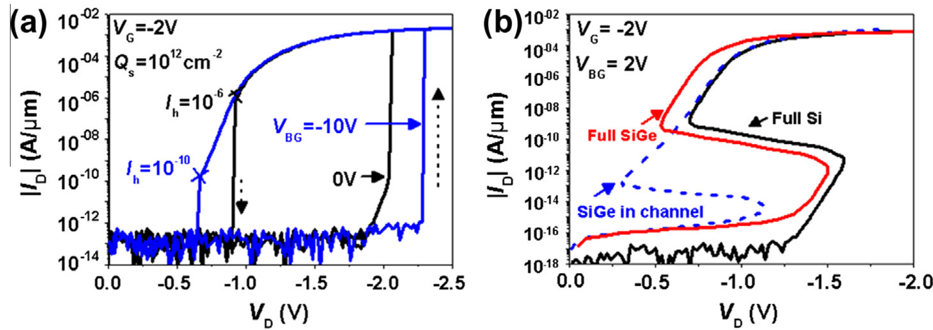

Fig. 18. Reduction of holding current I_h by (a) combining the Q_S and V_{BG} to adjust the injection barrier (experiment) and (b) using $Si/Si_{0.7}Ge_{0.3}$ heterojunction to enhance the injection coefficient (simulation).

An alternative method to reduce I_h is to use a heterojunction device. Fig. 18b shows the I_D–V_D simulations of V_{BG}-operated Z^2-FETs with an advanced structure of L_G = 50 nm, L_{IN} = 50 nm, T_{ox} = 1 nm SiO_2, T_{Si} = 5 nm and T_{BOX} = 20 nm, and employing combinations of Si and $Si_{0.7}Ge_{0.3}$ materials in the channel and source/drain regions. We find that when the Z^2-FET uses either Si or $Si_{0.7}Ge_{0.3}$ in both channel and source/drain regions, the I_h remains approximately the same. But when the channel is made of $Si_{0.7}Ge_{0.3}$ and source/drain regions are Si, I_h is markedly reduced thanks to higher injection coefficient in $Si/Si_{0.7}Ge_{0.3}$ heterojunction [28]. Even so, the leakage current is much higher than in conventional 6T-SRAM and the use of the Z^2-FET in SRAM mode would only make sense in applications where space is a greater constraint than power consumption.

9. Conclusions

In this paper, we presented a systematic study of a new, compact sharp-switching device we have named the Z^2-FET. Our device is fully compatible with SOI fabrication, has a single front gate, can be operated with either a back gate bias V_{BG} or dielectric stored charge density Q_S, shows very high $I_{ON}/I_{OFF} > 10^8$ ratio and a near-zero subthreshold swing SS < 1 mV/dec. The device also exhibits voltage-controlled hysteresis in I_D–V_D domain with V_{ON} linearly controlled by V_G. The operation of the Z^2-FET, as confirmed by TCAD simulations, involves positive feedback between carrier flow and carrier injection barriers, with no need for impact ionization. The device is scalable down to 30 nm (20 nm in an advanced structure with non-overlapping gates) and shows good temperature stability and reliability. We also have developed an analytical model using field-effect controlled diffusion that reproduces our experimental results. The Z^2-FET can be used as a high-speed 1T-DRAM with V_{DD} down to 1.1 V, retention time up to 5.5 s and simulated write/read time down to 1 ns. The application as 1T-SRAM is promising for its ultra-compact device structure, albeit with static power consumption that can be reduced by combining V_{BG} and Q_S or by using $Si/Si_{0.7}Ge_{0.3}$ heterojunction between the channel and the source/drain regions. Further applications are related to surface-charge sensing and ESD protection schemes.

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