Top-Gated Indium–Zinc–Oxide Thin-Film Transistors With *In Situ* Al_2O_3/HfO_2 Gate Oxide

Yang Song, Rui Xu, Jian He, Stylianos Siontas, Alexander Zaslavsky, and David C. Paine

***Abstract*— We report on top-gated indium–zinc–oxide (IZO) thin-film transistors (TFTs) with a 3-nm layer of aluminum between the IZO active layer and high-*k* HfO_2 gate insulator. A series of anneals at 300 °C was used to convert the Al metal into Al_2O_3, resulting in high-performance top-gated TFTs. The 8-h-annealed TFT with Al layer has a threshold voltage $|V_T| < 0.5$ V, an ON/OFF ratio of 1×10^7, a subthreshold slope (SS) of 0.14 V/decade, and a saturation mobility $\mu_S \sim 115$ cm^2/V · s in devices with $L_G = 50$ μm gate length. For smaller devices with $L_G = 5$ μm, the threshold voltage and SS are similar, but the ON/OFF ratio and mobility are lower. Cross-sectional TEM images and C–V_G characteristics with little hysteresis confirm that the thin Al layer, converted *in situ* into Al_2O_3, can protect the IZO channel during processing and produce a good high-*k* gate-stack.**

***Index Terms*— Indium zinc oxide, thin film transistors, *in-situ* process, top gate, aluminum oxide.**

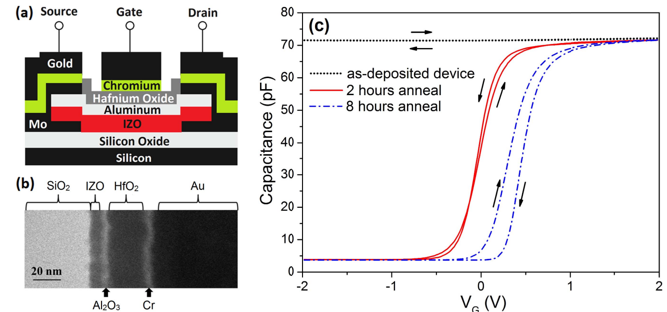

Fig. 1. (a) Schematic of the as-deposited TFT structure with a thin Al metal layer between the IZO channel and HfO_2 gate insulator. (b) Gate area cross-sectional TEM image of 8-hour-annealed TFT with the Al interlayer converted to Al_2O_3. (c) C-V_G curves of large-area TFTs ($W/L_G = 250/50$ μm) with Al layer at 0 (as-deposited), 2 hour and 8 hour anneal times. The gate voltage is swept up from –2 V to 2 V and then back. All curves are measured using a 100 kHz ac signal.

I. Introduction

WITHIN the last decade, after the initial report by Nomura *et al.* in 2004 [1], oxide semiconductors have become one of the main materials for high-performance TFTs. Indium- and zinc-oxide based amorphous TFTs—such as In-Zn-O (IZO) [2], In-Ga-Zn-O [3], [4], Zn-Sn-O [5]—have been widely studied for display applications [6]. The requirements of TFTs to be used in active matrix liquid crystal displays include: a field effect mobility $\mu > 1$ cm^2/V·s, an on/off ratio $> 10^6$, low temperature processing, and low fabrication costs [7]. The field effect mobility of indium- and zinc-oxide compounds easily meets the mobility requirement, and many of the amorphous oxide TFTs can be fabricated at low temperature on arbitrary substrates. Besides the application in displays, the same advantages of amorphous oxide materials, such as high mobility and arbitrary substrate capability, make them potentially suitable for top-gated high-current low-cost radio frequency (RF) transistors [8]. To make such RF devices, one must obtain an appropriate dielectric gate stack with low leakage, high dielectric constant and good interface with amorphous oxide channel material. In this letter, we demonstrate a way to form a dielectric gate stack by using an *in-situ* metal oxidation process.

Our top-gated IZO TFTs, with channel material deposited by sputtering a 90 wt.% In_2O_3-10 wt.% ZnO target, feature an *in-situ* formed Al_2O_3 interlayer between the IZO channel and the HfO_2 high-*k* gate insulator. A schematic of the as-deposited TFT structure is shown in Fig. 1(a), with a thin layer of Al metal (2–3 nm) between the IZO and the HfO_2 that confers two advantages. First, the Al layer serves as a protective layer to minimize the bombardment from O and Ar ions during the atomic layer deposition (ALD) of HfO_2, and thus minimize the damage to the IZO channel, which has been reported as a failure mode in top-gated oxide TFTs [9]. Second, when the TFTs are annealed, the Al layer is converted into Al_2O_3, and this Al_2O_3 can suppress the charge trapping at the IZO/HfO_2 interface [10], [11]. Compared to the sputter-deposition of the Al_2O_3 interlayer reported by Chang *et al.* [11], our *in-situ* oxidation of Al into Al_2O_3 is advantageous because it can protect the oxygen-sensitive IZO from oxygen-containing deposition environment.

The *in-situ* formation of dielectric oxide is a consequence of the thermodynamic instability of many metals (Al, Ti, Hf, and others) in contact with In_2O_3 (and ZnO). As discussed in [12], this instability can be predicted from the free energy of formation values of the oxides to calculate the free energy of the overall reaction. In this case, the direction (forward or reverse) of the reaction $2Al + In_2O_3 = Al_2O_3 + 2In$ is predicted by subtracting the free energy of formation of In_2O_3 from Al_2O_3: $\Delta G = \Delta G^F_{Al2O3} - \Delta G^F_{In2O3}$. At 200 °C, the result is reported [12] to be negative (−752.6 kJ/mol) which indicates that, in the absence of kinetic constraints, Al metal will oxidize by chemically reducing In_2O_3 to produce

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Al_2O_3. In our TFTs, the Al metal layer is thin (2–3 nm, of which ~1 nm would be consumed by the native oxide formed on the Al surface prior to ALD of HfO_2) and was deposited on a ~10 nm IZO layer sputtered in an oxygen-rich ambient to produce fully oxidized stoichiometric In_2O_3. The IZO thickness was chosen to ensure that the underlying IZO was not fully consumed. Instead, the oxygen extracted by the Al oxidation is expected to create an oxygen vacancy-rich sub-stoichiometric oxide, effectively doping the IZO channel [13].

II. EXPERIMENT

The fabrication sequence for the TFTs shown in Fig. 1(a) ran as follows. We started with a Si wafer coated with 500 nm of thermal SiO_2. The source and drain electrodes, active layer and top gate electrode were all patterned using conventional lift-off process. First, 10 nm Mo was deposited on source/drain areas at room temperature via dc magnetron sputtering. Then a ~10 nm IZO channel layer was deposited using dc magnetron sputtering with an 86/14 Ar/O_2 gas volume ratio and a power density of 0.22 W/cm^2 at a 280 V dc bias. Then a 2–3 nm Al layer was sputter-deposited onto the IZO layer. The sample was transferred into a metallization tool, where we deposited 10 nm of sputtered Mo (contact metal), 10 nm Cr (adhesion layer) and 70 nm Au (probing metal) by e-beam evaporation. Then 25 nm of HfO_2 was deposited by ALD from an $Hf(N(CH_3)_2)_4$ precursor at 200 °C, using 300 W oxygen plasma in Ar ambient. The ALD-deposited HfO_2 was removed from the Cr/Au source/drain metal and, finally, the 10/70 nm Cr/Au gate metal was deposited via e-beam evaporation. We made TFTs with width to gate length (W/L_G) ratios of 15/5 μm and 250/50 μm. These TFTs were measured in as-deposited form and after anneals at 300 °C in atmosphere (to convert the Al interlayer to Al_2O_3). Control samples with the same fabrication sequence but no Al layer between the IZO channel and HfO_2 gate insulator were also fabricated. A cross-sectional TEM image of the layers under the gate of an annealed TFT, produced using a focused ion beam (FEI NOVA NanoLab 600i) is shown in Fig. 1(b).

III. RESULTS AND DISCUSSION

The gate capacitance of large-area ($W/L_G = 250/50$ μm) TFTs containing a thin Al layer was measured as a function of anneal time in a light-tight box using a 100 kHz ac signal. During C-V_G measurements, the source, drain and substrate were all grounded, and V_G was swept up from −2 V to 2 V and then down. Fig. 1(c) demonstrates the obtained C-V_G curves for anneal times of zero (as-deposited), 2 hours and 8 hours. As-deposited devices exhibit constant C independent of V_G, as the thin remaining Al layer screens the IZO channel. The constant C makes it possible to infer the dielectric constant of HfO_2 as ~16 (with a slight uncertainty introduced by the Al native oxide). When the device is annealed, the Al is transformed into Al_2O_3 and the C-V_G curves reveal gate control and full depletion of the IZO channel. Fig. 1(b) shows the cross-sectional TEM image of the gate area of an 8-hour-annealed TFT, confirming the existence of an *in-situ* layer of Al_2O_3 of ~5 nm thickness. The HfO_2/Al_2O_3 dielectric stack can be modeled as two capacitors in series. In accumulation, $V_G > 1$ V, C reaches a constant C_{MAX} that decreases slightly from the as-deposited value as the Al layer turns into Al_2O_3. Conversely, in depletion, $V_G < -1$ V, the annealed devices exhibit a minimum capacitance ($C_{MIN} \sim 3.7$ pF) corresponding to the total capacitance of the serially connected gate insulator, fully depleted IZO layer, and the buried SiO_2 layer (together with parallel capacitance from the 150×150 μm gate contact pad directly on the buried SiO_2 layer). The hysteresis observed in the C-V_G curves of annealed devices is very small in 2-hour-annealed TFTs and larger in 8-hour-annealed TFTs, see Fig. 1(c). Estimating the interface trapped charge density N_{TC} as $C_{MAX} \times \Delta V_G/q$, where $\Delta V_G \sim 0.2$ V is the width of the hysteresis loop and q is the electron charge, yields $N_{TC} \sim 3.6 \times 10^{12}$ cm^{-2}, comparable to reported results on HfO_2 gate insulators on IZO [14] or IGZO [15]. The trapped charge may result from the formation of vacancies or vacancy clusters due to the Al/IZO reaction. Further study of the *in-situ* Al_2O_3/IZO annealed interface is needed to explain our C-V_G data and the observed TFT threshold shift.

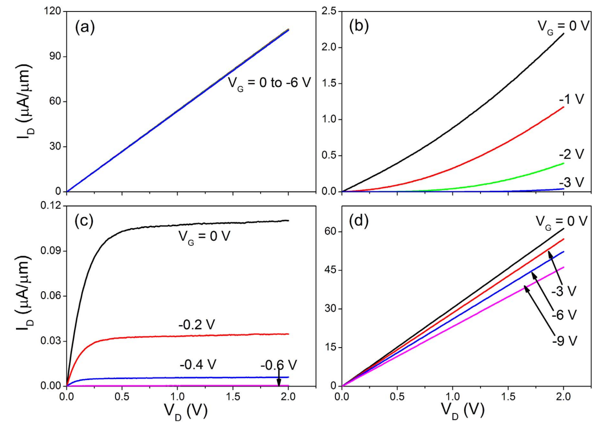

Fig. 2. I_D-V_D characteristics of $L_G = 5$ μm TFT: (a) as-deposited TFT with Al layer, $V_G = 0$ to -6 V with a step of -2 V; (b) annealed for 2 hours at 300 °C, $V_G = 0$ to -3 V with a step of -1 V; (c) annealed for 8 hours at 300 °C, $V_G = 0$ to -0.6 V with a step of -0.2 V, showing fully saturating output characteristics; (d) as-deposited control TFT with no Al layer, $V_G = 0$ to -9 V with a step of -3 V. Annealing does not alter the output characteristics of TFTs with no Al layer.

The corresponding TFT characteristics are shown in Fig. 2, measured with the substrate grounded. Fig. 2(a) shows the I_D-V_D output curves of as-deposited TFTs with the Al layer. As a result of the Al, there is no gate control for the as-deposited device even at large V_G = –6 V, in agreement with the constant C-V_G curves. When the devices are annealed, the Al layer is converted to Al_2O_3, resulting in gate-controlled TFTs. As shown in Fig. 2(b), the devices annealed for 2 hours exhibit transistor characteristics; after an 8 hour anneal the TFTs show fully saturating output characteristics and can be pinched off at low V_G < –1 V, see Fig. 2(c).

For comparison, Fig. 2(d) shows the output curves of control TFTs fabricated in the same process without the thin Al interlayer. These TFTs show some gate control, but they cannot be fully pinched off (even when $V_G \leq$ –9 V) and their characteristics are not improved by annealing. The inferior performance of control TFTs is likely due to the damage

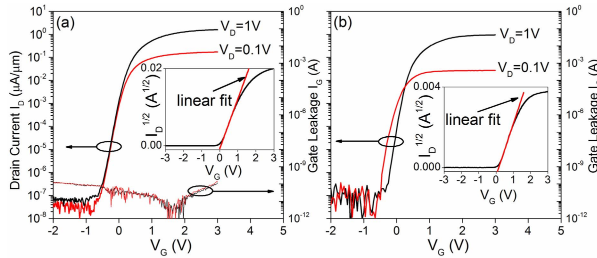

Fig. 3. Transfer characteristics of 8-hour-annealed TFTs with Al: (a) $W/L_G = 250/50$ μm; (b) $W/L_G = 15/5$ μm. Inset shows ${I_D}^{1/2}$ *vs.* V_G plot for V_T and field mobility extraction at $V_D = 1$ V. The gate leakage I_G for the larger transistor is also shown.

to the IZO channel during HfO_2 deposition and the inferior IZO/HfO_2 interface without the Al_2O_3 interlayer.

Transfer characteristics of Al-layer-containing TFTs with $W/L_G = 250/50$ and $15/5$ μm after an 8-hour anneal are compared in Fig. 3. All the transfer curves were measured with V_G swept from positive to negative with negligible gate leakage ($< 10^{-10}$ A for the large transistor, see Fig. 3(a), and $< 5 \times 10^{-11}$ A for the small transistor). In the $L_G = 50$ μm TFT in Fig. 3(a), the on/off current ratio exceeds 10^7, and SS ~ 0.14 V/decade, with no measurable threshold shift as V_D is changed from 0.1 to 1 V. One can estimate the saturation mobility μ_S and threshold voltage V_T by the standard ${I_D}^{1/2}$ *vs.* V_G technique [16],

$$I_D = \mu_S \times C_{ox} \times (W/2L_G) \times (V_G - V_T)^2,$$

to obtain $\mu_S \sim 115$ cm^2/V·s at $V_D = 1$ V and $V_T \sim 0.06$ V, which matches the threshold voltage from C-V_G curves – see inset in Fig. 3(a). In the smaller $L_G = 5$ μm TFT shown in Fig. 3(b), the saturation mobility, on/off ratio, V_T and subthreshold slope are estimated at 6.7 cm^2/V·s, 0.13 V, 2.6×10^6 and 0.14 V/decade.

The mobility of $L_G = 50$ μm TFTs is high, but similar values were recently reported in large top-gated IZO-based TFTs [17] (and Al-doped ZnO TFTs [18], although those devices had crystalline channel material). The estimated μ_S of $L_G = 5$ μm TFTs is much lower, possibly due to source contact resistance or increased scattering due to interface diffusion of metal from the contacts (which is still under investigation), but even so the $L_G = 5$ μm TFTs provide similar maximum I_D and a slightly better subthreshold slope compared to $L_G = 50$ μm TFTs. In both large and small TFTs, the SS and on/off ratio are very good, comparable to the best reported values.

The measurements on the annealed Al-layer-containing TFTs were taken within two weeks after fabrication, as the device characteristics then begin to degrade in these non-encapsulated prototype devices.

IV. Conclusions

We fabricated top-gated IZO TFTs with 3 nm Al metal layer between IZO channel and high-k HfO_2 gate dielectric. We have shown that annealing at 300 °C converts the Al layer into Al_2O_3, resulting in TFTs that show good characteristics with a low $|V_T| < 0.5$ V, on/off ratios larger than 10^7, and a subthreshold slope of 0.14 V/decade. The estimated saturation mobility μ_S of large $L_G = 50$ μm TFTs is very high at 115 cm^2/V·s, whereas μ_S in small $L_G = 5$ μm TFTs is lower, possibly due to contact resistance. Our *in-situ* approach to producing a thin Al_2O_3/ HfO_2 high-k stack with low leakage and trapped charge is promising for high-performance submicron oxide TFTs.

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