Beyond TFET: Alternative Mechanisms for CMOS-Compatible Sharp-Switching Devices

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***Abstract*—Tunneling-based transistors (TFETs) have attracted interest due to their (theoretical) capability of switching more sharply than MOSFETs. However, other mechanisms that take place in SOI devices can provide even more abrupt switching and higher current. We examine the family of emerging TFET-competing devices based on barrier modulation, bipolar amplification and impact ionization. Practical results for devices fabricated in 14-28 nm FDSOI technology will be discussed.**

Keywords—FDSOI; CMOS; TFET, BET-FET; Z^2-FET; sharp switching, tunneling

I. Introduction

MOSFET scaling requires maintaining both a high ON current I_{ON} for speed and a low OFF current I_{OFF} to limit standby power consumption. The reduction of the supply voltage V_{DD} is impeded by the subthreshold slope which cannot be lowered below S = 2.3(kT/q) ~ 60 mV/decade at room temperature, even in ideal fully-depleted MOSFETs. This explains the growing interest in CMOS-compatible devices that switch more abruptly than MOSFETs [1].

We briefly review the mechanisms that offer abrupt switching between OFF and ON states in SOI transistors: floating body, coupling, band-to-band tunneling and impact ionization. A typical device is the I-MOS [2], studied a decade ago and abandoned because of poor scalability, unacceptably high V_{DD} and lack of reliability.

Tunneling FETs (TFETs) are not limited by S > 60 mV/decade, because the current is carried by V_G-controlled tunneling of carriers through the bandgap, rather than injection over a potential barrier. Today, state-of-the-art CMOS-compatible TFETs can provide S < 60 mV/decade over a narrow range of V_G but have difficulty in reaching a competitive I_{ON}. We will show recent progress in current drive capability achieved by combining SOI and SiGe technologies (Fig. 1) [3].

In this paper, we focus on alternative sharp switching devices with potential to surpass the performance of TFETs.

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II. BET-FET

We will discuss a proposed innovation: a bipolar-enhanced TFET (BET-FET) structure, in which the tunneling current is amplified by the gain of a heterojunction bipolar transistor [4]. The TFET and the bipolar junction are co-integrated in a single monolithic device (Fig. 2).

The simulated performance in Si/SiGe BET-FET structures is unrivalled by any other type of TFET: I_{ON} higher than 1 mA/um and sub-60 mV/dec subthreshold swing over 7 decades. The BET-FET is, in principle, compatible with other promising material systems (such as staggered GaSb/InAs heterostructures).

III. Barrier Modulation Devices

A different approach to sharp-switching transistors is based on devices with internal positive feedback combined with potential barrier modulation. Like TFETs, they have a gated-diode configuration, but are operated in forward-bias mode. Electrostatic barriers are formed (via gate biasing or channel doping) to prevent electron/hole injection into the channel until the gate or drain bias reaches a turn-on value. Once injection into the channel begins, the electrons modulate the hole injection barriers and vice versa, leading to abrupt switching (S < 1 mV/decade) to a high I_{ON} corresponding to a forward-biased diode.

The family of feedback barrier-modulation devices includes several SOI designs:

- Field-effect diode (FED) with two adjacent top gates [5],
- Thyristor-like structures with specific dual body doping and control via ground-plane bias [6],
- Z^2-FET (zero swing and zero impact ionization FET) which has an underlapped top gate and additional control from the ground plane [7].

We will discuss in detail the device physics, architecture, and technology boosters for the most promising variant (Z^2-FET). The Z^2-FET features a large hysteresis useful for single-

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transistor DRAM and SRAM cells [7], as well as ESD protection [6].

Experimental and simulation results for the 28 nm and 14 nm FD-SOI technology nodes will be documented.

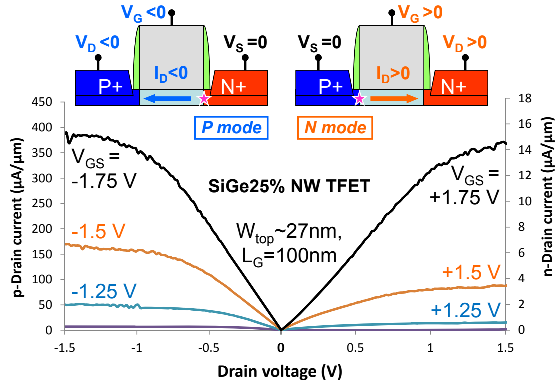

Fig. 1: SiGe/SOI nanowire TFET showing high ON current [3].

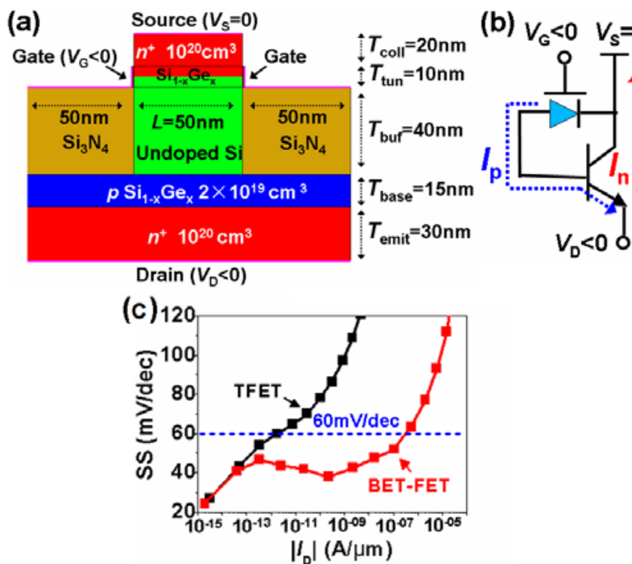

Fig. 2: (a) Configuration of the bipolar-enhanced TFET, (b) equivalent circuit and (c) typical simulated performance [4].

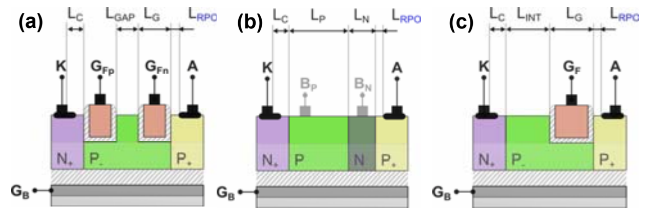

Fig. 3: Configuration of several barrier-modulation devices on FD-SOI: (a) field-effect diode (FED) [5], (b) back-bias-controlled thyristor [6] and (c) Z^2-FET [6].

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