Solid-State Electronics 97 (2014) 23–29

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Z^2-FET: A promising FDSOI device for ESD protection

Yohann Solaro [a,b,c,*], Jing Wan [c], Pascal Fonteneau [a], Claire Fenouillet-Beranger [b], Cyrille Le Royer [b], Alexander Zaslavsky [d], Philippe Ferrari [c], Sorin Cristoloveanu [c]

[a] STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France
[b] Univ. Grenobles Alpes, F-38000 GRENOBLE, France, CEA, LETI, MINATEC Campus, F-38054, Grenoble, France
[c] University Grenoble Alpes, CNRS, IMEP-LAHC, France
[d] School of Engineering, Brown University, Providence, RI 02912, USA

ARTICLE INFO

Article history:
Available online 17 May 2014

The review of this paper was arranged by Costin Anghel

ABSTRACT

In this work, the use of the Z^2-FET (Zero subthreshold swing and Zero impact ionization FET) for Electro-Static Discharge (ESD) protections is demonstrated. The device, fabricated with Ultra-Thin Body and Buried Oxide (UTBB) Silicon-On-Insulator technology, features an extremely sharp off-on switch and an adjustable triggering voltage (V_{t1}). The principle of operation, relying on the modulation of electron and hole injection barriers, is reviewed. The impact of process modules and design parameters on electrical characteristics is analyzed with TCAD simulations, showing that very low leakage current (I_{leak}) and triggering capability adapted to local protection schemes are achievable. Experimental results validate the possible use of this device as an ESD protection in the 28 nm FDSOI technology.

© 2014 Elsevier Ltd. All rights reserved.

1. Introduction

The protection of CMOS circuits against Electro Static Discharges (ESD) is a major concern for the IC industry in order to avoid reliability issues. When an ESD event occurs, the current should not reach the core MOSFETs transistors but must be deviated through protection devices. Various degradation or destruction mechanisms can directly be attributed to ESD events including degradation of the core MOSFETs characteristics (transconductance and threshold voltage), gate oxide rupture or thermal failure due to excessive current flow in the channel [1]. On the one hand, Fully Depleted SOI (FDSOI) is an efficient alternative to bulk technology to enhance the electrostatic control of the gate on the MOSFET channel, needed to pursue the CMOS scaling beyond 22 nm node [2]. On the other hand, the Buried Oxide (BOX) is suspected to prevent heat dissipation from the SOI film into the substrate, leading to reduced current handling (I_{t2}) capability during ESD [3].

Traditional power devices used in ESD protections, with vertical current paths such as Silicon Controlled Rectifiers [4,5] are not directly implementable in SOI due to the BOX layer vertical isolation. In addition, the ESD design window is reduced for thin Si films because the parasitic Bipolar Junction Transistor (BJT) in core design or in Input/Output MOSFETs is triggered earlier as compared to bulk [6,7]. That means the protection should be able to maintain the voltage drop during an ESD event between 1 V (V_{dd}) and a reduced high value of ~3 V. Below V_{dd}, the protection should be in high impedance mode, preventing any current leakage and unnecessary power consumption.

To design ESD protections, two strategies are possible: local or global [8]. They are represented in Fig. 1. Global schemes rely on complex current paths with several clamps dispatched in the whole circuit: typically a forward biased diode (only during an ESD event), and a central clamp between a power rail and the ground. The central clamp is a power switch designed to evacuate the high current of the ESD discharge with a very limited voltage drop. By contrast, local strategy uses only one clamp to directly shunt the ESD current to ground, avoiding unnecessary series resistances (caused by the power bus interconnections in the "global current path"). The need of a local protection device to address these challenges is evident and is not fulfilled by standard devices such as SOI-GGNMOS [9] which exhibit holding voltages in the same range as the core FDSOI-MOSFETs to be protected [6].

Recently, the Z^2-FET (Zero Impact Ionization and Subthreshold Slope FET) has been proposed for logic and memory (1T-DRAM) applications [10]. Promising performances have been demonstrated in terms of ultra-steep switching [11]. This device, as opposed to the Lateral SOI-SCR (Silicon Controlled Rectifier) [12,13], does not use avalanche for the triggering, and does not require accurate doping optimization of the BJT bases. It is quite similar to the Field Effect Diode [14–17] which uses two front gates

* Corresponding author at: STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France.
E-mail address: costin.anghel@isep.fr (Y. Solaro).

http://dx.doi.org/10.1016/j.sse.2014.04.032
0038-1101/© 2014 Elsevier Ltd. All rights reserved.

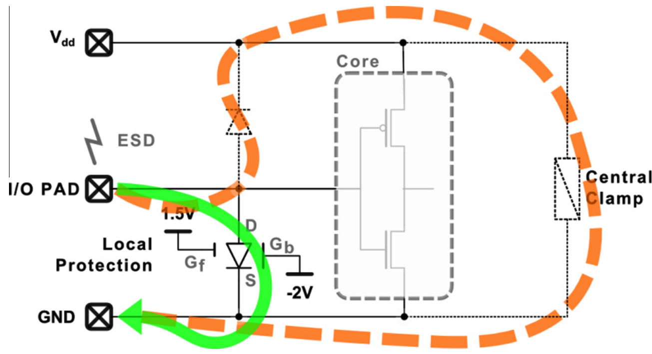

Fig. 1. Local (green, plain) and global (red, dashed) ESD protection schemes: global strategy relies on several clamps dispatched in the circuit and consequent bus series resistance. Local strategy is simpler and avoids complicated and resistive current paths. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

instead of one and a thicker body (Partially Depleted) SOI technology.

The paper is organized as follows. First, the structure and operation of the Z^2-FET is presented. Then, the dependence of leakage current I_{leak} and triggering voltage V_{t1} on design and process parameters is explored with simulations. Finally, the electrical properties of the device such as configurable V_{t1} are experimentally validated, in a 28 nm FDSOI technology.

2. Device and technology description

The Z^2-FET structure is a slightly modified P–I–N gated-diode, with an ultrathin body (7 nm for the 28 nm technology node [18,19]). The deviation from standard gated diode is that the front gate (G_f) is only partially covering the channel. The device topology is presented in Fig. 2. No other modification from standard CMOS FDSOI process [19] is necessary to fabricate the Z^2-FET. The anode (P+) of the P–I–N diode acts as the drain (connected to the I/O pad), and the cathode (N+) as the source. The (High-K + Metal) gated area has a L_G length and the uncovered area has a length L_{int} (intrinsic length). The whole channel, constituted by $L_G + L_{int}$ was left undoped (P-type, with $N_A = 10^{15}$ cm^{-3}). The Si epitaxy (raised sources and drains, needed for reduced series resistance [20]) is performed on all un-gated areas, so the L_{int} region has a final thickness of $t_{Si} + t_{epi} = 22$ nm, as opposed to the ultrathin body in the gated area ($t_{Si} = 7$ nm). Below the structure, a thin BOX ($t_{BOX} = 25$ nm) isolates the SOI film from the back gate (made with a highly doped P-type Ground Plane implantation: $N_{A\ GP} \approx 10^{18}$ cm^{-3}).

3. Simulations

The simulations were conducted with Synopsis software.

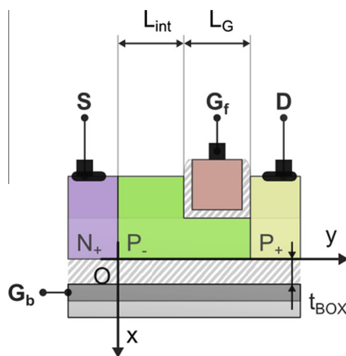

Fig. 2. N-type Z^2-FET structure (cross-section view).

3.1. Triggering mechanism of the Z^2-FET

The device is biased with positive drain voltage (V_d), positive gate voltage (V_{Gf}) and negative back-gate voltage (V_{Gb}). When the Z^2-FET is locked, the gated area is inverted and the uncovered area is accumulated, hence forming a virtual N+/P/N/P+ structure: 3 junctions are created. As opposed to a Lateral SOI-Thyristor [12,13], the central P/N junction is not made by implantation (undoped body) and there is no real Bipolar Junction Transistor in our device. The P-like region (base of the NPN in an “equivalent” thyristor) and N-like region (base of the PNP in the equivalent thyristor) of the body are created by field effect rather than by doping. Also, no avalanche takes place in the triggering of the Z^2-FET.

In this locked mode, the Z^2-FET presents an S-shaped I_d–V_d characteristic presented in Fig. 3. Simulations were achieved, at constant temperature $T = 300$ K, using the adaptive load line technique [21,22]. Standard drift-diffusion model was used without self-heating. (Indeed, we are primarily interested in the triggering mechanism of the structure which occurs at low power). Firstly, the back and front gates were biased in order to create accumulation (P) and inversion (N) regions, thus, two barriers are built up (Point A of the S shape and Fig. 3(A)), at the Cathode side and at the Anode side, respectively. Next, the drain voltage was increased, but these two barriers prevent any carriers to flow from the Cathode (electrons) or the Anode (holes). The current in the structure remained very low (Point B and Fig. 3(B)). When the triggering voltage V_{t1} (dependent of the front gate voltage V_{Gf}) is approached, the barriers start to decrease and injection of holes takes place from the Anode to the Cathode (Point C and Fig. 3(C)). After this point, the current coming from the cathode causes the forward biasing of the cathode/channel junction, increasing even more the current that reaches the channel/anode junction. The two barriers self-collapse (Fig. 3(D)). A feedback loop is formed and this sharp increase of current results in a negative differential resistance region until the holding point D in Fig. 3. Finally, the high conduction regime is reached (ON-state), as in a standard PIN diode.

3.2. Modulation of triggering voltage with V_{Gf}

In order to study the switching of the device from the locked (high impedance) mode to a low resistive path able to shunt the Electro Static Discharge to ground (diode mode), different voltages were applied on the front gate (V_{Gf}) and the back gate (V_{Gb}). The triggering voltage V_{t1} can be accurately controlled, thanks to the front gate voltage V_{Gf}. Indeed, the potential below the gate directly determines the barrier amplitude and the Anode voltage needed for the structure triggering. The variation of V_{t1} versus V_{Gf} is shown in Fig. 4.

For a constant back gate voltage V_{Gb} of −2 V, it is observed that V_{Gf} linearly sets the triggering voltage. When V_{Gf} is lower than 0.5 V, the device behaves like a forward biased diode (inversion in the gated area is not strong enough for the formation of holes injection barrier). A minimum V_{Gf} of 1.5 V is needed to ensure the turn-on just over the $V_{dd} = 1$ V of the technology. With this biasing scheme, the device is correctly locked, and the leakage current (defined for a constant voltage $V_d = V_{dd} = 1$ V) is decreased from 10^{-5} A/μm to 10^{-16} A/μm.

3.3. Impact of back-gate bias

The back-gate voltage V_{Gb} is used to build the electron injection barrier at the cathode side. To assess the impact of V_{Gb} on the electrical characteristics of the device, simulation results with variable V_{Gb} are reported in Fig. 5.

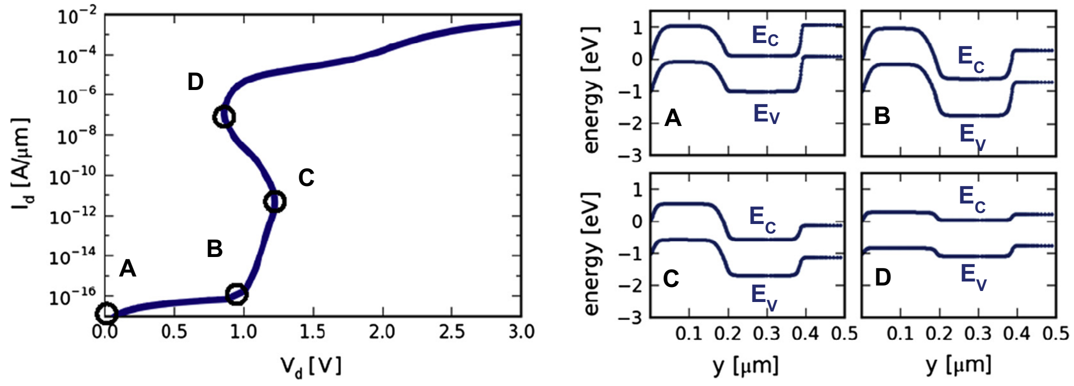

Fig. 3. (left) Simulated DC I_d–V_d characteristic of the locked Z^2-FET and (right) simulated band-diagram at mid-channel (x = 3.5 nm), from source (y = 0 µm) to drain (y = 0.4 µm). V_{Gf} = +1.5 V, V_{Gb} = −2 V, L_G = L_{int} = 200 nm, t_{BOX} = 25 nm.

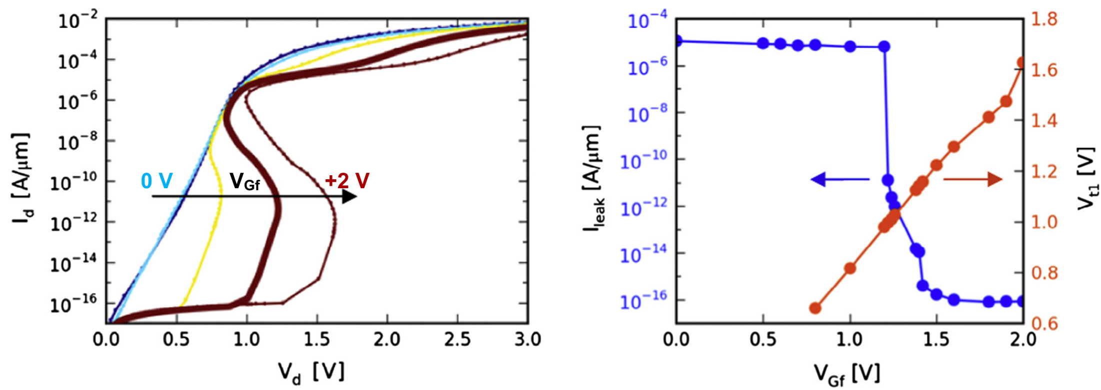

Fig. 4. (left) Simulated I_d–V_d characteristic of Z^2-FET, for V_{Gf} from 0 to 2 V and V_{Gb} = −2 V, L_G = L_{int} = 200 nm, t_{BOX} = 25 nm. (right) Evolution of triggering voltage (V_{t1}) with front-gate voltage.

A negative V_{Gb} helps to strongly accumulate holes in the L_{int} area. For a constant t_{BOX} of 25 nm, a significant decrease of the leakage current is observed (6 decades) when V_{Gb} is set to −1.5 V, as compared to V_{Gb} = 0 V. Moreover, the triggering voltage V_{t1} is maximum when −0.6 V is applied on V_{Gb}. Between 0 V and that value, the electrons injection barrier is weak and the device is not triggered at an optimum voltage. For more negative bias (V_{Gb} < −0.6 V), the inter-coupling between the back gate and the front gate occurs in the channel, at the anode side, which slightly degrades the holes injection barrier, and consequently, V_{t1}.

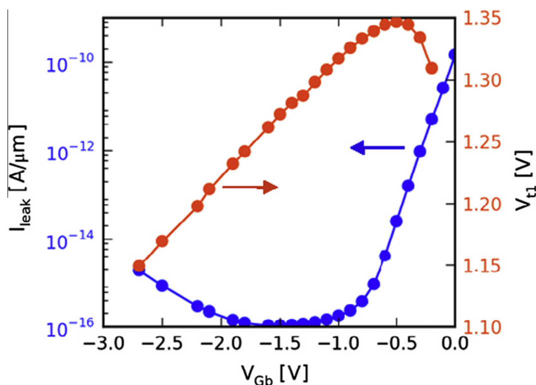

Fig. 5. Back-gate voltage (V_{Gb}) impact on the DC leakage and triggering voltage V_{t1}, for V_{Gf} = 1.5 V, L_G = L_{int} = 200 nm, t_{BOX} = 25 nm.

3.4. Impact of BOX thickness

The BOX thickness t_{BOX} impact on device performances is investigated in this section. Fig. 6 gives the I_d–V_d characteristic and the leakage current versus t_{BOX}. A dramatic reduction of the OFF-state (for V_d = 1 V and V_{Gb} = −2 V) current is noticed when the BOX is reduced from 300 nm to 25 nm (I_{leak} < 10^{-15} A/µm). Reducing the BOX allows a stronger electrostatic control of the L_{int} area which needs to be accumulated. The electrons injection barrier (from the Cathode) is strengthened up with thin BOX. This demonstrates that the behavior of this device is strongly improved in an ultra-thin-BOX technology.

3.5. Impact of film thickness

Silicon thickness under the gate changes the electrical behavior of the Z^2-FET. When the silicon film is not thin enough t_{Si} > 25 *nm*, for V_{Gb} = −2 V and V_{Gf} = +1.5 V, the lack of electrostatic control of the front and back gates on the body inhibits the formation of injections barriers. In that configuration, the OFF-state cannot be achieved below V_{dd}, and an important leakage current flows in the structure, as shown in Fig. 7. When the SOI thickness is reduced, the barriers are formed and the carriers are locked in the Anode and the Cathode. Moreover, for t_{Si} below 12 nm, V_{t1} is improved over V_{dd} = 1 V. Quantum Mechanical Correction (density gradient [22]) was activated to achieve this simulation, validating that Z^2-FET operation is not affected by quantization effects above 8 nm thickness. It was also observed a quasi-linear decrease of the triggering voltage: $\Delta V_{t1}/\Delta t_{Si} \approx -75$ mV/nm, for V_{Gf} = 1 V or V_{Gf} = 1.5 V. In fact, when t_{Si} is thinned down the front gate is more

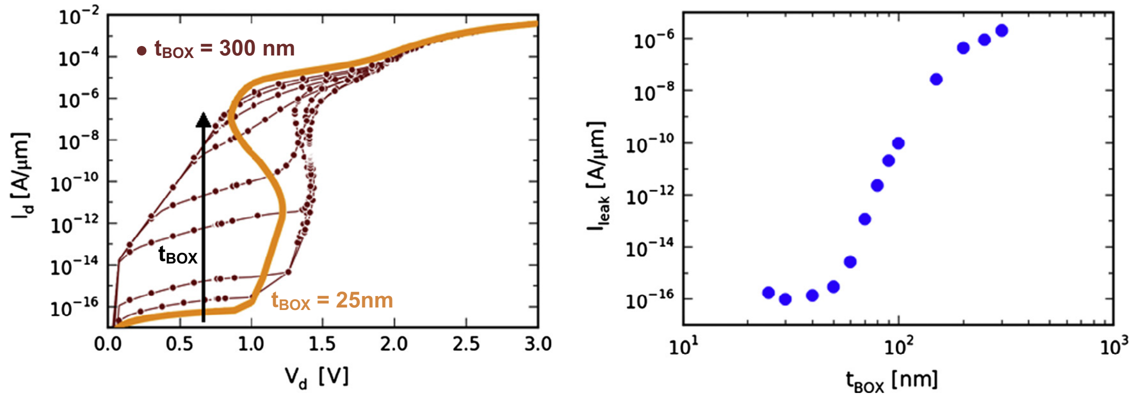

Fig. 6. (left) Simulated DC I_d–V_d characteristics with t_{BOX} changing from 300 nm to 25 nm. (right) Extracted values of I_{leak} versus t_{BOX}, V_{Gf} = +1.5 V, V_{Gb} = −2 V, L_G = L_{int} = 200 nm, t_{Si} = 7 nm.

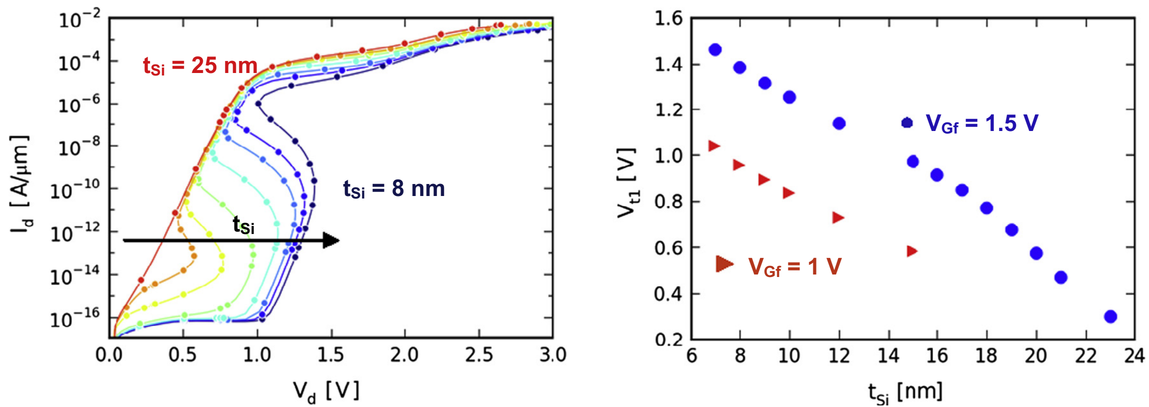

Fig. 7. (left) Simulated I_d–V_d characteristic for different silicon thickness. (right) Variation of the triggering voltage with film thickness. V_{Gb} = −2 V, V_{Gf} = 1.5 V, t_{BOX} = 25 nm.

influent on the whole body depth, explaining this gain in triggering voltage. However, if the body is too thin, V_{Gb} bias may compete with V_{Gf} (for high $|V_{Gb}|$ or thin t_{BOX}) in controlling the gated region which results in a possible reduction of the front gate barrier. Nevertheless, along with a thin BOX, a thin Body technology is advantageous for the operation of the Z^2-FET.

3.6. Impact of carrier lifetime

The feedback mechanism between the two injection barriers is greatly affected by the carrier lifetime in the channel. To evaluate this aspect, the device was simulated with the doping-dependent Scharfetter model [22]. For simplicity, we considered bulk Shockley-Read-Hall (SRH) recombination and equal lifetimes for electrons and holes. The maximum lifetime ($\tau_{MAX} = \tau_{nMAX} = \tau_{pMAX}$) was changed from τ_{MAX} = 1 ps to τ_{MAX} = 10 ns. A low lifetime, which can be caused by a high concentration of impurities and defects, increases the recombination current; this is detrimental for the leakage (I_{leak} is increased by 3 decades). On the other hand, a high τ_{MAX} increases the net number of holes reaching the cathode (less bulk recombinations), which in turn enhances the ON current as well as the feedback between the two barriers. The same mechanisms happens for the electrons driven from the cathode to the anode. Hence, the holding point in I_d–V_d curve is shifted to lower voltage and the snapback is accentuated. This trend is beneficial for the sharpness of the switch.

The interfaces tend to reduce the effective lifetime, in particular in ultrathin films. However, their contribution can be neglected when the bulk recombination lifetime is low (τ_{MAX} < 1 ns). This is noticed when surface SRH recombinations (with velocity $s_n = s_p = 10^3$ cm/s) are activated, as shown in Fig. 8.

3.7. Impact of gate underlap

Length reduction is important for several reasons: layout area efficiency and possible decrease of the ON-state series resistance. The variations of the triggering voltage and leakage current with L_{int} are shown in Fig. 9, for V_{Gb} = −2 V and t_{BOX} = 25 nm. The leakage current increases sharply when the underlap length is below L_{int} < 120 nm. For these short L_{int}, the triggering voltage V_{t1} is

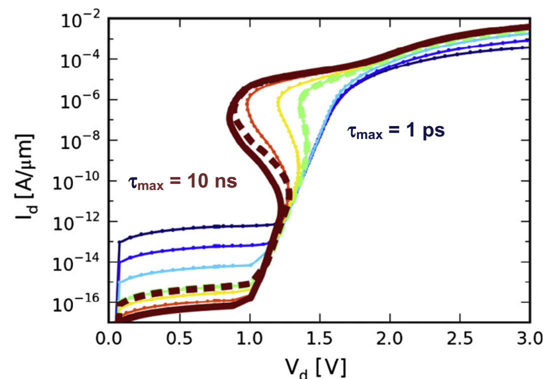

Fig. 8. Simulated I_d–V_d characteristics for variable carrier lifetime. Solid lines: only bulk SRH recombinations, Dashed lines: bulk and surface SRH recombinations. V_{Gf} = +1.5 V, V_{Gb} = −2 V, L_G = L_{int} = 200 nm, t_{Si} = 7 nm.

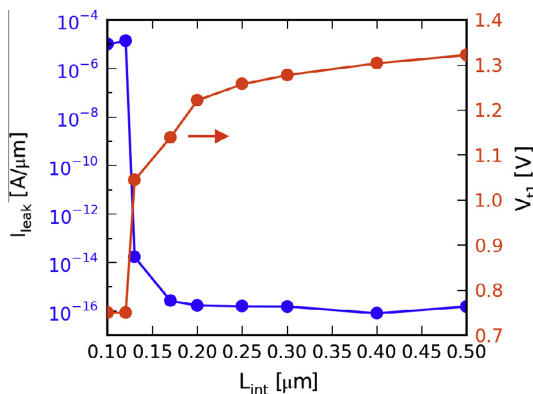

Fig. 9. Variation of leakage current (left axis) and triggering voltage (right axis) with ungated length L_{int}, for V_{Gf} = +1.5 V, V_{Gb} = −2 V, L_G = L_{int} = 200 nm, t_{si} = 7 nm.

degraded below V_d = 1 V, causing an increase of I_{leak}. Below L_{int} < 100 nm, the snapback-type I_d–V_d characteristic is quickly suppressed because the L_{int} area is no longer sufficiently controlled by the back gate and the electrons injection barrier is collapsed. When L_{int} is shrunk from 500 nm down to 200 nm, the leakage stays in a very low range, indicating that a safe downscaling of the device is possible to 200 nm, for the studied bias condition (V_{Gb} = −2 V) and BOX thickness (t_{BOX} = 25 nm). Even shorter devices are feasible if an increase of the back-gate bias or a decrease of BOX thickness can be tolerated.

3.8. Transient characteristics

The transient response is critical for ESD protection devices. Voltage overshoot must be limited to prevent damages of the load. Bulk thyristors typically present slow turn-on times (500 ps to 1 ns [23]), caused by the carrier transit time in the BJT bases. Transient simulations of the Z²-FET were achieved, with a pulse current of 1 mA/μm and an abrupt rise time of 50 ps. Results reported in Fig. 10 show that for long (L_{int} = 1 μm) devices, the response time t_r (time to reach the static voltage +10% [24]) is equal to 196 ps, and the peak overshoot voltage V_{max} is equal to 5.9 V. This value is unacceptable for the protection of low power FDSOI circuits [6].

The transient response can clearly be improved by reducing the device length, as proved in Fig. 10 with the transient characteristic obtained for L_{int} = 200 nm. In that case, the Z²-FET is turned on faster (t_r = 36 ps) and the overshoot peak voltage is reduced to V_{max} = 2.8 V. In CDM (Charged Device Model [25]) discharges rise

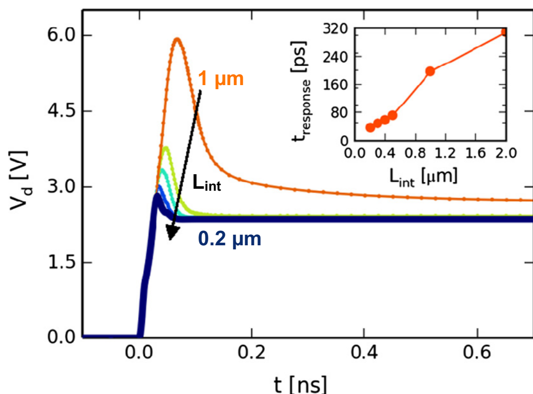

Fig. 10. Simulated transient response of the Z²-FET (I_{pulse} = 1 mA/μm, V_G = 1.5 V, V_{Gb} = −2 V) for different ungated lengths (L_{int}). Inset: variation of the response time t_r with L_{int}.

time and duration of the ESD waveform are very short (in the order of 1 ns). The fast triggering of this device, confirms that Z²-FET with relatively short length is able to evacuate CDM events.

4. Experimental study of the Z²-FET

4.1. Validation of the DC triggering voltage behavior

Z²-FET characterizations were carried out at room temperature ($T \approx 300$ K). Measured I_d–V_d characteristics are shown in Fig. 11. When V_d (the Anode voltage V_A) is swept, the device triggers sharply: for a ΔV_d < 100 mV, the current increases by 9 decades (Fig. 11a). This abrupt turn-on is observed for 1 V ⩽ V_{Gf} ⩽ 2.5 V. The leakage current remains below 10 fA/μm for V_d = V_{dd}. The triggering voltage V_{t1} was defined for a constant current of I_d = 1 pA/μm (this current value corresponds in both experimental and simulation data to the maximum I_d–V_d slope, before snapback). Our measurement confirms that V_{t1} is linearly controlled by V_{Gf} with a high coupling coefficient of $\Delta V_{t1}/\Delta V_{Gf} \approx 830$ mV/V, for all device geometries (Fig. 11b).

4.2. Impact of device length on performances

As previously discussed, scaling down the device is possible down to L_{int} = 200 nm without compromising the BOX thickness or the back gate voltage. When ESD events occur during manufacturing, the device is disconnected from any power supply. In this case, the Z²-FET is operated in the “unlocked mode”, the two gates (G_f and G_b) are biased to 0 V. Transmission Line Pulse characterization [26] of the unlocked Z²-FET, for 3 geometries, were performed by stressing the Anode with 100 ns pulses. These measurements do not cause device degradation, as shown by monitoring the DC drain current between V_d = −1 V and V_d = +1 V (in locked mode with V_{Gb} = −2 V, V_{Gf} = +1.5 V). The results were compared to gated diode characteristics, fabricated in the same SOI technology: t_{BOX} = 25 nm, t_{si} = 7 nm, thick High-K (CET = 3.7 nm) and metal gate. Typical Quasi-Static TLP I_d–V_d curves, shown in Fig. 12, indicate that in unlocked mode the high current I_d–V_d characteristic of the Z²-FET does not deviate significantly from the forward biased gated diode characteristic.

From these measurements, we extracted the ESD On-Resistance (R_{ON}) using the slope of the linear part of the I_d–V_d curve. Self-heating, which may cause a deviation from the constant-slope behavior of I_d–V_d curves, was not observed in our devices below I_d = 2 mA/μm. The results summarized in Table 1 show that the R_{ON} resistance is decreased by shrinking L_G and L_{int}. The main improvement is achieved by scaling L_G from 500 nm to 200 nm: R_{ON} is decreased from 673 Ω μm to 521 Ω μm (for L_{int} = 0.5 μm). Since the silicon film is thicker in the L_{int} part, the dominant term in R_{ON} is caused by the resistance of the gated area. Consequently, L_G optimization (as compared to L_{int}) is the best approach to reduce the Anode to Cathode voltage drop and to build a more efficient protection with the Z²-FET.

4.3. Z²-FET usability as an ESD protection: design guidelines

The main design guidelines are thereafter summarized in order to clarify the role of each parameter in the device behavior. Firstly, the BOX thickness is demonstrated to play a significant role in leakage mechanisms. The thinner the BOX, the stronger is the cathode to body barrier and the lower is the diode leakage current (at V_d = V_{dd} = 1 V): we observe $I_{leak} < 10^{-14}$ A/μm for t_{BOX} < 60 nm. Then, decreasing the silicon film thickness helps to linearly increase the triggering voltage above V_{dd} which is necessary for using this structure as a local clamp (we obtained $V_{t1} \geqslant 1.1$ V for

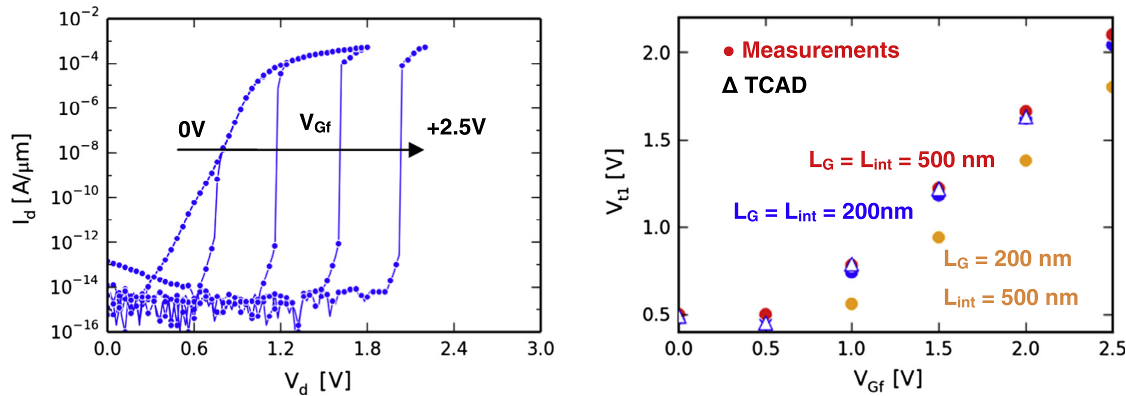

Fig. 11. (left) Experimental I_d–V_d characteristics of Z^2-FET for t_{BOX} = 25 nm, t_{Si} = 7 nm, V_{Gb} = −2 V, $L_G = L_{int}$ = 200 nm. (right) Triggering voltage (extracted at I_d = 1 pA/µm) as a function of front-gate voltage, for different device lengths. Good agreement between simulations (open triangles) and measurements (closed circles) is obtained.

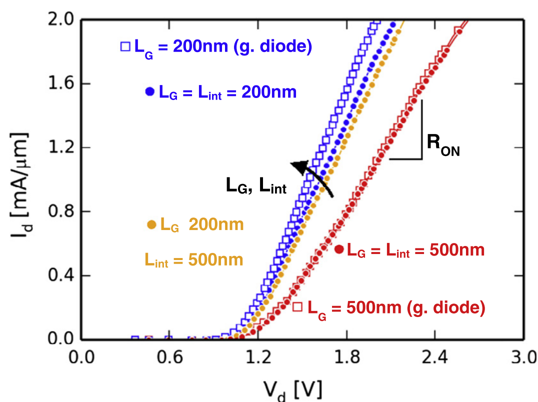

Fig. 12. TLP I_d–V_d characteristics (t_{PULSE} = 100 ns, 250 ps rise time) of the 3 designed Z^2-FETs (closed squares), compared with the gated diode curves (open circles). $V_{Gf} = V_{Gb}$ = 0 V (diode mode), t_{BOX} = 25 nm, t_{Si} = 7 nm.

Table 1
R_{ON} resistance, from TLP measurements, for the Z^2-FET and the SOI gated diode, with t_{Si} = 7 nm, t_{BOX} = 25 nm and $t_{Si} + t_{epi}$ = 22 nm.

L_G (µm)	0.2	0.2	0.2	0.5	0.5
L_{int} (µm)	0	0.2	0.5	0	0.5
R_{ON} (Ω µm)	446	499	521	657	673

t_{Si} < 10 nm). TLP characterizations show improved differential conductance in shorter gate device (L_G = 200 nm). Finally, the length of the ungated L_{int} area has to be carefully scaled in order to avoid the lowering of the electron injection barrier (at the cathode side) while keeping the turn-on time of the device as brief as possible. Response time below 100 ps can be obtained (in simulation) with leakage current below 10 fA/µm (shown in simulated and DC experimental data).

5. Conclusions

The use of the Z^2-FET as an original ESD protection device has been proposed and documented. The operation mechanisms, performance and optimization solutions of this device were studied. Numerical simulations showed the impact of length, thicknesses or biasing of the front and back gates. The triggering voltage V_{t1} can be linearly adjusted with gate voltage to comply with the design rules of protection devices. Thanks to the ultra-sharp switching characteristic, the leakage current can be controlled down to a very low value below 10 fA/µm in normal circuit operating conditions. For the first time, the astonishing properties of the Z^2-FET were experimentally validated with advanced UTBB technology. As a conclusion of our experimental results, the Z^2-FET stands as a viable candidate for ESD protections in FDSOI technologies.

Acknowledgements

Thanks are due to ST-ESD/LU team for inspiring discussions concerning ESD characterizations, to ST-TCAD team for support regarding device simulations and to Places2Be and MINOS projects for financial support. A. Zaslavsky also acknowledges support by the U.S. National Science Foundation (award ECCS-1068895).

References

[1] Griffoni A, Thijs S, Russ C, Tremouilles D, Linten D, Scholz M, et al. Electrical-based ESD characterization of ultrathin-body SOI MOSFETs. Dev Mater Reliability, IEEE Trans On 2010;10:130–41.
[2] Colinge J-P. Silicon-On-Insulator technology: materials to VLSI. 3rd ed. Springer; 2004.
[3] Benoist T, Fenouillet-Beranger C, Perreau P, Buj C, Galy P, Marin-Cudraz D, et al. ESD robustness of FDSOI gated diode for ESD network design: thin or thick BOX?. In: SOI conference (SOI), 2010 IEEE international; 2010. p. 1–2.
[4] Mergens MPJ, Russ CC, Verhaege KG, Armer J, Jozwiak PC, Mohn R, et al. Diode-triggered SCR (DTSCR) for RF-ESD protection of BiCMOS SiGe HBTs and CMOS ultra-thin gate oxides. In: Electron devices meeting. IEDM '03 technical digest. IEEE, international; 2003. p. 21.3.1–4.
[5] Di Sarro J, Vashchenko V, Rosenbaum E, Hopper P. A dual-base triggered SCR with very low leakage current and adjustable trigger voltage. In: Electrical overstress/electrostatic discharge symposium. EOS/ESD 2008; 30th, 2008. p. 242–8.
[6] Benoist T, Fenouillet-Beranger C, Perreau P, Buj C, Galy P, Marin-Cudraz D, et al. Experimental investigation of ESD design window for Fully Depleted SOI N-MOSFETs. Microelectron Eng 2011;88:1276–9.
[7] Fenouillet-Beranger C, Perreau P, Boulenc P, Tosti L, Barnola S, Andrieu F, et al. Parasitic bipolar impact in 32 nm undoped channel Ultra-Thin BOX (UTBOX) and biased Ground Plane FDSOI high-k/metal gate technology. Solid-State Electron 2012;74:32–7.
[8] Amerasekera A, Duvvury C. ESD in silicon integrated circuits. 2nd ed. Wiley; 2002.
[9] Dray A, Guitard N, Fonteneau P, Golanski D, Fenouillet-Beranger C, Beckrich H, et al. ESD design challenges in 28 nm hybrid FDSOI/Bulk advanced CMOS process. In: Electrical overstress/electrostatic discharge symposium (EOS/ESD); 34th, 2012. p. 1–7.
[10] Wan J, Le Royer C, Zaslavsky A, Cristoloveanu S. A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration. Electron Dev Lett, IEEE 2012;33:179–81.
[11] Wan J, Cristoloveanu S, Le Royer C, Zaslavsky A. A feedback Silicon-On-Insulator steep switching device with gate-controlled carrier injection. Solid-State Electron 2012;76:109–11.
[12] Entringer C, Flatresse P, Galy P, Azais F, Nouet P. Partially depleted SOI body-contacted MOSFET-triggered silicon controlled rectifier for ESD protection. In: Electrical overstress/electrostatic discharge symposium. EOS/ESD '06; 2006. p. 166–71.

[13] Mergens MPJ, Marichal O, Thijs S, Van Camp B, Russ CC. Advanced SCR ESD protection circuits for CMOS/SOI nanotechnologies. In: Custom integrated circuits conference. Proceedings of the IEEE; 2005. p. 481–8.
[14] Raissii F. A brief analysis of the Field Effect Diode and breakdown transistor. Electron Dev, IEEE Trans On 1996;43:362–5.
[15] Cao S, Chun J-H, Salman AA, Beebe SG, Dutton RW. Gate-controlled field-effect diodes and silicon-controlled rectifier for charged-device model ESD protection in advanced SOI technology. Microelectron Reliab 2011;51:756–64.
[16] Salman AA, Beebe SG, Emam M, Pelella MM, Ioannou DE. Field Effect Diode (FED): a novel device for ESD protection in deep sub-micron SOI technologies. In: Electron devices meeting. IEDM '06. International; 2006. p. 1–4.
[17] Yang Y, Gangopadhyay A, Li Q, Ioannou DE. Scaling of the SOI Field Effect Diode (FED) for memory application. In: Semiconductor device research symposium. ISDRS '09. International; 2009. p. 1–2.
[18] Fenouillet-Beranger C, Perreau P, Tosti L, Thomas O, Noel J, Weber O, et al. Low power UTBOX and back plane (BP) FDSOI technology for 32 nm node and below. In: IC design technology (ICICDT), 2011 IEEE international conference on; 2011. p. 1–4.
[19] Planes N, Weber O, Barral V, Haendler S, Noblet D, Croain D, et al. Symposium on VLSI technology (VLSIT). IEEE 2012;2012:133–4.
[20] Fenouillet-Beranger C, Denorme S, Perreau P, Buj C, Faynot O, Andrieu F, et al. FDSOI devices with thin BOX and Ground Plane integration for 32 nm node and below. Solid-State Electron 2009;53:730–4.
[21] Goossens RJG, Beebe S, Yu Z, Dutton RW. An automatic biasing scheme for tracing arbitrarily shaped *I–V* curves. Comput – Aided Des Integrated Circ Syst, IEEE Trans On 1994;13:310–7.
[22] Synopsys. Sentaurus device user guide version C-2009.06; 2009.
[23] Di Sarro J, Chatty K, Gauthier R, Rosenbaum E. Study of design factors affecting turn-on time of Silicon Controlled Rectifiers (SCRS) in 90 and 65 nm bulk CMOS technologies. In: Reliability physics symposium proceedings. 44th Annual, IEEE international; 2006. p. 163–8.
[24] Manouvrier JR, Fonteneau P, Legrand CA, Nouet P, Azaïs F. Characterization of the transient behavior of gated/STI diodes and their associated BJT in the CDM time domain. Microelectron Reliab 2009;49:1424–32.
[25] Semenov O, Sarbishaei H, Sachdev M. ESD protection device and circuit design for advanced CMOS technologies. 1st ed. Incorporated: Springer Publishing Company; 2008.
[26] Barth JE, Verhaege K, Henry LG, Richner J. TLP calibration, correlation, standards, and new techniques, electronics packaging manufacturing. IEEE Trans On 2001;24:99–108.