Electron-Hole Bilayer TFET: Experiments and Comments

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***Abstract*— We investigate $Si/Si_{0.85}Ge_{0.15}$ fully depleted-SOI tunnel FET (TFET) devices operated in the electron-hole bilayer (EHB) mode. The application of negative bias on front gate and positive bias on back gate results in confined hole and electron layers that are expected to enable vertical band-to-band tunneling (BTBT). The idea of the EHB-TFET device is to enhance the tunneling current by expanding the BTBT generation area from the narrow lateral source/channel junction to the entire channel region. Our systematic measurements on a variety of TFETs with variable geometry and channel materials do not offer support to this attractive concept. Self-consistent simulations confirm that the vertical BTBT transitions do not produce an appreciable current in our devices, due to size- and bias-induced quantization, effective mass anisotropy, and incomplete formation of the bilayer. We examine the conditions for efficient vertical BTBT to occur and show that they cannot be met simultaneously, at least in Si or Si/SiGe devices.**

***Index Terms*— Characterization, electron hole bilayer TFET, quantum confinement, SOI, sub-band alignment, sub-band splitting, supercoupling, tunnel-FET.**

I. INTRODUCTION

DUE to their low-subthreshold swing (SS), tunnel FETs (TFETs) have attracted considerable interest for operation at low V_{DD} [1]–[4]. Numerous results have been reported showing progress in technology, but to date no TFET has achieved both sub-60 mV/decade SS (at 300 K) and high-I_{ON} current.

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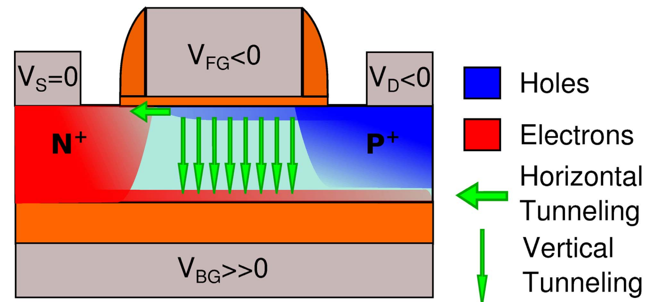

Fig. 1. Sketch of the TFET biased with opposite potentials at the front gate and at the back gate (substrate) to form electron and hole layers. The arrows indicate the horizontal and the expected vertical BTBT transitions.

One reason for the low-I_{ON} current is the geometrical distribution of the band-to-band tunneling (BTBT) that is concentrated in a very narrow region near the source/channel tunnel junction. This is why the BTBT current is not improved by the scaling of the channel length, as in a MOSFET.

Novel device geometries have been considered to overcome this limitation [5], [6], boosting the I_{ON}. In particular, Lattanzio *et al.* [7] have proposed a new device structure replacing the small horizontal tunneling region at the source/channel junction with a vertical tunneling region that covers the whole transistor body. The alignment of tunneling direction and vertical electric field is achieved by back-gate biasing.

In a double-gate (DG) TFET, the front and back gates are biased with opposite polarities such as to induce an electron-hole bilayer in the channel area under the front gate, effectively extending the physical N^+ and P^+ source and drain terminals into the channel (Fig. 1). In the resulting EHB-TFET, BTBT occurs vertically between the virtual bias-induced terminals. The clear advantage is that the tunneling surface becomes as large as the front gate area.

A series of articles reported the concept and predicted performance of Si and Ge EHB-TFETs obtained from extensive semiclassical simulations [7]–[9]. A later paper [10], based on a more refined Schrödinger–Poisson simulator coupled with a full quantum BTBT model, concluded that earlier expectations for I_{ON} were overestimated by 2–3 orders of magnitude. On the other hand, Teherani *et al.* [11] examined the details of band alignment and raised fundamental questions about the practicality of the EHB-TFET. They argued that,

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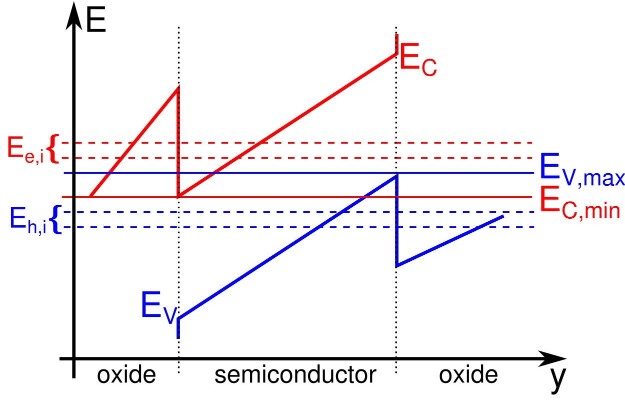

Fig. 2. Splitting of the conduction and valence band in sub-bands in a DG structure with an opposite biasing of the front and the back gates. While the edges of conduction and valence bands are favorably aligned ($E_{V,\max} > E_{C,\min}$) the lowest valence sub-band $E_{h,0}$ still lays below the lowest conduction sub-band $E_{e,0}$, hence BTBT cannot take place.

due to size- and bias-induced quantization, prohibitively high-gate voltages would be required, causing oxide reliability concerns.

For BTBT to occur in TFETs several conditions need to be fulfilled:

1) simultaneous formation of the proper band alignment and of the electron and hole layers in the channel;
2) strong vertical electric field leading to short tunneling distance;
3) significant overlap of the electron and hole wave-functions in the vertical direction.

Condition 2) implies ultrathin film, which in turn affects requirements 1) and 3). Semiclassical models, based on WKB approach [12], indicate that the BTBT generation rate increases exponentially in thinner films. However, in a strong vertical field, size- and field-induced quantization leads to the splitting of the valence and conduction bands into well-resolved sub-bands at energies above the band extrema $E_{C,\min}$ and $E_{V,\max}$, making band alignment more difficult to achieve, as shown schematically in Fig. 2. Furthermore, the lowest sub-band energies $E_{e,0}$ and $E_{h,0}$ are determined by the heaviest effective masses in the vertical direction, but this impedes 3). A direct consequence is that semiclassical models are not fully reliable for modeling EHB-TFETs and more advanced approaches are requested, such as those reported in [13] and [14].

Band alignment can eventually be achieved by increasing the vertical field (i.e., the voltage drop V_B across the body). The efficiency of this method is modest, because the bias-induced quantization further separates the $E_{e,0}$ and $E_{h,0}$ sub-bands. In addition, a change in body voltage ΔV_B requires a much higher difference $\Delta V_{G,\text{fb}}$ between the front and back gate voltages. Below 10-nm thickness, the efficiency rate $\Delta V_B/\Delta V_{G,\text{fb}}$ drops severely, which means that higher gate voltages are needed [11]. This is not an option for several reasons: 1) it negates the main advantage of TFETs, which is low-supply voltage operation; 2) it increases significantly the gate tunneling current, which jeopardizes the SS and I_{OFF}; and 3) it may even cause oxide breakdown.

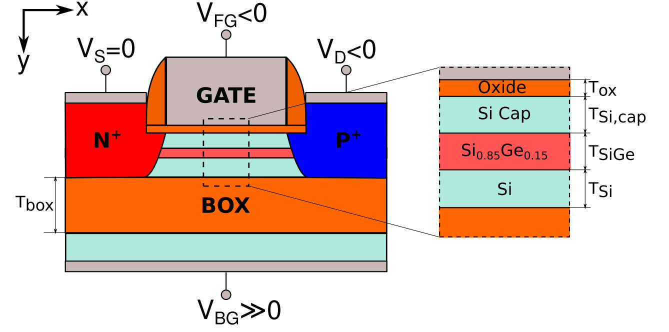

Fig. 3. Sketch of the TFET structures tested in this paper.

TABLE I
THICKNESS OF THE MATERIAL LAYERS FOR THE THREE CONSIDERED TFET DESIGNS

	EOT	T_{box}	T_{Si}	T_{SiGe}	$T_{Si,cap}$
Design 1	≈1.2nm	145nm	≈6.3nm	0nm	0nm
Design 2	≈1.2nm	145nm	≈3.5nm	≈1.7nm	≈1.5nm
Design 3	≈1.2nm	145nm	≈3.5nm	≈9.6nm	≈1.5nm

TABLE II
GEOMETRIC DIMENSIONS OF THE TESTED DEVICES FOR ALL THE THREE DESIGNS

	L [μm]	W [μm]	Fingers	Ch. Area [μm^2]
Device 1	1	10	10	100
Device 2	0.5	10	20	100
Device 3	0.2	10	50	100
Device 4	0.1	10	10	10
Device 5	0.2	10	1	2
Device 6	0.15	10	1	1.5

Furthermore, the formation of the electron and hole bilayers in ultrathin films faces the supercoupling effect [15]. Below a critical thickness, it is impossible to induce accumulation and inversion layers facing each other. One of the gates dominates and either electrons or holes fill the body, leading to volume inversion or volume accumulation. Supercoupling is a general size effect governed by the film thickness. Changing the materials, gate bias or buried oxide thickness only modifies the critical thickness by a few nanometer.

On the experimental side, given the significant research effort devoted to TFETs in recent years, it is troubling that no experimental confirmation for EHB-TFET operation has been reported to date. The aim of this paper is to fill the experimental gap by measuring the vertical tunneling in several types of Si/SiGe fully-depleted SOI (FD-SOI) TFET devices. The experimental conditions are given in Section II and the measurements are reported in Section III, with no effective vertical BTBT current observed for any combination of front and back gate biasing. In view of the results obtained, we performed self-consistent quantum simulations to revisit the conditions needed for EHB-TFET operation. These results are discussed in Section IV.

II. Tested Devices and Measurement Setup

Measurements have been carried out on three recent runs of FD-SOI TFETs, fabricated at LETI-CEA, which showed some of the best TFET performance reported to date.

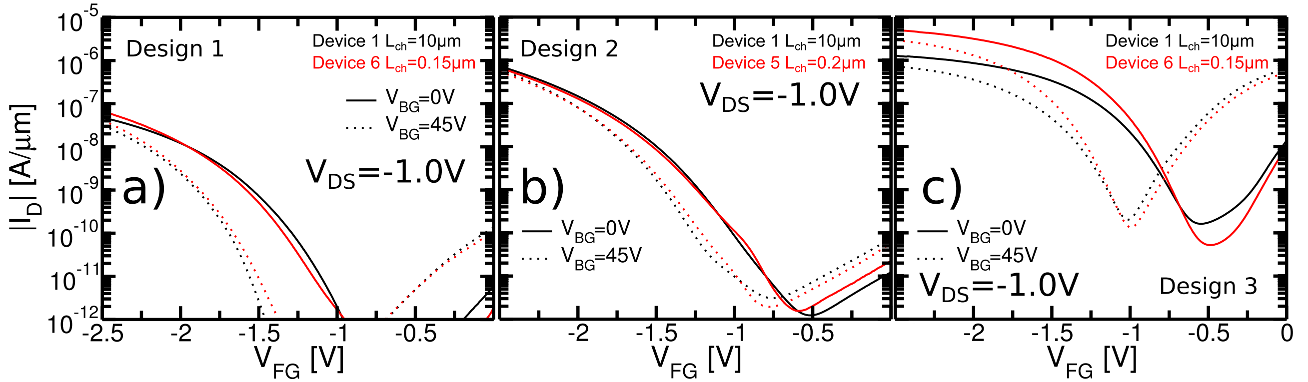

Fig. 4. Trans-characteristics of small area (A_{ch} = 1.5 μm^2) and large area (A_{ch} = 100 μm^2) TFETs for all the three designs with back-gate biasing (V_{BG} = 45 V) and without back-gate biasing and without back-biasing for the TFETs of Design 1 (plot a), Design 2 (plot b) and Design 3 (plot c).

The first variant (Design 1) has an ultrathin channel entirely composed of silicon with a thickness $T_{Si} = 6.34$ nm.

Designs 2 and 3 feature three-layer composite channels, as shown in Fig. 3: 1) a lower Si layer of thickness $T_{Si} = 3.5$ nm; 2) a central compressively strained $Si_{0.85}Ge_{0.15}$ layer of thickness T_{SiGe}; and 3) an upper Si cap of $T_{Si,cap} = 1.5$ nm. The buffer Si serves for epitaxial growth of strained SiGe, whereas the Si cap achieves improved interface quality with the gate oxide. Designs 2 and 3 differ in the T_{SiGe} layer thickness, 1.7 and 9.6 nm, respectively.

For all designs, the gate dielectric is HfO_2 with an EOT $\approx$ 1.2 nm and the SiO_2 buried oxide is 145-nm thick. The thicknesses of the various layers are reported in Table I. Devices made from the three designs all had the same range of geometric dimensions W (gate width), L (gate length), and numbers of fingers, as reported in Table II. We have chosen these FD-SOI devices because of their record I_{ON} performance in TFET mode, reported in [16], and of their structure that permits to create an electron inversion channel at the back interface using a large V_{BG}, allowing us to study them in a EHB-TFET working mode.

The first design is representative of a state-of-the-art Si FD-SOI technology. The introduction of the SiGe in Designs 2 and 3 results in enhanced BTBT given its reduced bandgap and the highest I_{ON} ever obtained for a Si/SiGe heterojunction TFET.

The measurements have been performed using the semiconductor parametric analyzer HP4155A with a Karl Suss probe station. The devices have been biased in p-mode configuration, the N^+ region is considered as the TFET source (grounded), while the P^+ terminal is the drain biased with $V_D < 0$. The front gate bias is negative $V_{FG} \leq 0$ V. For the electrical field in the channel to have the dominant component in the vertical direction, needed for EHB-TFETs, a positive back-bias V_{BG} has been applied to the substrate.

III. Experimental Results

Representative trans-characteristics for the three families of TFETs are shown in Fig. 4. Our goal is to identify the origin of the tunneling current. The sketch in Fig. 1 qualitatively illustrates the two possible BTBT mechanisms. Horizontal BTBT takes place from the source terminal to the channel region, whereas vertical BTBT occurs between the virtual accumulation and inversion layers of the EHB-TFET. Only the vertical BTBT requires back-gate biasing.

We first discuss the case of grounded substrate ($V_{BG} = 0$ V) for horizontal tunneling, which is the conventional mechanism in planar TFETs. The $I_D(V_{FG})$ curves in Fig. 4 are normally behaved. On the technology side, they confirm the advantage of SiGe channel for boosting the I_{ON} and of ultrathin channel for reducing the OFF-current. No significant impact of gate length is observed, except in Design 3 where the shorter TFET performs better, as explained by the potential drop in the lateral MOSFET channel at high current [17].

When a high-positive $V_{BG} = 45.0$ V bias is applied to the back gate, we simply note a lateral shift of the characteristics to the left. This effect is well known in FD-SOI MOSFETs as interface coupling [18], a positive V_{BG} increases the threshold voltage of the hole channel at the front interface V_{FT} by $\Delta V_{FT}/\Delta V_{BG} \simeq \mathrm{EOT}/T_{box}$. In our case ($\mathrm{EOT}/T_{box} \simeq 0.08$), the calculated shift is 350 mV, in good agreement with Fig. 4.

Another argument against vertical BTBT is given by the comparison of devices with very different channel (gate) area A_{ch}. Fig. 4 shows characteristics for TFETs with A_{ch} changed by two orders of magnitude. Since the vertical BTBT scales with the channel area, the current in Device 1 (with $A_{ch} = 100\ \mu m^2$) should be significantly higher than the one of Devices 5 or 6 ($A_{ch} = 1.5\ \mu m^2$). For fair comparison of the different devices, we have considered a unique criterion of leakage current, $I_{OFF} = 6$ nA/μm, and measured the corresponding gate voltage $V_{FG} = V_{FG,OFF}$. We defined the ON-current I_{ON} for 1 V voltage swing at $V_{FG,ON} = V_{FG,OFF} - 1$ V. Fig. 5 shows the normalized I_{ON} current (accounting for gate width and number of fingers) measured for all designs, with and without positive back-gate biasing, as a function of gate area. In presence of a noticeable vertical BTBT current at $V_{BG} = 45$ V, the I_{ON} should have increased linearly with the channel area. However, the curves in Fig. 5 are quite flat. These results suggest that vertical EHB current is completely absent or negligible with respect to the horizontal BTBT current between the source and the channel.

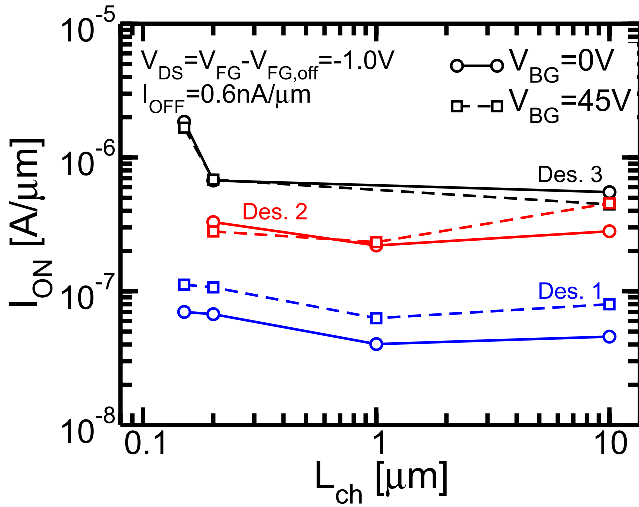

Fig. 5. I_{ON} current (per unit width) defined as $I_D(V_{FG} = V_{FG,OFF} - 1$ V), where $V_{FG,OFF}$ is the V_{FG} voltage at which $I_D = I_{OFF} = 6$ nA/μm. Measurements with back-bias (dashed line) and without back-bias application (solid line) are compared.

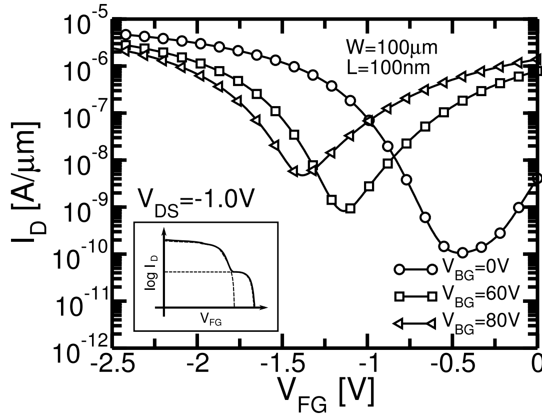

Fig. 6. Trans-characteristics of Design 3 TFET measured at very high back-gate bias. For $V_{BG} = 80$ V the ON-current is smaller than for $V_{BG} = 0$ V showing the absence of vertical tunneling. Inset: schematically the kink in I–V curves expected from the transition from lateral to vertical tunneling.

To maximize the possibility of observing vertical BTBT, we measured Design 3 TFETs at an even higher V_{BG}, up to 80 V. Fig. 6 shows the resulting transfer curves. Again, increasing V_{BG} even far beyond the threshold of forming an electron layer at the back interface does not lead to a higher I_{ON}. Furthermore, the $V_{BG} = 80$ V curve is smooth, whereas the combination of lateral and vertical BTBT would presumably lead to a kink in subthreshold characteristics, as schematically shown in the inset of Fig. 6 since the two tunneling mechanisms have different parameters. In addition, quantization has different effect on the horizontal tunneling component with respect to the vertical one [10], [13], [19]. Due to effective mass quantization and strain, the valence band is split into multiple sub-bands and in presence of a strong contribution of the vertical BTBT this should lead to the possible appearance of multiple kinks in the I_D–V_{FG}, reflecting the sequential alignment of the conduction and valence sub-bands as V_{FG} increases [20]. The smooth I_D–V_{FG}, even for $V_{BG} = 80$ V, indicates that the current is dominated by the horizontal BTBT near the source/channel junction.

IV. Simulation Results

A self-consistent 1-D Schrödinger–Poisson simulator has been used to simulate the sub-band splitting in the vertical quantization direction of the multilayer stack. The computation of the Schrödinger problem requires specifying the effective mass of electrons and holes, the bandgap and the affinity of the materials. The vertical profiles of electrons and holes have been computed self-consistently with the wave-functions and the Fermi-Dirac statistics for 2-D quantized gases [20]. These simulations give insight on the fulfillment or violation of the conditions for vertical BTBT. In this regard, a 1-D approach is sufficient, since the electric field in the device is maximum in the vertical direction and almost constant over the entire channel area. In addition, since the EHB-TFET requires large channel area, and therefore large L_{ch} and W_{ch}, the quantization and corner effects in the plane normal to the tunneling direction can be neglected.

A. Alignment of the Valence and Conduction Sub-Bands

The simulations for Designs 1 and 2 structures, given their thin-channel thicknesses, show no possible alignment of the lowest conduction and valence sub-bands even when biasing the front and back gates with very high, unrealistic voltages ($V_{BG} = 100$ V). An example is given in Fig. 7 where only the band profiles (best case) are reported. Even ignoring quantization effects there is no chance of EHB tunneling in Design 1 [Fig. 7(e)] or Design 2 (similar curves, not shown), since E_C at the back interface lies above E_V at the front interface. On the other hand, considering the lowest electron and hole sub-band for Design 3 for $V_{BG} \leq 60$ V [Fig. 9(a)] there is no intersection between the hole and the electron sub-bands for any potential V_{FG} between 0 and -2.5 V. If $V_{BG} > 60$ V a favorable alignment of the sub-bands can take place at $|V_{FG}| < 2.5$ V, as discussed later. Regarding the bias conditions, it has been shown that the front-gate voltage can be reduced by tuning of the work-function [7]. The back-gate bias is of serious concern: 1) even with very thin 25-nm BOX; 2) V_{BG} will be in the 10 V range; and 3) too high for practical applications. The TFETs with FinFET structure and independent lateral gates may be a solution that requires experimental confirmation.

B. Existence of Electron-Hole Bilayer Reservoirs

The right panels in Fig. 7 show the carrier profiles computed with the Schrödinger–Poisson simulator along the quantization direction, at mid-distance between source and drain. The biasing potentials are $V_{DS} = -1$ V, $V_{FG} = -2.5$ V (strong accumulation of holes) and $V_{BG} = 50$ and 80 V. In Design 3*, which is identical to Design 3 but with thicker $T_{sc} = 30$ nm [Fig. 7(b)], there is clear formation of opposite layers of electrons and holes with very high concentrations ($\geq 10^{19}$ cm^{-3}). For the experimental thickness of 15 nm in

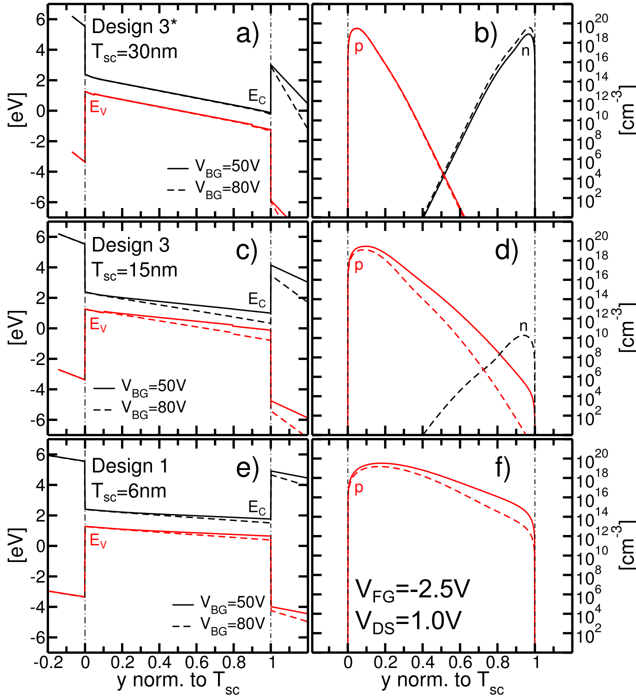

Fig. 7. Left: (a), (c), and (e) vertical profiles of the conduction E_C and valence band E_V along the quantization direction at the midpoint between source and drain. Right: (b), (d), and (f) corresponding concentrations of holes p and electrons n versus normalized distance across the film. First row considers a variant of Design 3, (denoted Design 3*) with thicker semiconductor stack ($T_{\mathrm{sc}} = 30$ nm). Second row corresponds to Design 3 with $T_{\mathrm{sc}} = 15$ nm. The last row corresponds to Design 1 and encompasses the case of Design 2.

Design 3 [Fig. 7(d)], the peak electron concentration barely reaches the intrinsic concentration in Si (10^{10} cm^{-3}). Even more dramatic is the case of ultrathin Designs 1 and 2 [Fig. 7(f)], where the electrons vanish from the body and the holes spread along the whole channel thickness. These simulations confirm the so called super-coupling effect, first discussed in [15]. For given gate biases, there is a critical film thickness below which electrons and holes cannot be accommodated together. The stronger gate bias imposes the body to host either electrons or holes. The bilayer simply transforms into a monolayer excluding any vertical EHB tunneling.

C. Vertical Electric Field

Fig. 8 shows the variation of the average value of the vertical field F_{av} with increasing back-gate bias, for $V_{\mathrm{DS}} = -1$ V and $V_{\mathrm{FG}} = -2.5$ V. In a thick film ($T_{\mathrm{sc}} = 30$ nm, diamond symbols), the average field saturates as soon as the electron layer is formed at the back interface ($V_{\mathrm{BG}} > 40$ V). There is no field saturation in the thinner structure ($T_{\mathrm{sc}} = 15$ nm, square symbols) because the super-coupling effect prevents the formation of the electron layer. The linear increase of the field with V_{BG} reflects a stronger bias-induced quantization and therefore a more pronounced sub-band splitting [11]. For $V_{\mathrm{BG}} = 80$ V, the average field reaches $F_{\mathrm{av}} = 1.35$ MV/cm, which is of concern for device reliability.

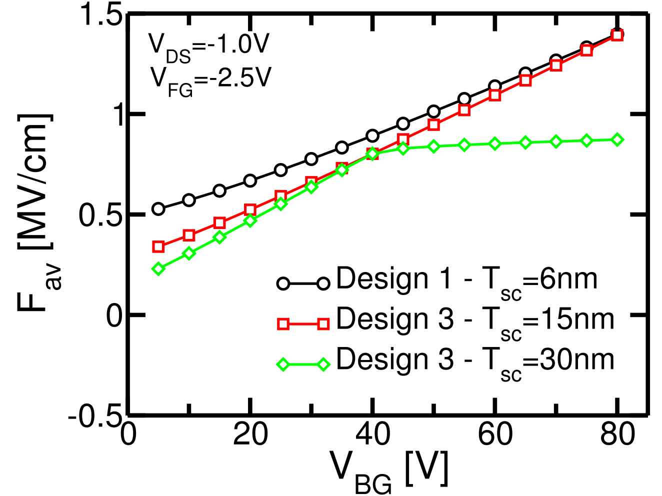

Fig. 8. Average electric field along the quantization direction at mid-distance between source and drain for TFETs with Designs 1 and 3 (with $T_{\mathrm{sc}} = 15$ and 30 nm).

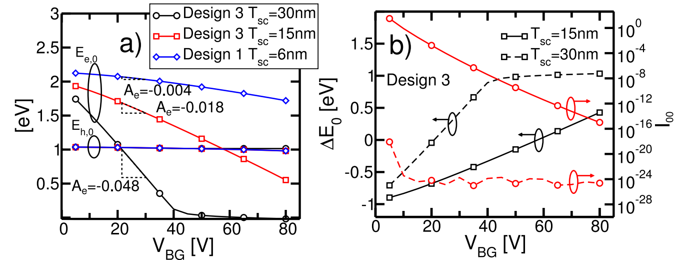

Fig. 9. Influence of back-gate voltage on (a) energy levels of the highest valence sub-band $E_{h,0}$ and the lowest conduction $E_{e,0}$ sub-band and (b) energy difference $\Delta E_0 = E_{h,0} - E_{e,0}$ (square symbols) and overlap integral I_{00} (circle symbols). Various TFET designs, $V_{\mathrm{DS}} = -1.0$ V and $V_{\mathrm{FG}} = -2.5$ V.

D. BTBT, Wave-Function Overlap, and Effective Mass Anisotropy

Effective BTBT requires strong overlap of the electron-hole wave-functions, in other words a short tunneling distance. According to Vandenberghe *et al.* [13], in indirect bandgap semiconductors, the probability for transition between the lth valence sub-band and the kth conduction sub-band T_{lk} is proportional to the wave-function overlap I_{lk} as follows:

$$T_{lk} \propto \begin{cases} I_{lk} & \text{if } E_{h,l} > E_{e,k} \\ 0 & \text{otherwise} \end{cases} \tag{1}$$

with

$$I_{lk} = \int_0^{T_{\mathrm{Si}}} dy |\Psi_{h,l}(y)|^2 |\Psi_{e,k}(y)|^2 \tag{2}$$

where $\Psi_{h,l}$ and $\Psi_{e,k}$ are the normalized wave-functions of the lth valence and of the kth conduction sub-bands, respectively, and $E_{h,l}$ and $E_{e,k}$ are the corresponding sub-band energies (neglecting the phonon energies in phonon-assisted BTBT).

To estimate the probability for vertical BTBT, we focus on the transition between the lowest valence $E_{h,0}$ and conduction $E_{e,0}$ sub-bands. Fig. 9(a) shows the energy levels for same TFET structures as in Fig. 8. The value for $E_{h,0}$ is fully governed by the strong accumulation condition at the front interface ($V_{\mathrm{FG}} = -2.5$ V) and is practically insensitive to

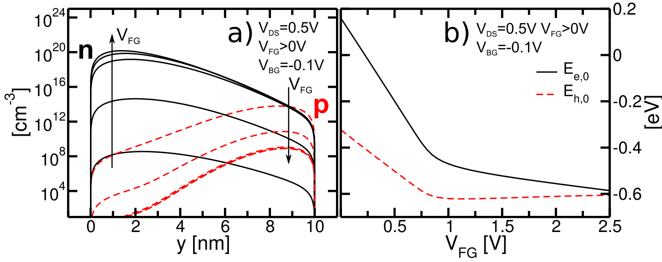

Fig. 10. (a) In-depth profiles of electrons (full lines) and holes (dashed) at the midpoint between source and drain for the symmetrical Ge TFET present in [8] biased in n-type configuration. (b) Dependence of the lowest electron and hole sub-band energies. $V_{\mathrm{DS}} = 0.54$ V, $V_{\mathrm{BG}} = -0.1$ V, EOT = 0.46 nm, $E_{\mathrm{wf,FG}} = 3.8$ eV, and $E_{\mathrm{wf,BG}} = 4.64$ eV.

back-gate bias and film thickness. The decrease in electron sub-band energy with V_{BG} reflects the buildup of the electron charge [20]. For $T_{\mathrm{sc}} = 30$ nm, the inversion layer forms rapidly at the back interface and $E_{e,0}(V_{\mathrm{BG}})$ variation has a steep slope $A_e = dE_{e,0}/dV_{\mathrm{BG}} = 0.048$ eV/V. This variation stops when the back electron channel reaches strong inversion ($V_{\mathrm{BG}} = 40$). In thinner films, the buildup of the electron layer is slowed down by supercoupling [see also Fig. 7(d) and (f)], reducing the rate at which the conduction sub-bands drop with V_{BG} ($A_e = 0.018$ for $T_{\mathrm{sc}} = 15$ nm and $A_e = 0.004$ for $T_{\mathrm{sc}} = 6$ nm). Note that slope A_e has a similar meaning as the efficiency rate $\Delta V_B/\Delta V_{G,\mathrm{fb}}$ defined in [11]. It follows that the presence of the bilayer is a necessary condition for vertical BTBT because it is the strong electron inversion and hole accumulation that allows the conduction and valence sub-bands to reach alignment.

Fig. 9 shows the impact of the back-gate bias on the energy difference $\Delta E_0 = E_{h,0} - E_{e,0}$ (square symbols) and on the overlap integral I_{00} (circle symbols) for TFETs with Design 3 and 3* (best case). The transition between these two sub-bands is possible when $\Delta E_0 \geq 0$. (For large ΔE_0, other transitions between additional valence and conduction sub-bands with higher energy become also possible.) In the thicker Design 3* device ($T_{\mathrm{sc}} = 30$ nm, dashed lines), favorable band alignment ($\Delta E_0 \geq 0$) is easily secured for $V_{\mathrm{BG}} \geq 20$ V and due to the saturation of the accumulation layer at the back-gate ($V_{\mathrm{BG}} > 40$ V) the value of $E_{h,0}$ cannot descend further. Unfortunately, the transition probability is negligible because of the insufficient overlap integral value I_{00} between the two wave-functions. This probability is higher by many orders of magnitude in the thinner TFET ($T_{\mathrm{sc}} = 15$ nm, plain lines) at low-carrier confinement, and decreases exponentially with the vertical field and V_{BG}. Since the band alignment is achieved at much higher voltage ($V_{\mathrm{BG}} \geq 60$ V), the overlap integral I_{00}, and therefore, the transition probability becomes modest again. Additional simulations demonstrate very high-overlap integral in ultrathin films (sub-10-nm thick as in Designs 1 and 2), but without the necessary band alignment for effective BTBT.

To rule out the possibility that it is the thick buried oxide that is responsible for the insufficient electron inversion layer at the back interface, we have simulated the exact Ge-channel structure proposed in [8] at the midpoint between the source and drain. Fig. 10(a) shows the electron and hole densities in the vertical direction as a function of V_{FG} in the n-type configuration proposed in [8]. It has the same EOT = 0.46 nm for both front and back gate oxides, but we observe that as we increase $V_{\mathrm{FG}} > 0$ V and, therefore, the electron inversion layer density is enhanced, at the same time the hole accumulation layer is reduced. This confirms that the super-coupling effect occurs in any ultrathin semiconductor channel, where one of the gates comes to dominate the other [15]. Additional confirmation is shown in Fig. 10(b), where we plot the lowest electron and hole sub-band energies as a function of increasing V_{FG}. For $V_{\mathrm{FG}} < 1$ V both sub-band energies decrease, whereas for $V_{\mathrm{FG}} > 1$ V the electron layer saturates and the sub-bands begin to approach each other, but even at $V_{\mathrm{FG}} = 2.5$ V a favorable BTBT sub-band alignment is not achieved. Similar simulations for Si-channel TFET with symmetrical gate oxides reveal far more unfavorable conditions than for Ge-channel.

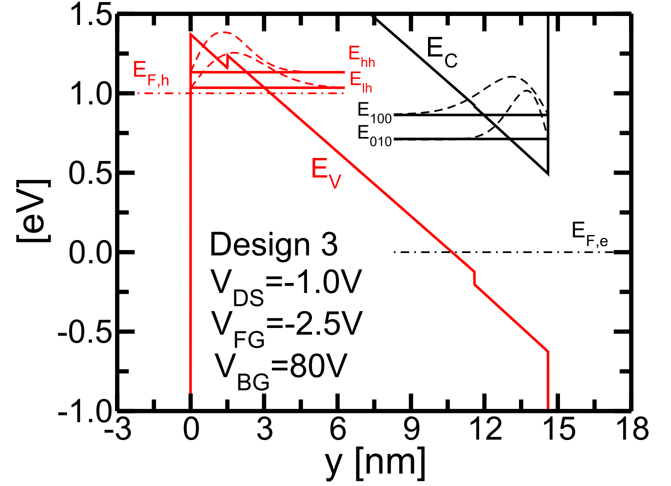

Fig. 11. Profile of the valence and conduction band with $V_{\mathrm{DS}} = -1.0$ V, $V_{\mathrm{FG}} = -2.54$ V, and $V_{\mathrm{BG}} = 80$ V. The lowest sub-bands are computed for the light- and heavy-hole valence band valleys and for the Δ_{100} and Δ_{010} conduction band valleys. The corresponding wave-functions are also shown (dashed lines). For the wave-function the vertical scale is arbitrary, but the horizontal scale is the same of the bands profile. The electron Fermi level is set as the zero of energy $E_{F,e} = 0$ eV.

Another element that impedes the operation of the EHB-TFET device is the effect of the effective mass in the vertical quantization direction. The lighter the vertical effective mass, the larger the splitting of the sub-band energies and more difficult the alignment between valence and conduction sub-bands. Therefore, a heavier mass is favorable for the sub-band alignment. On the other hand, heavy effective mass in the quantization direction reduces the penetration of the wave-function into the channel [21], and hence the wave-function overlap in (2). Fig. 11 shows the profile of the valence and conduction bands and of the lowest light- and heavy-hole valley sub-bands together with the Δ_{100} and Δ_{010} conduction valley sub-bands (ignoring the second eigen-energy of the heavier longitudinal electron effective mass for clarity). The corresponding wave-functions are also shown. The light hole mass is $m_{lh} = 0.16m_0$ and the heavy hole mass is $m_{hh} = 0.49m_0$. Considering [010] to be the quantization direction, Δ_{100} has the quantization effective mass $m_{c,y} = m_t = 0.19m_0$, whereas the Δ_{010} has

$m_{c,y} = m_l = 0.91m_0$. The wave-functions corresponding to the heavier quantization masses form the ground state, but have the lowest overlap integral in (2). The simultaneous fulfillment of both sub-band energy alignment and strong overlap of the wave-functions is therefore problematic.

V. Conclusion

Extensive measurements in TFETs with variable front gate area and channel architecture demonstrate that EHB vertical tunneling in ultrathin Si or Si/SiGe TFETs is difficult to achieve. The main experimental argument is the lack of scalability of the tunneling current with the gate area and the absence of kinks in the current–voltage characteristics.

Numerical simulations confirm the experimental conclusion and explain the reasons. It turns out that EHB tunneling is a complex problem with many competing issues. In principle, an ultrathin body is suited for achieving a narrow tunneling barrier and high-tunnel current. This condition adversely affects the sub-band alignment due to size-quantization. The formation of the bilayer structure is also difficult without violating the super-coupling effect. Increasing the gate bias has a beneficial effect on the band alignment, but at the expense of very high, impractical vertical electric field. Furthermore, the effective mass anisotropy in Si and SiGe works against the wave-function overlap between the lowest energy sub-bands that determines the vertical BTBT. Thus, we believe that SOI or SGOI EHB-TFETs cannot work because the conditions for vertical BTBT cannot be fulfilled simultaneously. A design window may open in semiconductors with a lower bandgap only if the key requirements (band alignment, ultrathin tunneling barrier, bilayer buildup, low-vertical effective mass for both electrons and holes and reasonable fields) can intersect. Perhaps the problem does not have a solution. For example, in III–V compound semiconductor with a low bandgap (e.g. InGaAs, InAs) the quantization effect is exacerbated by the small electron effective mass, making band alignment more difficult to achieve.

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References

[1] A. C. Seabaugh and Z. Qin, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[2] F. Mayer *et al.*, "Demonstration of MOSFET-like ON-current performance in arsenide/antimonide tunnel FETs with staggered hetero-junctions for 300 mV logic applications," in *Proc. IEEE IEDM*, Dec. 2011, p. 781.

[3] J. Wan, C. L. Royer, A. Zaslavsky, and S. Cristoloveanu, "Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling," *Solid-State Electron.*, vols. 65–66, pp. 226–233, Nov./Dec. 2011.

[4] G. Dewey *et al.*, "Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," in *Proc. IEEE IEDM*, Dec. 2011, p. 785.

[5] C. Hu, "Green transistor as a solution to the IC power crisis," in *Proc. 9th Int. Conf. Solid-State Integr.-Circuit Technol., ICSICT*, Oct. 2008, pp. 16–20.

[6] R. Asra, M. Shrivastava, K. V. R. M. Murali, R. K. Pandey, H. Gossner, and V. R. Rao, "A tunnel FET for V_{DD} scaling below 0.6 V with a CMOS-comparable performance," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 1855–1863, Jul. 2011.

[7] L. Lattanzio, L. D. Michielis, and A.-M. Ionescu, "Electron-hole bilayer tunnel FET for steep subthreshold swing and improved ON current," in *Proc. Eur. Solid-State Device Res. Conf., ESSDERC*, Sep. 2011, pp. 259–262.

[8] L. Lattanzio, L. D. Michielis, and A. M. Ionescu, "Complementary germanium electron–hole bilayer tunnel FET for sub-0.5-V operation," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 167–169, Feb. 2012.

[9] L. Lattanzio, L. D. Michielis, and A. M. Ionescu, "The electron–hole bilayer tunnel-FET," *Solid-State Electron.*, vol. 74, pp. 85–90, Aug. 2012.

[10] C. Alper, L. Lattanzio, L. D. Michielis, P. Palestri, L. Selmi, and A. M. Ionescu, "Quantum mechanical study of the germanium electron–hole bilayer tunnel FET," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2754–2760, Sep. 2013.

[11] T. J. Teherani, S. Agarwal, E. Yablonovitch, J. L. Hoyt, and D. A. Antoniadis, "Impact of quantization energy and gate leakage in bilayer tunneling transistors," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 298–300, Feb. 2013.

[12] *Synopsys Sentaurus TCAD Sdevice 2012.06G User's Manual*, Synopsys, Inc., Mountain View, CA, USA, 2010.

[13] W. Vandenberghe, B. Sorée, W. Magnus, and M. V. Fischetti, "Generalized phonon-assisted Zener tunneling in indirect semiconductors with non-uniform electric fields: A rigorous approach," *J. Appl. Phys.*, vol. 109, no. 12, p. 124503, 2011.

[14] R. K. Pandey, K. V. R. M. Murali, S. S. Furkay, P. J. Oldiges, and E. J. Nowak, "Crystallographic-orientation-dependent gate-induced drain leakage in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2098–2105, Sep. 2010.

[15] S. Eminente, S. Cristoloveanu, R. Clerc, A. Ohata, and G. Ghibaudo, "Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects," *Solid-State Electron.*, vol. 51, no. 2, pp. 239–244, Feb. 2007.

[16] A. Villalon *et al.*, "Strained tunnel FETs with record ION: First demonstration of ETSOI TFETs with SiGe channel and RSD," in *Proc. Symp. Very Large Scale Integr. Technol., VLSIT*, Jun. 2012, pp. 49–50.

[17] J. Wan, C. L. Royer, A. Zaslavsky, and S. Cristoloveanu, "A tunneling field effect transistor model combining interband tunneling with channel transport," *J. Appl. Phys.*, vol. 110, no. 10, p. 104503, 2011.

[18] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct. 1983.

[19] A. Revelant, P. Palestri, P. Osgnach, and L. Selmi, "Calibrated multi-subband Monte Carlo modeling of tunnel-FETs in silicon and III–V channel materials," *Solid-State Electron.*, vol. 88, pp. 54–60, Oct. 2013.

[20] D. Esseni, P. Palestri, and L. Selmi, *Nanoscale MOS Transistors*. Cambridge, U.K.: Cambridge Univ. Press, 2011.

[21] T. Ando, A. B. Fowler, and F. Stern, "Electronic properties of two-dimensional systems," *Rev. Modern Phys.*, vol. 54, pp. 437–672, Apr. 1982.

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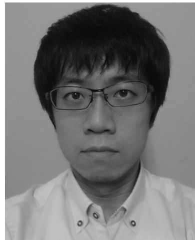

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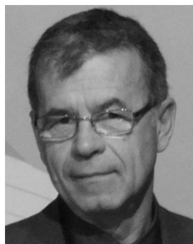

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