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# Comment on "Investigation of tunnel field-effect transistors as a capacitor-less memory cell" [Appl. Phys. Lett. 104, 092108 (2014)]

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In a recent paper,[1] Biswas *et al.* demonstrated a one-transistor dynamic random access memory (1T-DRAM) based on asymmetrical tunneling field effect transistor (TFET) with an underlapped front gate. The device operates in reverse bias between source and drain, with charge stored in the underlapped $L_{IN}$ region modifying the electric field at the source-channel tunnel junction and leading to a modulation of the TFET current that distinguishes the "0" and "1" states. In this comment, we compare the mechanism and performance of the TFET 1T-DRAM device of Biswas *et al.* with a different feedback-based operation mode of the same physical device used for the same 1T-DRAM application, which we have characterized in recent years.[2–5] In our version of the device, which we called the $Z^2$-FET (for *zero* subthreshold swing and *zero* impact ionization), the same asymmetrical structure is operated in forward bias, with front and back gates providing controllable injection barriers. The resulting performance appears significantly better in terms of operating current, current sensing margin, and speed.

The two structures are compared in Fig. 1. Both the TFET DRAM and the $Z^2$-FET DRAM (which comes in *p*-type and *n*-type configurations[4]) originate from the same asymmetrical TFET, in which only a part of the channel is covered by the front gate ($L_G$) and the rest is uncovered ($L_{IN}$) in order to reduce the ambipolar leakage current.[5] In both devices, the front and back gates are biased to form potential barriers in $L_G$ and $L_{IN}$ regions. However, in the TFET DRAM, there is reverse bias ($V_{DS} > 0$) between drain and source, leading to the potential profile in Fig. 1(c), whereas in the $Z^2$-FET, the drain-source bias is forward ($V_{DS} < 0$), leading to the potential profile in Fig. 1(d) for the *p*-type $Z^2$-FET.

Other important differences are the charge location and the reading mechanism. In the TFET DRAM,[1] the positive (hole) charge, stored within the potential well formed in the $L_{IN}$ region, is used to differentiate the memory states by modulating the $V_G$-controlled tunneling current. However, due to the $L_G$ region separating the stored charge and the tunneling junction ($P^+$-body), the stored charge has a weak effect on the tunneling current, leading to the weak hysteresis in the $I_D$-$V_{BG}$ curves in Fig. 2(a) and a very small (~20 nA) current difference between "1" and "0," as shown in Fig. 2(b).[1]

In the $Z^2$-FET, the source-drain junction is forward biased but the device stays in the *off* state under low $|V_D|$ due to the carrier injection barriers formed by the front and back gates. As the $|V_D|$ ramps up approaching to $|V_G|$, the barrier on the drain side is lowered and this triggers a feedback process between the hole and electron flows, which turns on the $Z^2$-FET abruptly.[2] In the *on* state, the $Z^2$-FET is essentially a forward-biased diode showing high current in the mA range. Figure 2(c) shows the $I_D$-$V_D$ curves of $Z^2$-FET with pronounced hysteresis controlled linearly by the front gate $V_G$. For DRAM operation,[3] the $Z^2$-FET stores the positive charge directly under the front gate in $L_G$ region. These charges are read out using a fast $V_D$ pulse and the discharge current turns on $Z^2$-FET abruptly through the feedback process. Figure 2(d) shows the $Z^2$-FET 1T-DRAM operation, in which the readout current of "1" state reaches 90 $\mu$A/$\mu$m and the device stays in the *off* state during the readout of "0," leading to a large sensing margin.

At the same time, the operating voltages required for the $Z^2$-FET 1T-DRAM are considerably lower, see Fig. 2. The reason for this is the low TFET tunneling current, which requires large gate and drain-source voltages of ~4 V to achieve the low measured currents of Fig. 2(b). Conversely, in the $Z^2$-FET, positive feedback collapses the injection barriers in the *on* state, leading to far higher current at lower operating voltage. The low TFET current is likely responsible for the slow access speeds of the device reported by Biswas *et al.* (<500 Hz), whereas the $Z^2$-FET 1T-DRAM was experimentally measured to work at 500 MHz (limited by the available test equipment) and has <1 ns access speed in simulation.[4]

In case of the advent of TFETs replacing MOSFETs in CMOS technology as logic switches, the device of Biswas *et al.* would be the first TFET-based memory concept. We note that if the TFET tunneling current were higher, due to sharper junctions or the use of a lower bandgap material in the channel, the operating voltage of the TFET 1T-DRAM could conceivably fall below that of the $Z^2$-FET DRAM, but for now the operating voltage comparison is clearly in the $Z^2$-FET's favor (see Fig. 2).

Other useful properties of the $Z^2$-FET DRAM include the non-destructive reading, thanks to the regeneration of the stored charge,[3] and the relatively small stored charge needed to distinguish the "0" and "1" states due to amplification of discharge current for short pulses.[3,4]

In conclusion, we agree with Biswas *et al.*[1] that the underlapped asymmetric TFET structure of Fig. 1 has interesting memory properties, but we believe the previously reported feedback-based forward-bias operation[2–4] is superior

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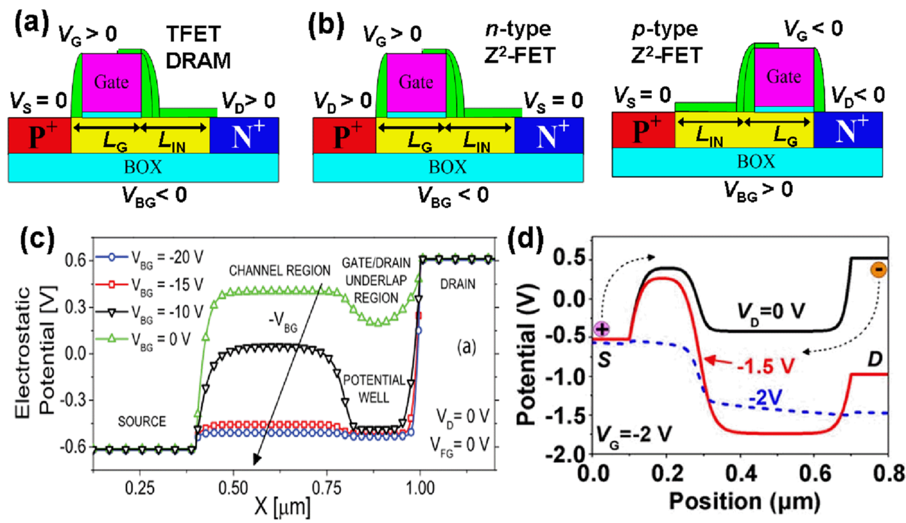


FIG. 1. The device structure and biasing of (a) TFET DRAM[1] and (b) $Z^2$-FET DRAM,[4] and the corresponding potential profiles of TFET DRAM in (c) and *p*-type $Z^2$-FET in (d).

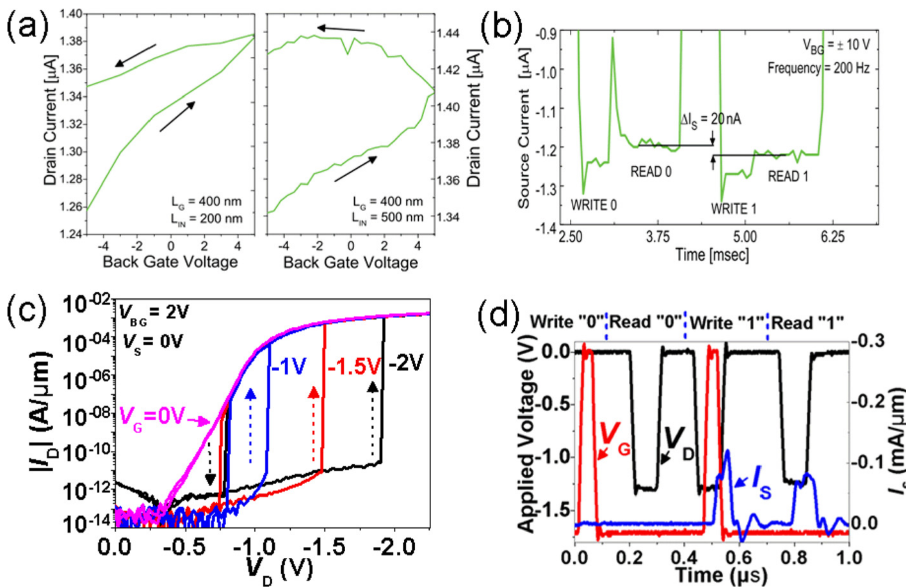


FIG. 2. (a) The $I_D$-$V_{BG}$ direct current (DC) characteristics and (b) transient measurement of TFET DRAM operation[1] and (c) and (d) show the corresponding $Z^2$-FET $I_D$-$V_D$ curve and transient measurement, respectively.[3]

for 1T-DRAM applications in several respects such as read-out current, applied voltage, and access speed.

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