ECS Transactions, 66 (5) 201-210 (2015)
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Special Memory Mechanisms in SOI Devices

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Several types of floating-body capacitorless 1T-DRAM memory cells with planar SOI or multi-gate configuration are reviewed and compared. We show that 1T-DRAMs are also compatible with the 'unified memory' paradigm which aims at combining, within a single SOI transistor, volatile, nonvolatile and multiple-state memory functionalities. We focus on our recently proposed concepts (MSDRAM, A2RAM and Z^2-FET), by addressing the device architecture and fabrication, operating mechanisms, and scaling issues. Experimental results together with numerical simulations indicate the directions for performance optimization.

Introduction

The conventional dynamic random access memory (DRAM) is composed of a transistor and a charge-storage capacitor (1) that can be billion-times cloned. DRAM circuits have been extremely successful for several decades, generating infinite benefit for our information society. However, their further miniaturization appears to be blocked by the difficulty to shrink the capacitor size without adversely affecting the amount of stored charge needed to discriminate '0' and '1' states. A paradigm shift consisting in the suppression of the storage capacitor is ineluctable. This pragmatic vision led to rapidly growing interest in alternative memory mechanisms: resistive memory, spintronics, floating-body single-transistor 1T-DRAM. We will focus on the latter approach where the charge is stored directly in the isolated body of SOI MOSFET which is also used to read the information.

Many versions of 1T-DRAM have been proposed, including planar SOI MOSFET with single- or double-gate control, FinFETs, nanowires, etc (2-24). We will review the most attractive concepts compatible with FDSOI technology, namely the MSDRAM (9), A2RAM (22), and Z^2-RAM (23). The device configuration and the methods for memory programming and reading will be discussed.

Even more ambitious is the 'unified' memory (25-31) which combines, within a single SOI transistor, volatile and nonvolatile memory functionalities as well as multiple memory states.

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1T-DRAM Operation Mechanisms

In this section, we describe the toolbox used to conceive most of the 1T-DRAM cells proposed so far. The isolated body of SOI transistors can be charged with majority carriers. The memory operation takes advantage of floating-body effects and coupling mechanisms. In all 1T-DRAM variants, state '1' (high drain current) reflects an excess of majority carriers (holes) in the body which increases the potential and hence the electron drain current. Conversely, state '0' features a lower current due to the removal of holes from the body.

In FD SOI MOSFETs, there is no neutral region and a negative gate bias is required to maintain the holes near the interface (potential well). Below are ranked the mechanisms used to program state '1' by generating holes.

(i) ***Band-to-Band tunneling (B2BT).*** When the local electric field is high enough (large negative gate pulse and positive drain pulse), the holes are generated at the gate-to-drain (source) overlap region (8-10). When the gate returns to a less negative value (used for 'hold' and 'read'), the hole concentration is larger than at equilibrium. The resulting temporary excess current (overshoot) makes B2BT mechanism very attractive. Compared with other programming methods, the holes are less likely to escape through the junctions because the body potential is negative.

(ii) ***Impact ionization.*** A drain bias V_D pulse being applied, the holes generated in the pinch-off region, close to the drain, accumulate at the negatively biased interface (2-5). Impact ionization allows fast 1-state writing but involves high power consumption and reliability issues (hot-carrier degradation).

(iii) ***Bipolar junction transistor (BJT).*** The BJT is intrinsic element in SOI MOSFET and uses the N^+, P-body and N^+ regions as emitter, base and collector (6,7). Negative V_D and V_{GF} pulses are used to forward bias the body/drain (emitter) junction and generate electron/hole pairs by impact ionization at the body/source junction. The holes are retained by the gate within the body. A superior programming scheme utilizes positive pulses on gate and drain. The gate switch from a negative bias (needed for carrier storage) to zero bias increases the body potential and turns on the source (now acting as emitter) junction. Hole generation by impact ionization now occurs at the reverse biased body/drain junction. Programming and reading in BJT mode is fast and power efficient but requires relatively high drain voltage, detrimental for device cycling.

(iv) ***Additional methods.*** Gate tunneling current (14) and photo-generation (15) are marginal mechanisms able to generate holes.

Switching from 1-state to 0-state requires the holes to be eliminated from the body. The programming of 0-state is less demanding. To evacuate the holes from the body, there are two options:

(i) ***Forward biasing*** the drain- or source-body junction**.**

(ii) ***Positive pulse*** on the gate that increases the body potential (by dynamic coupling) above equilibrium and inherently turns on the junctions.

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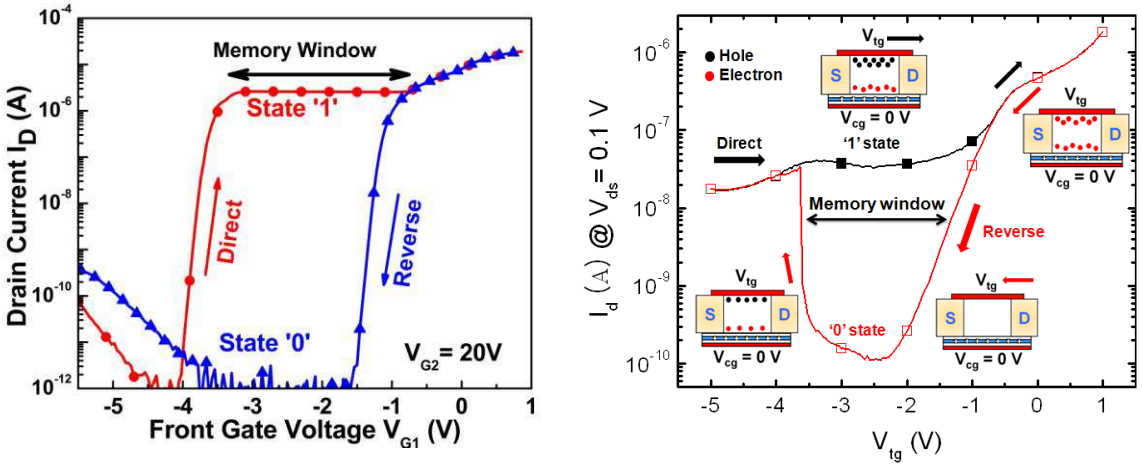
Other general aspects are worth mentioning:

- State '1' is permanent (equilibrium condition) and does not require refresh.
- The memory retention time is mostly limited by the parasitic generation of holes in 0-state.
- Memory reading is non-destructive because the drain voltage is low (except for BJT method) and does not alter the memory states.

MSDRAM Device

The MSDRAM is based on the Meta-Stable Dip (MSD) effect which results in a hysteresis as shown in Fig. 1a (9). The back channel of the FDSOI MOSFET is biased in moderate inversion ($V_{GB} \geq V_{TB}$) and the front gate is swept from strong accumulation to nearly 0V. For high negative V_{GF}, B2B tunneling occurs and rapidly supplies holes in the front channel. Since the memory is at equilibrium, a high current flows at the back channel. For reverse V_{GF} scan, the situation is totally different: there is no source to provide holes fast enough, hence the body potential drops in deep depletion, temporarily suppressing the back-channel current. The very wide hysteresis ($-4 < V_{GF} < -2$, in Fig.1) is used as a memory window. The current ratio I_1/I_0 between '1' and '0' states exceeds 6 orders of magnitude.

The MDRAM takes full advantage of double-gate operation and coupling between the hole and electron channels. The memory status can be read even at very low drain voltage which is important for low-power consumption and reliability. The architecture of source and drain is tailored (gate underlap, etc) such as to enhance B2B tunneling for quick programming of '1' state and to inhibit it during 'hold' phase for longer retention time. A thin BOX allows reducing the programming voltage (≤ 2 V) and back-gate bias.



(a) **(b)**

Figure 1. Measurements demonstrating the MSDRAM concept: drain current versus decreasing (reverse scan) and increasing (direct scan) front-gate bias. (a) FDSOI MOSFET operated with V_{GB} = 30 V and V_D = 0.1V (T_{BOX} = 400nm, L= 1.5µm). (b) MOSFET with ONO BOX acting as non-volatile memory (NVM). The back gate is grounded, hence the MSD hysteresis effect is entirely governed by the BOX charge (29). A positive charge stored in the nitride can invert the back channel.

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The MSDRAM scalability was investigated by 2D simulations of a 35-nm-long channel cell with optimized architecture. The retention time for I_1/I_0=10 was long (14 s) and the programming time short (5 ns). Recent measurements confirm that the MSD effect is maintained in small-area MOSFETs (0.1 μm^2) (24). Fig. 2a shows the measured back-channel drain current versus back-gate voltage for both memory states, '1' and '0', in a cell featuring only 0.064 μm^2. The back-channel threshold voltage is shifted, by coupling effect, according to the presence or absence of holes at the top interface.

Despite this memory cell is nothing but a regular FDSOI MOSFET without MSDRAM optimization, very high current margins (I_1 - I_0 > 180 μA/μm) can be obtained, surpassing other advanced 1T-DRAM candidates (2-8). Fig. 2b illustrates the strong dependence of the current margin and retention time on gate length. Retention times exceeding 450 ms can be achieved at room temperature (24). Decreasing the gate length from L = 100 nm to 80 nm causes a small increase in the current margin and retention time. This is explained by a more effective hole injection by band-to-band tunneling thanks to the higher lateral electric field. Short-channel effects are responsible for the performance degradation when shrinking the memory cell beyond L = 80 nm. The intrusion of source and drain depletion regions into the potential well degrades the hole storage efficiency.

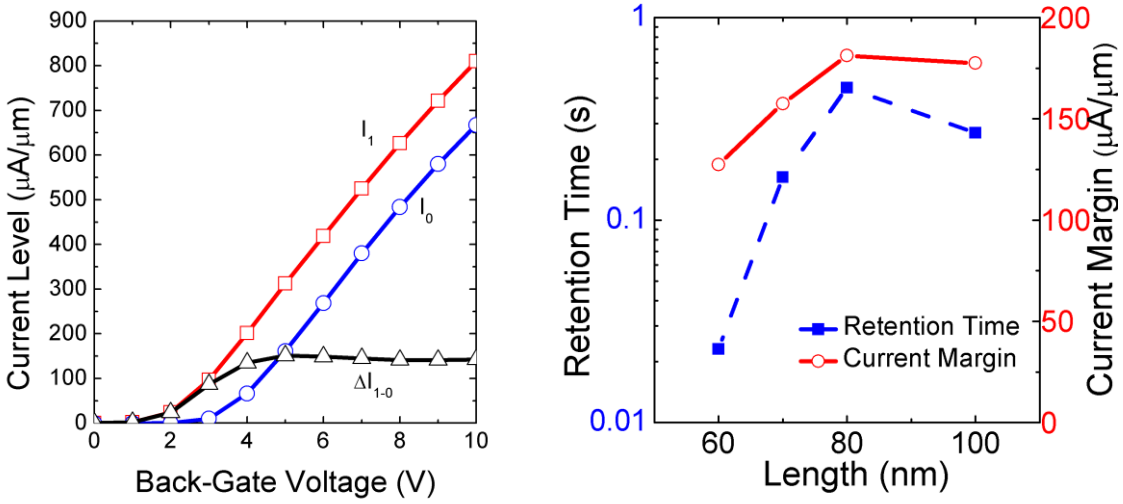

Figure 2. (a) Experimental current in both MSDRAM memory states and current margin ($I_1 - I_0$) versus back-gate voltage, L = 80 nm. (b) Measured current margin and retention time against the gate length. T = 300 K, W = 80 nm, EOT = 3.1 nm, t_{Si} = 25 nm, t_{BOX} = 25 nm and $N_A = 2 \cdot 10^{17}$ cm^{-3}.

The operation of most 1T-DRAMs, including the MSDRAM, is based on the coexistence of electrons and holes in the body. In ultrathin SOI films (T_{si} < 10 nm), the so-called *super-coupling effect* forbids the formation of accumulation and inversion layers facing each-other (20). Since only electrons or only holes can be present in the body, the memory effect vanishes.

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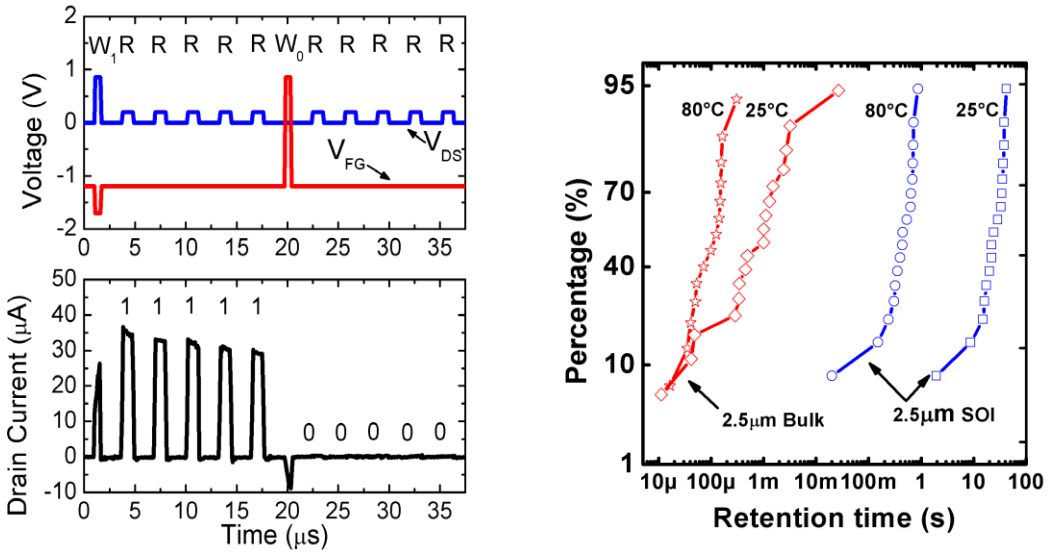
A2RAM Device

The aim of the A2RAM concept is two-fold: eliminate the back-gate action and solve the super-coupling problem (21,22). To this purpose an N^+ layer is implemented, by ion implantation or selective epitaxial growth, at the bottom of the fully depleted P^- body. This means that the source and drain are short-circuited by the N^+ bridge. Holes are stored at the front gate whereas the N^+ bridge serves for current sensing. Holes accumulated at the surface (thanks to a negative V_{GF}) screen the vertical electric field enabling an electron current flow through the bridge. By contrast, if the surface is temporarily depleted of holes, the gate field is no longer screened; the bridge becomes fully depleted and the drain current is suppressed (Fig. 3a).

It is important to note the similarity of A2RAM and MSDRAM. Both are programmed by B2BT (1-state) and dynamic coupling (a positive gate pulse restores 0-state by eliminating the holes). Efficient reading of the cells is performed with the MSD hysteresis effect. The sole difference is the nature of the back channel: electrostatically induced by the back gate (MSDRAM) or physically implemented (A2RAM).

Preliminary measurements have validated the A2RAM concept (22). Fig. 3a shows the bias pattern of a programming sequence and the resulting drain readout current on 22nm-node SOI cells. After the writing (W_1) operation, five consecutive reads show a relatively high and nearly constant current in state '1'. On the other hand, the current is negligible after the erase (W_0) event. This reflects the full depletion of the implanted N-bridge between source and drain.



(a) **(b)**

Figure 3. (a) Experimental bias pattern and readout current in A2RAM fabricated with 28nm FDSOI technology (W = 10 µm, L = 100 nm, EOT = 3.1 nm, t_{Si} = 36 nm and t_{BOX} = 10 nm). (b) Cumulative distribution of the retention time for bulk and SOI A2RAM cells fabricated with 2.5 µm technology. W = 30 µm, L = 4 µm, t_{OX} = 30 nm (t_{Si} = 350 nm and t_{BOX} = 400 nm for SOI).

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A2RAM cells have also been processed with a less advanced 2.5 µm technology on SOI and bulk substrates. Fig. 3b demonstrates the A2RAM memory behavior, even for bulk substrates, thanks to the multi-body cell architecture. The N-bridge prevents the holes from escaping through the substrate. Nevertheless, the performance of bulk samples is severely degraded when compared to SOI. Retention times of over 25 s and 100 ms are extracted at room temperature for SOI and bulk substrates, respectively. This comparison confirms the advantage of SOI isolation that improves the integrity of the two memory states.

Increasing the temperature adversely impacts the memory performance mainly due to the parasitic repopulation of holes during state '0'. The retention time is shorted by one order of magnitude at 80°C.

Z^2-FET Memory Device

The Z^2-FET is a different device, a special gated PIN diode rather than a MOSFET. The undoped floating body is partially covered by the control gate as shown in Fig. 4a. The diode is forward biased in double-injection mode and the electron/hole current is normally high. The key point is to bias the gate and the substrate such as to form potential barriers that block the injection of electrons and holes from the N^+ and P^+ contacts, respectively. The biasing scheme shown in Fig. 4a emulates a PNPN thyristor without needing body implants. The doping of the P and N base regions is virtual, induced electrostatically by the top gate and the back gate (ground plane), respectively.

A typical output $I_D(V_D)$ characteristic is reproduced in Fig. 4b (23). As long as the 'thyristor' is blocked in 'off' mode, the current is very low. At some point, V_D is high enough to lower the electron injection barrier. Electrons injected from N^+ contact into the body flow to the source where they reduce the hole injection barrier. Some holes now can flow from P^+ source to drain, further reducing the electron barrier. A positive feedback occurs that turns the device on and completely flattens the injection barriers. The feedback mechanisms gives rise to a strong hysteresis in $I_D(V_D)$ curves (Fig. 4b) which is useful for capacitor-less memory. The Z^2-FET features extremely sharp transition with triggering voltage controlled by the gate bias, which adds further flexibility to the memory.

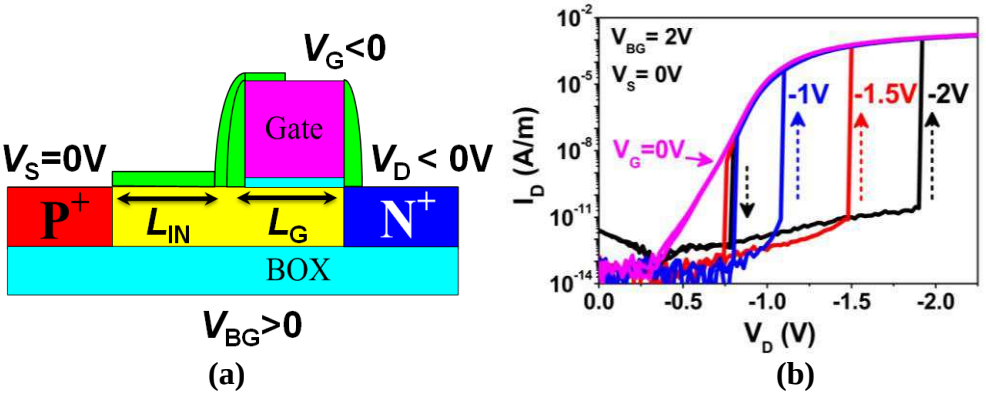

Fig. 4. (a) Schematic of the Z^2-FET memory and (b) typical output $I_D(V_D)$ characteristics showing hysteresis controlled by the gate voltage.

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A similar 'vertical' switch from off- to on-state is observed in $I_D(V_G)$ characteristics. Thanks to the band modulation effect, the subthreshold swing is below 1 mV/decade without involving impact ionization. This explains the name given to the device: Z^2 means zero impact ionization and zero subthreshold swing.

The 1T-DRAM operation consists in turning the device on ('1' state) and off ('0' state). To program the '1' state, holes are stored under the negatively biased gate (23). Memory reading consists in discharging this stored charge: the discharge current $\Delta Q_G/\Delta t$ is sufficient to turn on the Z^2-FET and the read current is high. In '0' state, no holes are stored under the gate. Since there is no discharge current, the diode remains blocked and the read current is negligible. The Z^2-FET memory cumulates high speed capability, scalability down to 20-30 nm gate length, long retention, and 1 V operating voltage. Reading is regenerative rather than destructive. Frequent reading extends the retention time because it eliminates the parasitic holes that accumulate under the gate and tend to corrupt '0' state.

The key advantage is that the memory effect does not depend on the number of stored carriers as in DRAMs and other 1T-DRAMs. Only the discharge current matters, in other words even if the charge stored is modest in miniaturized devices, it is sufficient to use very fast read pulses (1 ns).

Unified Memory

The ideal 'universal memory' that offers high speed, high density, and non-volatility is still to be discovered. An intermediate step is the 'unified memory (URAM) able to combine non-volatile memory (NVM) and DRAM functionalities in a single transistor.

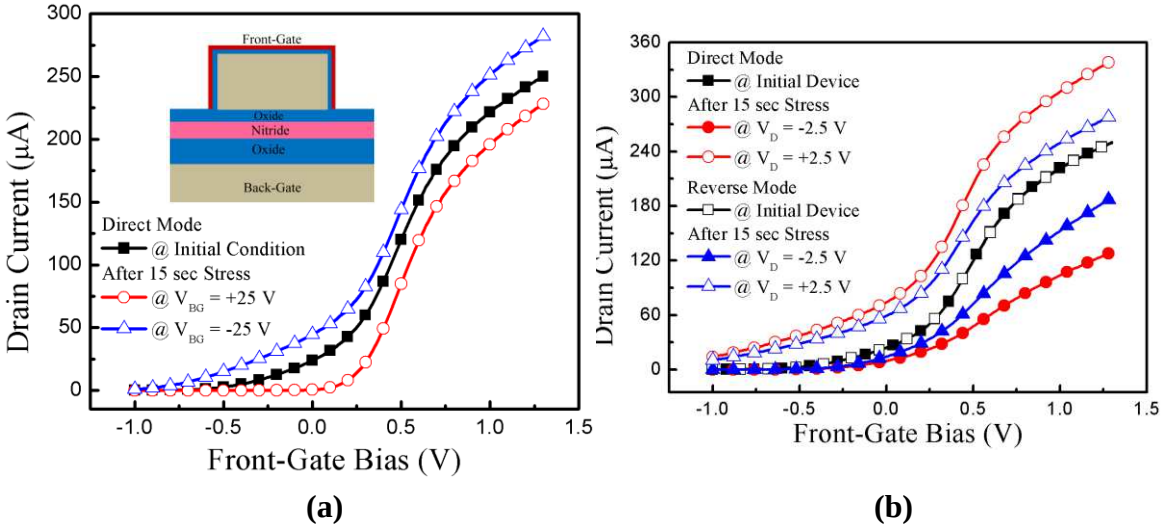

Fig. 5. Transfer characteristics of a FinFET with buried ONO stack tested as unified memory. Nonvolatile carrier trapping in the Si_3N_4 layer is programmed by (a) back-gate or (b) drain biasing. L_G = 100 nm, W_F = 90 nm, V_{BG} = 0 V, V_D = 50 mV.

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The URAM concept has been demonstrated by adding a NVM charge trapping layer (for example, oxide/nitride/oxide (ONO) stack) to the 1T-DRAM (Fig. 5a) (25-30). Electrons or holes are injected (by Fowler-Nordheim or hot carrier mechanisms) and trapped into the silicon nitride layer. In the meantime, the floating body is used as a storage volume for the 1T-DRAM function. Planar MOSFETs with ONO BOX have been fabricated for URAM tests (29). A positive charge trapped in the ONO acts as a positive back gate. This enables the MSDRAM to operate in single-gate mode (at V_{GB} = 0V, see Fig. 1b) and to show multi-bit capability (29).

Figure 5 shows the URAM implementation within a FinFET (28). The NVM charge is detected, via coupling effect, by the current flowing at the front-gate. The physical separation of the two interfaces used for programming (back) and reading (front) avoids the disturbance of the stored charge during sensing. In Fig. 5a, the back-gate bias was used to store electrons ($V_{GB} > 0$) or holes ($V_{GB} < 0$) in the nitride. Due to 3D coupling effects, the NVM is more efficient in short and not too narrow FinFETs (28).

An alternative programming method makes use of the drain voltage (Fig. 5b). For V_D = +2.5 V (with $V_{GB} = V_{GF} = 0$), holes are injected and trapped into the ONO whereas for V_D = -2.5 V electrons are trapped. The front-channel current is very sensitive to the type and amount of charge stored (Fig. 5b). The retention time exceeds 10 years. Since the charge is actually localized near the drain, the $I_D(V_D)$ curves measured in direct mode (source-to-drain) and reverse mode (drain-to-source) are different. This property opens the door to 'multiple bit' URAM. As experimentally demonstrated, positive *or* negative charges can be trapped near the drain *or* near the source. These four memory states are easily discernable: the charge polarity is deduced from the current level (increased or decreased) and the charge location from the difference between direct and reverse currents (28).

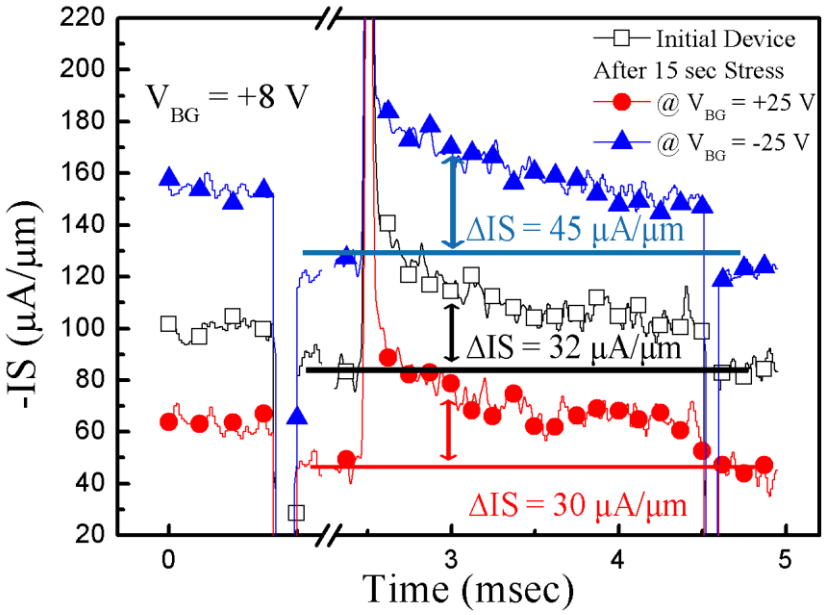

Fig. 6. Demonstration of multi-bit unified memory in ONO FinFET. Transient currents in '1' and '0' states of the 1T-DRAM before and after the programming of positive or negative nonvolatile charge.

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Same devices were operated in 1T-DRAM mode (Fig. 6). For programming and reading, the back-channel is inverted (V_{BG} = +8 V > V_{THB} = +3.5 V) while the front interface is accumulated (V_{FG} = -1 V). The '1' state is set by impact ionization (V_D = +1.5 V) or band-to-band tunneling. Excess holes are stored in the Si body and increase the potential so that the current level is 'high'. For 0-state, negative drain (V_D = -0.5 V) and positive front-gate (V_{FG} = +0.8 V) voltages are applied. The body-drain junction is forward biased and the stored holes are eliminated, hence the drain current level becomes 'low'. The difference in current between '1' and '0' states (*i.e.*, sensing margin) is 32 μA/μm (open square symbol) and fully confirms 1T-DRAM operation (32).

The crucial aspect is that the *volatile* current levels can be combined with the *nonvolatile* charges stored in the ONO (blue triangle and red circle curves in Fig. 6). Positive (negative) charges injected into the nitride clearly induce an increase (decrease) of the 1T-DRAM current.

The nonvolatile charge can be programmed by back-gate biasing (as in Fig. 6) or by localized hot carrier injection, which doubles the number of memory states (32). These results affirm the concept of multi-bit unified memory with combined nonvolatile and volatile memory operations and decent sensing margin (32–45 μA/μm) in regular ONO FinFETs. Albeit device optimization will massively improve the performance, several practical aspects need to be solved: interference between the programming voltages of 1T-DRAM and NVM, decorrelation of the threshold voltage shifts or current levels resulting from the volatile and non-volatile memory functions, etc.

Conclusion

The floating-body capacitorless 1T-DRAM is attractive for low-power, embedded memory solutions. We have described the principles of several competing versions: MSDRAM, A2RAM and Z^2-FET. B2B tunneling is suitable for 1-state programming, as the capacitive coupling is for 0-state. Except for Z^2-FET, the main concern is the retention time in very short 1T-DRAM cells. The volatile functionality can be enriched, by adding nonvolatile capability, in order to achieve the unified memory. Preliminary tests with SOI transistors and ONO FinFETs demonstrate that unified and multi-bit memory cells are realistic.

Acknowledgements

ANR AMNESIA project (ANR 2011 JS03 001 01), Place2be and Compose3 European projects are thanked for support.

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