A Simulation Framework for Analyzing Transient Effects Due to Thermal Noise in Sub-Threshold Circuits

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ABSTRACT

Noise analysis in nonlinear logic circuits requires models that take into account time-varying biasing conditions. When considering thermal noise, which moves the circuit away from its equilibrium point, a correct modeling approach has to go beyond the additive white Gaussian noise (AWGN) used in classical noise analysis. Even when accurate models are available, running standard Monte-Carlo simulations that will expose rare soft errors may still be computationally prohibitive. Probabilistic methods are often preferred for estimating the failure rate. However, these approaches may not provide any insight about the dynamic response to noise events. In this paper, we target both problems in the sub-threshold logic application domain. We first provide a time-domain model for fundamental, technology–independent thermal noise in sub-threshold circuits. Then, we use this model to generate noise input files for SPICE transient analysis. The effectiveness of the approach is demonstrated using 7nm FinFET predictive technology models (PTM) for an inverter and a NAND gate.

Categories and Subject Descriptors

I.6.5 [**Simulation and Modeling**]: Model Development— *Modeling methodologies*

Keywords

thermal noise,noise analysis,time-domain simulation,CMOS logic circuits,sub-threshold circuits

1. INTRODUCTION

The classical approach to modeling thermal noise in electronic circuits assumes that the magnitude of the noise is small enough to consider linear response. The assumption of linearity, however, cannot always be justified in logic circuits, especially when operating in the sub-threshold regime in which the supply voltage V_{DD} is kept below the threshold voltage of the transistors[3][5]. In these operating conditions, the number of electrons in the channel is so small that even small fluctuations can have a pronounced impact on the circuit biasing point.

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Therefore, noise analysis for nonlinear logic circuits requires using models that take into account the time dependence of the circuit biasing conditions. The authors of [14] and [13] have shown that taking time-varying biasing conditions when computing the capture and emission rates in random telegraph signal (RTS) noise, can lead to much more accurate models. Their results are useful for obtaining improved spectral noise analysis. The authors of [12] have defined an analytical model for thermal noise. Their approach considers the load capacitor of an inverter as a queue in which the arrival and departure rates are modeled after the forward and reverse drain currents of the transistors. This representation is derived from Sarpeshkar's fundamental work [17] in which the author presented a unified model for thermal noise, viewed as two-sided shot noise process. A queue representation of the output current fluctuations was then used for computing the probability of a soft error in sub-threshold operation. More recently, similar approaches [8][9][10] have been used for modeling the error rate of flip-flops both in sub-threshold and above-threshold operation for end-of-roadmap CMOS technology.

We note that all these works have focused on the analysis of thermal noise in the frequency domain by studying the probability of soft error events. While this has led to some interesting results, we still lack a time-domain framework necessary for capturing the dynamic response to noise in nonlinear circuits. In this paper, we extend the same unified model for thermal and shot noise [8][9][10] to the time domain by modeling the noise fluctuations as a stochastic process.

Our approach requires an understanding of how the statistics of the Poissonian processes describing the charging and discharging rates are affected by the time-varying physical characteristics of the devices. While creating an accurate model for this stochastic process is feasible, the greater challenge is creating one that is computationally-affordable, such that it can be used for simulations over relatively long time frames to capture rare errors that cannot be seen in standard Monte Carlo simulations. This is particularly desirable when doing repeated simulations for design exploration.

For example, if we were to apply this model directly to SPICE circuit simulations, we would need to run a transient analysis in the time range of seconds with time steps on the order of picoseconds, in order to guarantee resolution greater than the fastest response time of the circuit, with the hope of encountering some rare noise pattern that may trigger a soft error in the circuit. Even by employing Monte Carlo methods, this approach would make simulation times too long to be of any practical use.

Instead, our approach is to use a two-step method in which we first look for rare failure-inducing events in the form of stochastic

current fluctuations using a fast ad-hoc simulator and then extract the desired portion of the time series to simulate the fault in SPICE. As a result, we can potentially compress simulated times of seconds down to the microsecond scale. In addition, our approach allows us to simulate for rare noise events in a matter of a few hours, rather than weeks. We demonstrate the effectiveness of our approach, both in terms of accuracy and simulation time, using 7nm FinFET models.

The remainder of the paper is organized as follows. In Section 2 we briefly review the analytical description of thermal noise in a CMOS transistor as a two-sided Poisson process, as was first shown in [12]. We then extend the analysis in Section 3 by studying the effect of the response time on the noise amplitude. Once we have established the features of the time-domain model, in Section 4 we describe the implementation of the model for a CMOS inverter and a NAND gate using 7nm FinFET predictive technology models (PTM)[18][16]. The results for both gates are validated against the statistical expectations derived from Monte Carlo simulations. In Section 5, we present the our simulation framework and provide some examples showing how this approach preserves the dynamic properties of thermal noise and allows speeding up time-domain SPICE noise simulations.

2. TWO-SIDED POISSON SHOT NOISE

The effect of thermal noise in a logic gate can be explained considering the fluctuations of the charge in the load capacitor C_{out}. If we consider the inverter in Figure 1, the mean flow of electrons in the load capacitance is determined by the equilibrium current flowing in the transistors. In sub-threshold, this current is given by:

$$I_D = I_0 \exp\Big(\frac{qV_{gs}}{mkT}\Big) \exp\Big(\frac{qV_{ds}\lambda_D}{kT}\Big)\Big[1 - \exp\Big(-\frac{qV_{ds}}{kT}\Big)\Big] \quad (1)$$

where λ_D is the DIBL parameter [20] and m is the ideality factor. Due to thermal agitation of the carriers, the charge stored in C_{out} is not constant. The number of electrons leaving or arriving at the output node is a Poisson distributed random variable and fluctuates in time. We can therefore describe the fluctuations of electrons at the output node as the result of four Poisson processes whose rates are associated with the transistor currents. Each transistor in the inverter has two rates associated with it, one for the forward current and one for the reverse current. For our subthreshold operated gates, the supply voltage $V_{DD} \approx 180mV$. These rates can be conveniently expressed in number of electrons per picosecond [12]:

$$\mu_n = \frac{I_0}{q} \exp\Big(\frac{qV_{out}\lambda_D}{kT}\Big) \exp\Big(\frac{qV_{in}}{mkT}\Big) \times 10^{-12} \quad (2)$$

$$\lambda_n = \mu_n \exp\Big(\frac{-qV_{out}}{kT}\Big) \quad (3)$$

$$\lambda_p = \frac{I_0}{q} \exp\Big(\frac{q(V_{DD} - V_{out})\lambda_D}{kT}\Big) \exp\Big(\frac{q(V_{DD} - V_{in})}{mkT}\Big) \times 10^{-12} \quad (4)$$

$$\mu_p = \lambda_p \exp\Big(\frac{-q(V_{DD} - V_{out})}{kT}\Big) \quad (5)$$

In these formulas we use λ for the rates of the processes charging the capacitor and μ for the rates discharging the capacitor. A property of the Poisson processes allows us to simplify the notation further. If we consider two Poisson processes with rates λ_1 and λ_2, the cumulative number of events associated with the two processes is still a Poisson process with rate $\lambda = \lambda_1 + \lambda_2$. Then, we can assume one Poisson charging process with arrival rate $\lambda = \lambda_n + \lambda_p$ and one Poisson discharging process with departure rate $\mu = \mu_n + \mu_p$.

This final form shows that the thermal noise fluctuations are in fact, the result of two competing Poisson processes. In ideal conditions, the two logic states "1" and "0", correspond to having full charge or zero charge on the output capacitor. Random fluctuations in the electron population for the two equilibrium states change the charge stored in the capacitor and can lead to a switch in the output logic state if the excursion from the equilibrium is large enough. This mechanism was described in [8] using a probabilistic framework based on 2–D Markov chain for analyzing sub–threshold flip–flops and extracting the probability of soft error, *i.e.*, finding the probability of going from the correct stable state to the other as an effect of noise fluctuations. However, it does not help in characterizing the transient behavior of the circuits in the presence of noise. Our goal is to provide an alternative approach that can be used to apply the results from the two-sided shot noise model to time-domain simulations. The value of the rates as extracted directly from the drain current (1) require a good match with the currents from the BSIMCMG model we used in our simulations. The curve fitting obtained by applying the DIBL correction is shown in Figure 2. We used $\lambda_0 = 0.07$ and $m = 1.2$ for the NMOS and $\lambda_0 = 0.08$ and $m = 1.3$ for the PMOS. The mismatch at low values of V_{ds} are due to the fact that we are still considering a relatively simple model for the sub–threshold current, which does not incorporate all the parameters used in the BSIMCMG model. For our simulator, we decided to implement all current and parameter models as a look–up table. This approach helps speeding up the calculations since the parameters have to be computed only once.

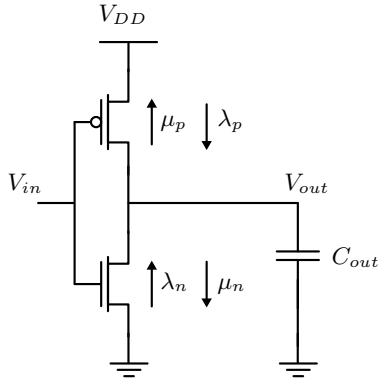


Figure 1: Inverter rates for NMOS and PMOS transistors.

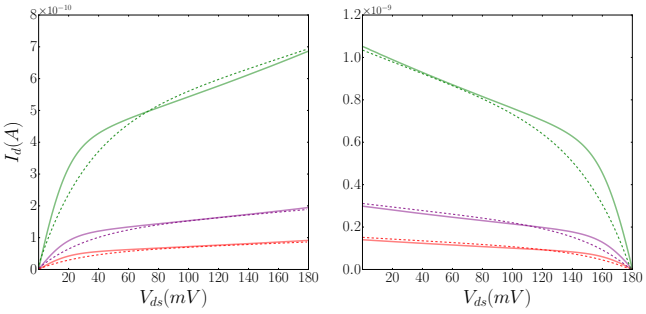


Figure 2: Comparison of the IV curves from the BSIMCMG 7nm FinFET model (solid lines) and the sub–threshold current model from (1) (dashed lines).

Should more accuracy be needed, we could still get rid of the mismatch from the curve fitting and implement the look–up tables using parameters extracted directly from SPICE simulations. In our analysis the parameters' calculation were not noticeably affected by the curve fitting approximation. Therefore, we chose to use the simpler current model. The details of the implementation will be discussed in Section 4.

3. ORNSTEIN–UHLENBECK PROCESS – THE EFFECT OF RESPONSE TIME ON NOISE AMPLITUDE

In this section we show how the response time of the circuit affects the final noise amplitude in the time-domain. The Ornstein–Uhlenbeck (OU) process [6][21] was first introduced for the study of Brownian motion. Its current applications span from the study of neural spikes to the representation of stock volatility in financial economics [1][19]. The use of an OU process to describe this circuit essentially extends a single-pole infinite-impulse-response (IIR) model of the circuit rigorously into a statistical description. As we have already established in the previous section, the mean current into the inverter output node is $I_{tot} = I_\lambda - I\mu$. However, the fluctuations in the two Poisson charging and discharging processes are additive and that sum $I_{SHOT} = |I_\lambda| + |I_\mu|$ is proportional to the variance of the shot noise current in the node. To do a time domain simulation of the circuit responding to a process of this type, one selects a small time interval, say Δt, and computes as a random variable a possible estimate the number of electrons entering the node X_t in that interval and from that computes the next output voltage value using the OU process model. This action repeats to produce a time series of output voltages. If Δt is sufficiently large ($\sqrt{\overline{X_t^2}} \geq 50$), then these pulses will resemble a Gaussian process and the calculation can be done very efficiently. However, if Δt is comparable to or larger than the instantaneous time constant of the circuit, then the circuit node voltage will relax back to its original value between pulses and this is not physically accurate. This situation is well described by the Ornstein–Uhlenbeck process [2].

Consider the time series describing the amplitude of the shot current pulses X_t in terms of the number of electrons at each time $t = n\Delta t$, where Δt is the unit time used for counting the number of events from the Poisson distribution. Consider also the instantaneous time constant of the circuit

$$\tau = \frac{1}{g_{dsNMOS} + g_{dsPMOS}} \times C_{out},$$

where C_{out} is the total capacitance at the output node including any input capacitance of the following stages. The resulting thermal voltage noise process V_t is related to X_t by a factor $\Delta V = \frac{q}{C_{out}}$ which is the voltage change due to a single electron on the capacitor. In our simulation $\Delta V = 1.1mV$. The OU process derives from the solution of a stochastic differential equation of the form [1]:

$$dv(t) = -\lambda v(t)dt + dW(t) \tag{6}$$

where $W(t)$ is a Lévy process[7]. Examples of Lévy processes are the Wiener process, used for describing the Brownian motion, and the Poisson process. The discrete time solution of Equation 6 can be expressed as:

$$V_0 = 0, \;\; V_t = V_{t-1} \exp\Big(-\frac{t}{\tau}\Big) + X_t \frac{q}{C_{out}}. \tag{7}$$

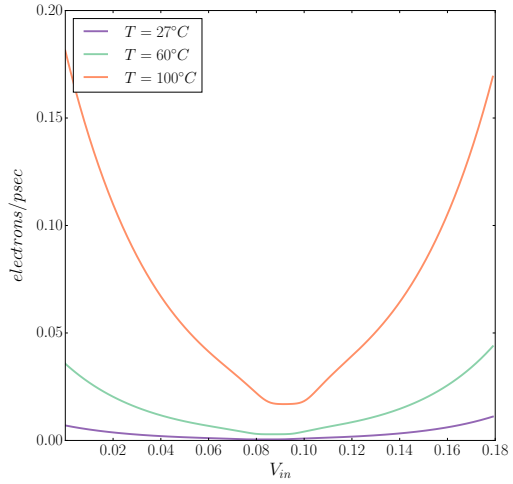


Figure 3: Charging rate λ as a function of the input voltage V_{in} for a CMOS inverter. The rate is expressed in electrons per picosecond.

With this expression for how the time response of the circuit combines with the noise current time series, we can integrate this information with the rates computed above to get the standard deviation of the noise as a function of the biasing point, as explained in the next Section.

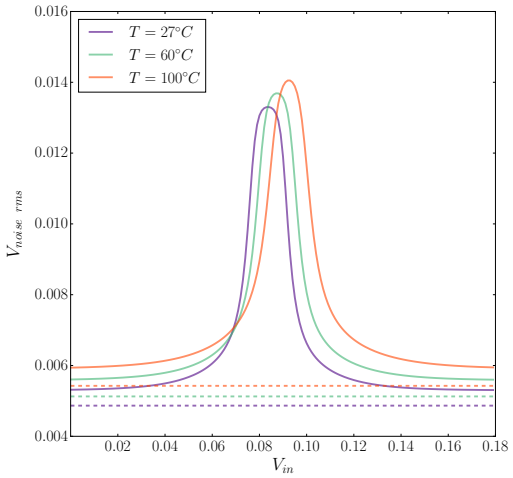


Figure 4: Standard deviation of the output noise voltage as a function of V_{in}. The dashed lines represent the theoretical minimum for thermal noise $(kT/C)^{1/2}$.

4. EXTENDING THE MODEL TO TIME DOMAIN APPLICATIONS

In Section 3, we have presented the basic concepts that allow us to study the statistical behavior of thermal noise in the time-domain. Previous works [12][8][9][10] that have been based on the same two-sided Poisson noise have used inverters or flip-flops. In all these cases, the output noise results from the contribution coming from two transistors. In this Section we first apply the results from Section 3 to a CMOS inverter and then we study how the same model can be extended to more complex gates. We have based our calculations on a 7nm FinFET predictive technology model (PTM). For all the examples show in this work, the capactive load is equivalent to drain capacitances of the first stage inverter and the gate

capacitances of the load inverter. Both inverters were sized using 2 fins for NMOS and PMOS alike. The resulting C_{out} is $149aF$ at $V_{DD} = 180mV$, hence, we assumed a total number of electrons of roughly 168 when $V_{out} = 180mV$.

Figure 3 shows the charging rate for a CMOS inverter at different temperatures. While Figure 3 shows lower rates at $V_{in} = \frac{V_{DD}}{2}$, the noise standard deviation will be the highest at this point. The actual standard deviation of the noise can be obtained combining the Poisson rates with the instantaneous time constant of the circuit as a function of the biasing point. This can be done by counting the average number of electrons in the time constant at a certain input voltage V_{in} and taking the square root of this average. Figure 4 shows the resulting noise rms voltage as a function of the input voltage V_{in}. It is important to notice how the standard deviation curves never go below the theoretical minimum thermal noise $\sqrt{kT/C}$ which would result from the classical noise analysis approach [17][22]. The curves in Figure 4 show the standard deviation of the noise in equilibrium conditions, that is, when the input and output voltage mean values match the voltage transfer curve of the inverter. These curves would depict the noise behavior when the circuit is changing state. A much more interesting situation is shown in Figures 5a and 5b. These two plots represent the case in which the input voltage is at a fixed value and the noise excursion is caused by variations of the output voltage. The asymmetry in the

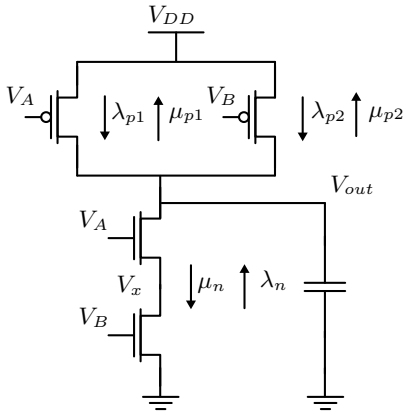


Figure 6: NAND rates. The transistor stack adds a degree of freedom in the calculation of the total noise.

plots from Figure 5a shows how the circuit reacts when it is away from its equilibrium point. For example, the plot on the left shows the case in which $V_{in} = 180mV$. The equilibrium point, where the charging and discharging rates match, is at $V_{out} = 0V$, as expected. For negative values of V_{out}, the charging rate becomes greater than the discharging rate, as the circuit wants to pull the output node back to its stable point. The same behavior appears for positive values of V_{out}, this time with the discharging rate being greater than the charging rate.

The simulation framework used for modeling the inverter can be easily scaled up to more complex multi-input gates. Figure 6 shows the configuration for a NAND gate. In our model, we assume that the total rate for either the charging or the discharging process is made up of three components (i.e., the currents from the two PMOS transistors and the current from the NMOS transistor at the top of the stack). While we do not directly consider the bottom transistor in the pull-down stack for the count of the total rate, its influence in the total noise is given by how the rates of the top

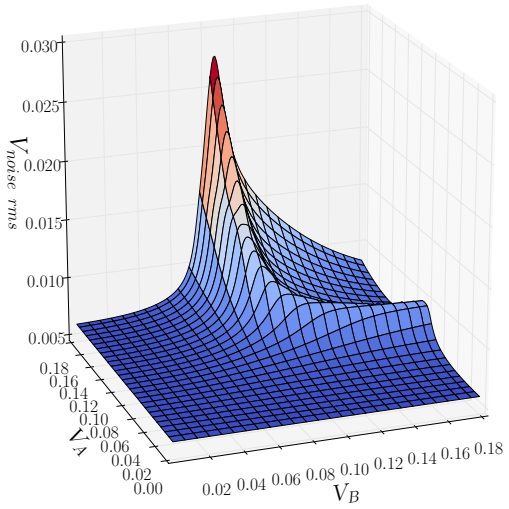
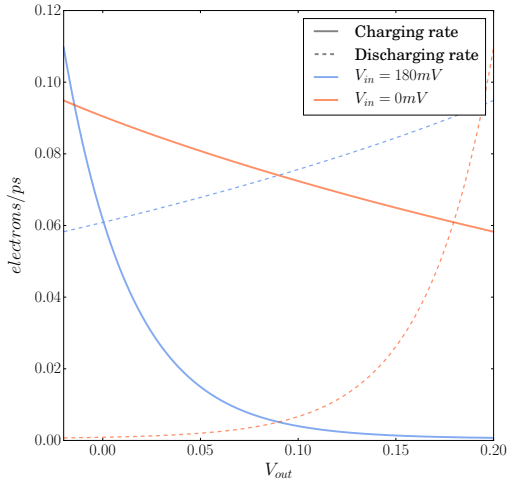


Figure 7: Standard deviation of the output noise voltage as a function of the two inputs V_A and V_B.

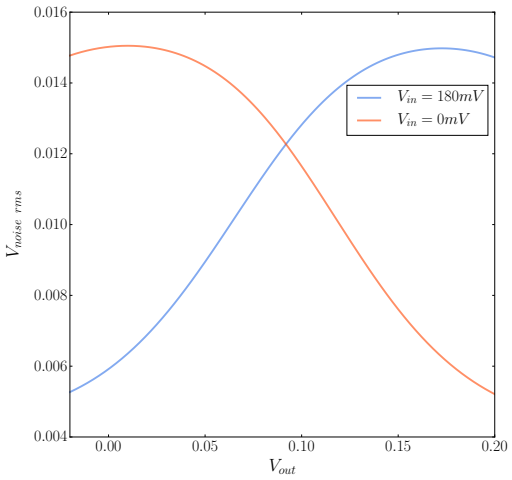
transistor are affected by the voltage V_x. This is made more clear by looking at Figure 7. When V_B is high and V_A is varying, the bottom transistor is on and the pull-down network behaves as in the case of the inverter with the rates governed by the V_A. This means that only the forward rate is affected. When V_A is high and V_B is varying, we observe a much higher peak noise. This behavior can be explained by considering that in the latter case, the rates are both controlled by the voltage V_x which varies with V_B.

5. NOISE SIMULATOR

Based on the model description from Section 4, we built our noise simulator. This model was entirely written in C ++ with the goal of being able to simulate noise time series in the range of milliseconds to seconds. The algorithm flow can be summarized as in Figure 8. Without loss of generality let us consider the case for an inverter. We start by initializing the parameters at a stable point in the transfer curve of the inverter. For the desired V_{in}, V_{out} pair, we extract the noise parameters λ_t, μ_t and τ_t. At this point we are ready to start the noise samples generation. We generate the Poisson events by counting the inter–arrival times in a period of $50ps$. This value has been chosen so that the integration time is always less than the time constant of the circuit. Since the value of the Poisson rates changes during the simulation, we need to generate the time series from a non–homogeneous Poisson process. A non–homogeneous Poisson process is defined by a time varying rate function $\lambda(t)$. The authors of [11] have shown an efficient way to generate Poisson samples having a time dependent rate function. The algorithm starts by generating Poisson samples in the interval $(0, T]$ with rate $\lambda^* \geq \lambda_t \quad \forall \quad t \in (0, T]$. Then, each sample X_i^* from the series $X_1^*, X_2^*, X_3^*, \ldots X_n^*$ is rejected with probability $1 - \lambda_i/\lambda^*$. The samples that survive this *thinning* procedure, constitute a non–homogeneous Poisson process with with rate function $\lambda(t)$. For our simulator, we generate samples at the highest rate λ_{max} and then add each event to the total count with probability λ_t/λ_{max}[4]. We get the cumulative count at each time–step by subtracting the discharging process count from the charging process count. This value is then translated into an equivalent voltage step ΔV and applied to the time series as shown in Equation 7.



(a) Charging and discharging rates.



(b) Standard deviation.

Figure 5: Rates and standard deviation of an inverter as a function of the output voltage V_{out}. For the charging and discharging rates, the equilibrium is reached when the values of the two rates are matched.

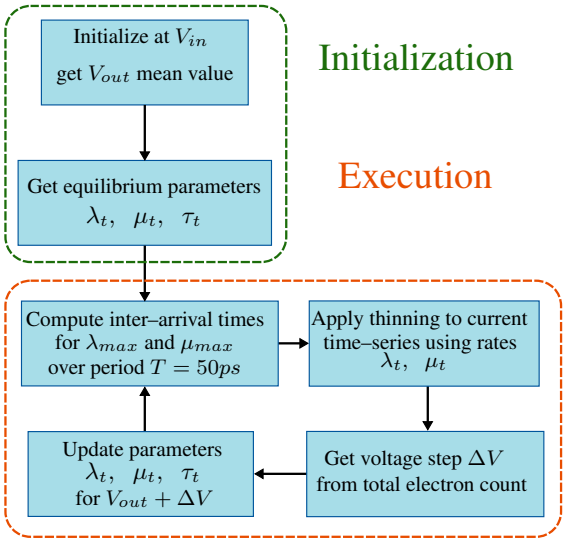


Figure 8: Algorithm flow for the noise simulator.

For each new value of the output voltage, we update the parameters λ_t, μ_t and τ_t, and we proceed to the next iteration of the loop. This last step guarantees that the new noise sample will take into account the deviation from the equilibrium condition. An important requirement of our simulator is to be able to generate long time series without incurring in any periodic pattern. We decided to use the Marsenne-Twister engine [15] which guarantees a period of 2^{19937} (well above our simulation needs). In Figure 9 we compare the accuracy of our approach against SPICE and also evaluate the importance of using the OU process in our approach. In particular, the purple traces in Figure 9 show the the voltage time series results generated from our model (*i.e.* as described in Equation 7). We compare this against the orange traces in Figure 9 which show the response of the SPICE circuit to shot–noise current pulses that were generated from the net electron count derived by our simulator. These current pulses were injected in the output node of the inverter to simulate the actual noise response of the circuit. Finally, the grey traces in Figure 8 show the time series composed of only the voltage steps $X_t q/C_{out}$ (*i.e.*, ignoring the OU process). From our results in Figure 9 we see that our approach give results in very close agreement to SPICE and the OU process is an important component to achieve accurate results. The performance can be tested on the comparison between the time needed by our noise simulator to generate $100\mu sec$ of noise samples and the time it takes for SPICE to run a full transient simulation on the same time interval. Our simulator generated the samples in $18.6sec$ while the SPICE simulation took in total 14.4 minutes, showing that simulation time can be improved by a factor of $47\times$. Moreover, our simulator takes on average a mere 4 hours to produce a 5σ event. By comparison, SPICE would have to run for almost 10 days to provide the same result. In order to take advantage of this performance improvement, we propose to use our simulator for exploratory analysis of noise transients. By running our simulator for long periods of time, we can extract noise transients from long noise time series, and use SPICE to simulate around rare noise samples in a time range of a few time constants.

6. CONCLUSIONS

In this work, we presented a framework for improving the simulation efficiency of thermal noise in the time domain, starting from the unified shot-thermal noise model. The Ornstein–Uhlenbeck process has been used to capture the correct dynamic response of the circuit while we have guaranteed the correct model behavior to varying biasing conditions using non–homogeneous Poisson processes for modeling the charging and discharging electron flows. Our model can noticeably decrease the simulation time of long thermal noise time–series allowing to capture rare events not only significantly faster than conventional SPICE simulations, but also with comparable physical accuracy. For future work we plan to use our approach as an easier method for evaluating the response of the circuit to rare thermal noise patterns. This will require enabling the simulator to analyze larger and more complex logic circuits. We note that with our current focus on thermal noise, we have not been able to directly compare our results to that of other published works such as [14] and [13] since these works promise non-Monte Carlo methods for modeling nonstationary low–frequency noise phenomena which are fundamentally different from thermal noise. However, we also plan to extend our framework to other noise sources

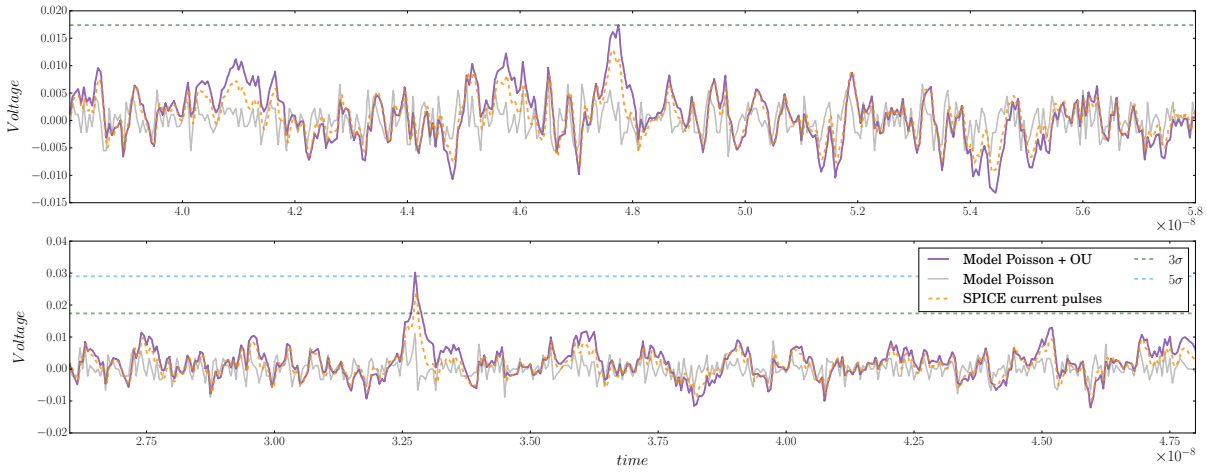


Figure 9: Comparison of the time series generated by our simulator and the SPICE transient response to the shot–noise currents. We used 3σ and 5σ thresholds for the noise events, where $\sigma = (kT/C)^{1/2}$

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such as RTS noise, providing better conditions for conducting a comparative study with other models.

7. ACKNOWLEDGEMENTS

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8. REFERENCES

[1] O. E. Barndorff-Nielsen and N. Shephard. Non–Gaussian Ornstein–Uhlenbeck-based models and some of their uses in financial economics. *J. R. Stat. Soc. B*, 63(2):167–241, 2001.

[2] E. Bibbona, G. Panfilo, and P. Tavella. The Ornstein–Uhlenbeck process as a model of a low pass filtered white noise. *Metrologia*, 45(6):S117–S126, Dec. 2008.

[3] D. Blaauw, D. Sylvester, Y. Lee, I. Y. Lee, S. Bang, I. Lee, Y. Kim, G. Kim, and H. Ghead. From digital processors to analog building blocks: Enabling new applications through ultra-low voltage design. In *SubVT 2012*.

[4] P. Bratley, B. L. Fox, and L. E. Schrage. *A Guide to Simulation*, volume 2. Springer, 1983.

[5] B. Calhoun, J. Ryan, S. Khanna, M. Putic, and J. Lach. Flexible Circuits and Architectures for Ultralow Power. *Proc. IEEE*, 98(2):267–282, Feb. 2010.

[6] D. T. Gillespie. Exact numerical simulation of the Ornstein-Uhlenbeck process and its integral. *Phys. Rev. E*, 54(2):2084–2091, 1996.

[7] K. Itô. *Stochastic Processes: Lectures Given at Aarhus University*. Springer, 2004.

[8] P. Jannaty, F. Sabou, R. Bahar, J. Mundy, W. Patterson, and A. Zaslavsky. Full two-dimensional markov chain analysis of thermal soft errors in subthreshold nanoscale cmos devices. *IEEE Trans. Device Mater. Rel.*, 11(1):50–59, March 2011.

[9] P. Jannaty, F. C. Sabou, S. T. Le, M. Donato, R. I. Bahar, W. Patterson, J. Mundy, and A. Zaslavsky. Shot-Noise-Induced Failure in Nanoscale Flip-Flops Part I: Numerical Framework. *IEEE Trans. Electron Devices*, 59(3):800–806, Mar. 2012.

[10] P. Jannaty, F. C. Sabou, S. T. Le, M. Donato, R. I. Bahar, W. Patterson, J. Mundy, and A. Zaslavsky. Shot-Noise-Induced Failure in Nanoscale Flip-Flops Part II: Failure Rates in 10-nm Ultimate CMOS. *IEEE Trans. Electron Devices*, 59(3):807–812, Mar. 2012.

[11] P. A. Lewis and G. S. Shedler. Simulation of nonhomogeneous poisson processes by thinning. *Nav. Res. Logist. Q.*, 26(3):403–413, 1979.

[12] H. Li, J. Mundy, W. Patterson, D. Kazazis, A. Zaslavsky, and R. I. Bahar. Thermally-induced soft errors in nanoscale CMOS circuits. In *NANOARCH*, pages 62–69, Oct. 2007.

[13] A. G. Mahmutoglu and A. Demir. Modeling and Analysis of Nonstationary Low-frequency Noise in Circuit Simulators: Enabling Non Monte Carlo Techniques. In *ICCAD 2014*.

[14] A. G. Mahmutoglu, A. Demir, and J. Roychowdhury. Modeling and analysis of (nonstationary) low frequency noise in nano devices: A synergistic approach based on stochastic chemical kinetics. In *ICCAD 2013*.

[15] M. Matsumoto and T. Nishimura. Mersenne twister: A 623-dimensionally equidistributed uniform pseudo-random number generator. *ACM Trans. Model. Comput. Simul.*, 8(1):3–30, Jan. 1998.

[16] N. Paydavosi, S. Venugopalan, Y. Chauhan, J. Duarte, S. Jandhyala, A. Niknejad, and C. Hu. BSIM–SPICE Models Enable FinFET and UTB IC Designs. *Access, IEEE*, 1:201–215, 2013.

[17] R. Sarpeshkar, T. Delbruck, and C. Mead. White noise in MOS transistors and resistors. *IEEE Circuits Devices Mag.*, 9(6):23–29, 1993.

[18] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao. Exploring sub-20nm FinFET design with Predictive Technology Models. In *DAC 2012*, pages 283–288.

[19] P. L. Smith. From Poisson shot noise to the integrated Ornstein–Uhlenbeck process: Neurally principled models of information accumulation in decision-making and response time. *J. Math. Psychol.*, 54(2):266–283, Apr. 2010.

[20] Y. Taur and T. H. Ning. *Fundamentals of Modern VLSI Devices*. Cambridge University Press, Cambridge, UK, 2013.

[21] G. Uhlenbeck and L. Ornstein. On the Theory of the Brownian Motion. *Phys. Rev.*, 36(5):823–841, Sept. 1930.

[22] A. Van der Ziel. *Noise in Solid State Devices and Circuits*. Wiley-Interscience, 1986.