CMOS-Compatible FDSOI Bipolar-Enhanced Tunneling FET

Peng Zhang[1], J. Wan[2], A. Zaslavsky,[1] and S. Cristoloveanu[2]
[1]Department of Physics and School of Engineering, Brown University, Providence, RI 02912, USA
[2]IMEP-LAHC, INP-Grenoble/Minatec, BP 257, Grenoble 38016, France

***Abstract*—We propose and simulate a bipolar-enhanced tunneling field-effect transistor (BET-FET) with a lateral layout that is fully FDSOI compatible. Simulations calibrated to experimental TFET data show a high on-current of I_{ON} ~ 260 µA/µm at V_{DD} = 1 V and a subthreshold swing (SS) well below 60 mV/dec over 7 decades of drain current. The mechanism involves the combination of gate-controlled sharp TFET switching with current gain from a $Si/Si_{1-x}Ge_x$ heterojunction bipolar transistor (HBT). An electrostatically controlled BET-FET variant with a local buried gate is also simulated.**

Keywords—bipolar-enhanced tunneling field-effect transistor; tunneling field-effect transistor; FDSOI; sharp switching.

I. INTRODUCTION

The unscalability of MOSFET subthreshold swing (SS) of 60 mV/dec at room temperature prevents us from dowscaling the supply voltage V_{DD} without degrading the I_{ON}/I_{OFF} ratio. The tunneling field-effect transistor (TFET), because of its band-to-band tunneling (BTBT) mechanism, is free from this limit and has therefore attracted much interest in recent years [1]–[5]. However, most of the experimental results published so far suffer from a low I_{ON}, and the small SS is only obtained over a narrow range of drain current. In the record Si-based TFET reported recently, with I_{ON} of 112 µA/µm at drain voltage V_D = –1 V and gate voltage V_G = –1.5 V, the SS was only 150 mV/dec [5].

Alternatives to the inadequate I_{ON} and SS have included TFETs based on different material systems (Si-III-V or all III-V junctions) [6]–[10], but the experimental structures have not been CMOS-compatible to date. Another promising approach is the bipolar-enhanced TFET (BET-FET) [11]–[12], where the BTBT current is amplified by the bipolar gain in a monolithic structure. Unlike the previously published BET-FETs with complex sidewall gates [11] and vertical current flow [11], [12], here we propose and simulate a simpler lateral structure that is compatible with FDSOI fabrication process [13], [14]. The BET-FET monolithically integrates a *p*-mode TFET with a $Si_{1-x}Ge_x$ layer to increase the BTBT rate as in [5], with a lateral $Si/Si_{1-x}Ge_x$ heterojunction bipolar transistor (HBT). The gate-controlled tunneling current acts as the base current of the HBT and triggers a high electron injection from the Si drain. The simulated device shows both low SS over a large current range and high I_{ON}, easily outperforming a conventional TFET with a similar lateral layout. Finally, a back-gated variant where electrostatic control replaces based oping is also investigated.

II. STRUCTURE AND SIMULATION RESULTS

Two-dimensional (2D) TCAD simulation was performed using Synopsys Sentaurus [15]. Figure 1(a) illustrates the simplest structure of an all-Si BET-FET that maps nicely on previously fabricated FDSOI ESD device process [13]. The device is built on an SOI structure with a 21 nm thick Si active layer and 25 nm buried oxide (BOX). The intrinsic section was covered by a HfO_2/metal gate stack with EOT of 1 nm and a metal workfunction of 5.2 eV. The doping of *n*-type emitter (drain) and collector (source) was set to 10^{20} cm^{-3}, with a Gaussian decay into the channel with a diffusion length of 2 nm. The base was *p*-doped at 3–4×10^{18} cm^{-3} with the same Gaussian decay profile on both sides. The resulting transistor was negatively biased at the emitter (drain), V_D < 0, with the collector (source) grounded. During the simulation, V_G was swept from zero to negative values.

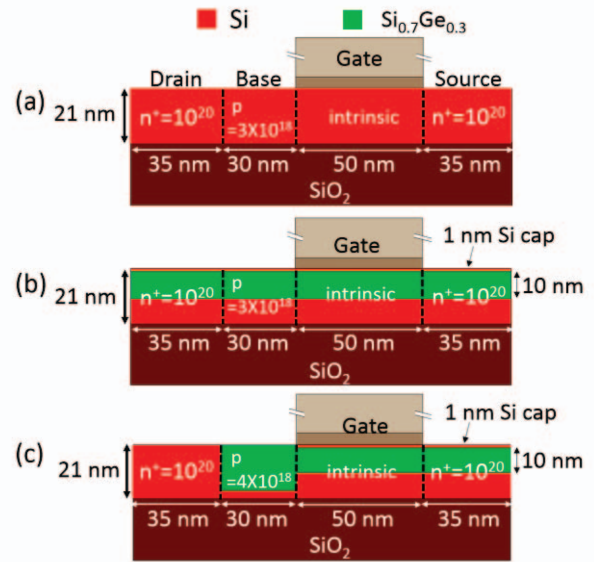

Fig. 1. Schematic view of the simulated structures: (a) all Si, (b) with an inserted planar 10 nm $Si_{0.7}Ge_{0.3}$ layer, and (c) with a 10 nm $Si_{0.7}Ge_{0.3}$ layer and $Si_{0.7}Ge_{0.3}$ base on top of a 3 nm Si pedestal. The black dashed lines indicate the boundaries of different sections.

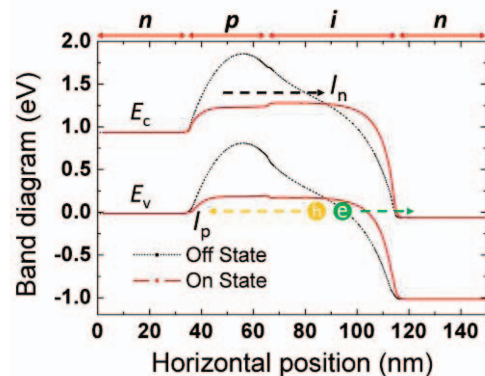

Fig. 2. Band diagram along the device in the ON (solid line) and OFF (dotted line) states. Arrows indicate electron and hole currents in the ON state.

978-1-5090-0259-7/15/$31.00 ©2015 IEEE

The operating principle of the BET-FET is illustrated in Fig. 2. When $V_G = 0$, the device is in the OFF state, with a large tunneling tunneling barrier (dotted line in Fig. 2) in the reverse-biased base-collector junction. The tunneling current is suppressed and there is only negligible current flow from the emitter to the collector. In the ON state, when $V_G = -1$ V, the tunneling gap becomes very small (solid line in Fig. 2). The BTBT base-collector tunneling current results in holes (I_p) flowing to the emitter, forward-biasing the emitter-base junction, and trigger a high injected electron current (I_n) injection from the emitter to the collector – see Fig. 2. So the hole current acts as the base current of a conventional bipolar transistor and is multiplied by the emitter-base gain β. Note that a $Si_{1-x}Ge_x$ can be inserted in the base section (as discussed later) to form a true HBT and thus improving the bipolar gain.

For the simulation, the dynamic nonlocal tunneling model for BTBT was used [15]. Figure 3(a) shows the I_D–V_G transfer curve at $V_D = -1.0$ V. For comparison, a conventional TFET with the same structure as in Fig. 1(a), but with the emitter doping changed to p^+-Si, was also simulated. As can be seen, the all-Si BET-FET enjoys limited current gain β < 20 with respect to that of TFET, so it still suffers from a relatively low I_{ON}.

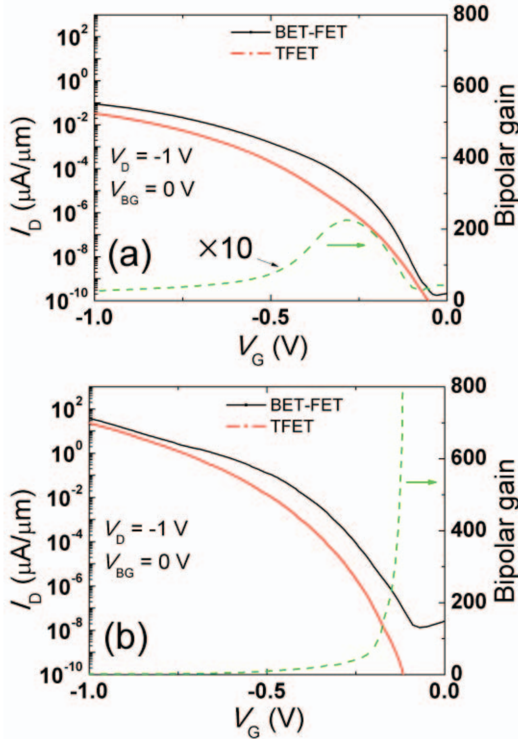

Fig. 3. (a) Comparison of current between all-Si BET-FET and a conventional TFET using the structure in Fig. 1(a). The green dashed line shows the bipolar current gain referenced to the TFET; (b) same as (a) but using the structure in Fig. 1(b) with a $Si_{0.7}Ge_{0.3}$ layer in the channel.

To improve the I_{ON}, a $Si_{0.7}Ge_{0.3}$ layer can be inserted in the channel, as shown in Fig. 1(b), which will effectively increase the BTBT rate due to smaller SiGe bandgap [5]. Note that the tunneling reduced mass m_r for SiGe, which is a fitting parameter for BTBT model, was modified from its default value to $0.4m_0$, to fit the experimental TFET data reported in [5] for a similar planar layout. The simulation results are shown in Fig. 3(b) and compared to the standard TFET. The I_{ON} improves by more than two orders of magnitude. The β also increases, but it blows up near $V_G = 0$ V due to high I_{OFF}. Furthermore, β decreases at high I_D, so the BET-FET advantage is lost as V_G approaches –1 V.

The performance of the BET-FET can be further optimized by using a true HBT. Figure 1(c) shows the final layout, where the heavily-doped $Si_{0.7}Ge_{0.3}$ base is grown on top of a thin 3 nm Si layer (a step analogous to selective SiGe raised S/D regrowth). As shown in Fig. 4(a), now the BET-FET exhibits a much higher I_{ON} of ~260 μA/μm at $V_G = V_D = -1.0$ V. The bipolar gain β peaks at 620 at $V_G = -0.4$ V.

The sharp-switching character of the BET-FET over a wide current range is confirmed in Fig. 5, showing SS < 60 mV/dec over seven decades of drain current in the BET-FET, as compared to ~3 decades in the TFET.

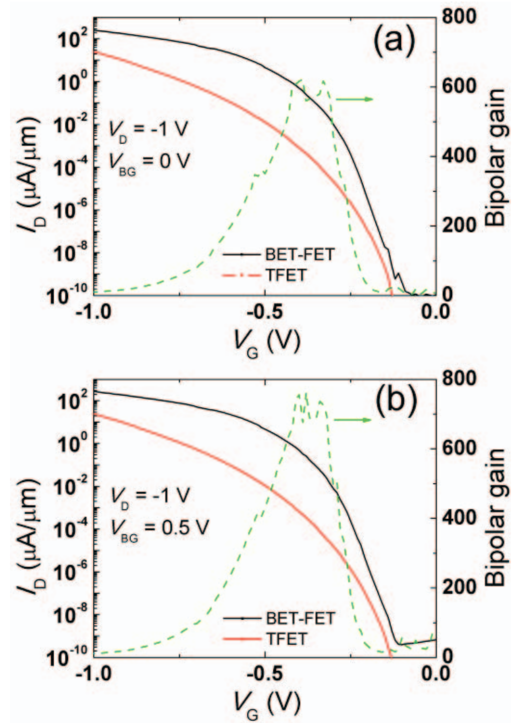

Fig. 4. (a) Comparison of current between BET-FET and a conventional TFET using the structure in Fig. 1(c). The green dashed line shows the bipolar current gain referenced to the TFET; (b) same structure but with back gate voltage $V_{BG} = 0.5$ V.

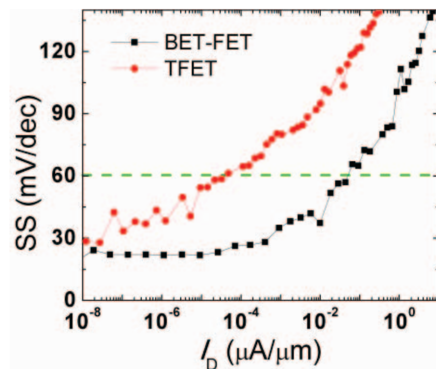

Fig. 5. SS *vs.* I_D for the BET-FET and a conventional TFET. The BET-FET shows small SS, well below 60 mV/dec, over a much larger I_D range.

The lateral FDSOI layout also makes it possible to apply a back gate voltage V_{BG} to the entire structure. A positive voltage attracts electrons to the channel/BOX interface and thus increases the electron current. This is verified in Fig. 4(b), where $V_{BG} = 0.5$ V was applied. Compared to Fig. 4(a), the I_{ON} and current gain improve slightly due to the higher electron current; the current gain β also increases, reaching 750 at $V_G = -0.4$ V Such low V_{BG} can be achieved via pocket implantation of dopants under the base, as was done in [13] for ESD devices based on a device layout analogous to Fig. 1(a). Higher $V_{BG} = 1.0$ V provide additional, albeit slight, enhancement of I_{ON}.

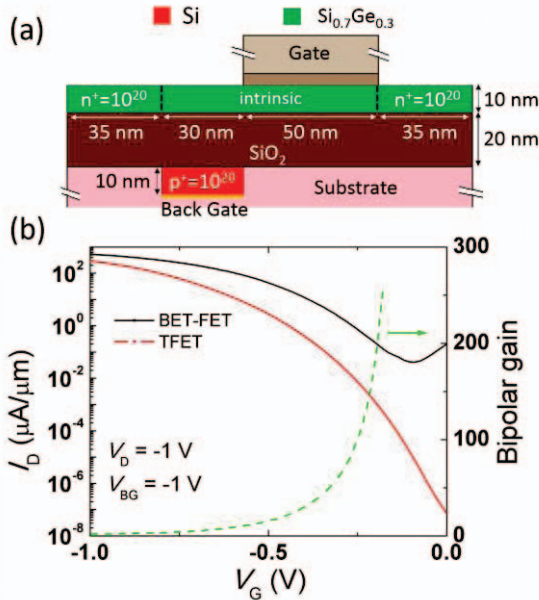

Fig. 6. (a) Schematic view of the simulated n^+-i-n^+ all $Si_{0.7}Ge_{0.3}$ structure; (b) comparison of current between all- $Si_{0.7}Ge_{0.3}$ BET-FET and a conventional TFET using the structure in (a).

Another alternative structure for the BET-FET is shown in Fig. 6(a). Instead of n^+-p-i-n^+ as shown before, here we use an all-$Si_{0.7}Ge_{0.3}$ n^+-i-n^+ structure with a buried local back-gate instead of a p-doped base region. The undoped channel (p-type, with $N_A = 10^{15}$ cm^{-3}) was only partially covered by the front gate. The uncovered area was controlled by a back gate voltage right below the buried oxide (t_{BOX} = 20 nm for the 14 nm technology node [13]), which would create a "virtual" p-doped region. In order for the back gate to have a good control over the virtual p-doped region, the body of the $Si_{0.7}Ge_{0.3}$ was made to be 10 nm. Such a UTBB (ultra-thin body and box) device is achievable, as was done in [13].

Figure 6(b) shows the transfer curve at $V_D = -1.0$ V and $V_{BG} = -1.0$ V. A similar behavior as Fig. 3 and Fig. 4 was obtained, with a I_{ON} of ~520 μA/μm at $V_G = -1.0$ V and bipolar gain β ranging from ~10–200. However, the locally backgated device suffers from a high OFF current. This is because when V_G decreases to zero, the device begins to conduct like an NMOS transistor: the local $V_{BG} = -1$ V is not enough to prevent large electron current through the channel. This problem could be overcome by going a thinner t_{BOX}.

III. Conclusion

We propose and simulate a bipolar-enhanced TFET with high I_{ON} of ~260 μA/μm and a subthreshold swing well below 60 mV/dec over seven decades of drain current for $|V_G| = |V_D| = 1$ V. We explain it by the sharp switching character of the TFET and high current gain of the HBT with which it is monolithically integrated. Unlike previously proposed BET-FETs, the lateral structure is compatible with the modern FDSOI process flow. A locally back-gated variant without p-doping in the channel delivers even higher I_{ON}, but at the cost of a higher I_{OFF}.

IV. Acknowledgments

The work at Brown University was supported by the National Science Foundation, awards ECCS-1068895 and DMR-1203186. We acknowledge a discussion with P. Galy.

References

[1] A. C. Seabaugh and Q. Zhang, Proc. IEEE, vol 98, no. 12, pp. 2095–2110, 2010.
[2] C. Aydin et al., Appl. Phys. Lett., vol. 84, pp. 1780–1782, 2004.
[3] W. Y. Choi, B.-G. Park, J.-D. Lee, and T.-J. K. Liu, IEEE Electron Device Lett., vol. 28, pp. 743 – 745, 2007.
[4] A. M. Ionescu and H. Riel, Nature, vol. 479, no. 7373, pp. 329–337, 2011.
[5] A. Villalon et al., IEEE Trans. Electron Devices, vol. 60, no. 12, pp. 4079–4084, 2013.
[6] K. Tomioka, M. Yoshimura, and T. Fukui, in VLSI Symp., 2012, pp. 47–48.
[7] U. E. Avci and I. A. Young, in Tech. Dig. IEDM, 2013, pp. 4.3.1–4.3.4.
[8] R. Bijesh et al., in Tech. Dig. IEDM, 2013, pp. 28.2.1–28.2.4.
[9] A. S. Verhulst et al., in Tech. Dig. IEDM, 2014, pp. 717–720.
[10] D. Cutaia et al., in Proc. EUROSOI-ULIS, 2015, pp. 61–64.
[11] J. Wan, A. Zaslavsky, C. Le Royer, S. Cristoloveanu, IEEE Electron Device Lett., vol. 34, pp. 24–26, 2013.
[12] A. Zaslavsky et al., ECS Trans., vol. 53, pp. 63–74, 2013.
[13] Y. Solaro et al., in Tech. Dig. IEDM, 2013, pp. 180–183.
[14] Y. Solaro et al., Solid State Electron., vol. 97, pp. 23–29, 2014.
[15] Synopsis Sentaurus TCAD ver. H-2013.03 using nonlocal band-to-band tunneling model.