A Novel Photodetector Based on the Interface Coupling Effect in Silicon-on-Insulator MOSFETs

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***Abstract*—We report a novel CMOS-compatible photodetector with record responsivity built on a silicon-on-insulator (SOI) substrate. The operating mechanism is based on the interface coupling effect in the SOI MOSFET, as confirmed by both TCAD simulations and experimental measurements on a prototype device fabricated using a simplified process flow.**

I. INTRODUCTION

Photodetectors based on the silicon-on-insulator (SOI) substrate are fully compatible with SOI waveguides and photonic devices and thus can play an important role in electric-photonic integrated systems (EPICs) [1]. Besides, thanks to the inherent advantages of SOI CMOS circuits, such as low power consumption, RF operation and radiation hardness, SOI-based photodetectors can find many applications in space navigation and low-power imaging systems. The top silicon thickness in modern SOI CMOS is typically less than 100 nm in order to reduce short-channel effects (SCEs) and achieve aggressive scaling. The thin silicon layer leads to poor quantum efficiency and extremely low responsivity in conventional SOI photodiodes (0.0075 A/W as reported in [2]). Thus, photodetectors with internal gain have been studied extensively, such as the bipolar junction transistors [3], junction field effect transistors (JFETs) [1, 4], MOSFETs and gate-body tied MOSFETs [5-7], which can achieve a remarkable responsivity as high as 2×10^4 A/W. However, many of these devices are built on sapphire substrates to reduce optical losses, which increases production cost and impacts CMOS integration [6, 7]. Recently, a photodetector has been demonstrated with excellent response and compatibility with the FD-SOI process [8, 9]. The detector uses a *p-n* photodiode embedded in the substrate to accumulate photogenerated electrons and thereby modulate the threshold voltage of a MOSFET.

In this work, we propose and demonstrate a novel interface-coupled photodetector (ICPD) built on an SOI substrate. Unlike the aforementioned devices, the ICPD utilizes the interface coupling effect that is stronger in thinner SOI [10-12]. TCAD simulations in Synopsys Sentaurus are performed to study its operating mechanism and benchmark its photoelectric response. A simplified process flow is developed to fabricate the device. Photoelectric characterization of fabricated unoptimized IPCDs agrees with simulations and shows a record responsivity of 3.3×10^4 A/W. The extremely high responsivity makes the device attractive for large-scale arrays, where the device area is restricted.

II. TCAD SIMULATION

Figure 1(a) shows the schematic view of the ICPD. The device is similar to a MOSFET except for the large ungated regions between the gate and source/drain electrodes. This is helpful to enhance the photoresponsivity and response speed. The holes induced by the back gate ($V_{BG} < 0$) accumulate at the channel/BOX interface (back interface), forming a conductive path from source to drain. The hole concentration at the back interface is affected by the front gate voltage (V_G) through interface coupling effect [10, 12]. The gating of the back interface by V_G is screened by the photo-induced electron concentration at the front gate-oxide interface. Figure 1(b) compares the I_D-V_G curves and electron concentration (at 1 nm below the front gate oxide) in the dark and under steady-state illumination (50 μW/cm^2 at 520 nm). As V_G increases, the electric field formed by the $V_G > 0$ draws the light-generated electrons to the front interface, screening the coupling of front gate to the back channel and leading to higher back channel current. The simulated photoresponsivity of the ICPD sensor is as high as 5.5×10^4 A/W due to the high internal gain.

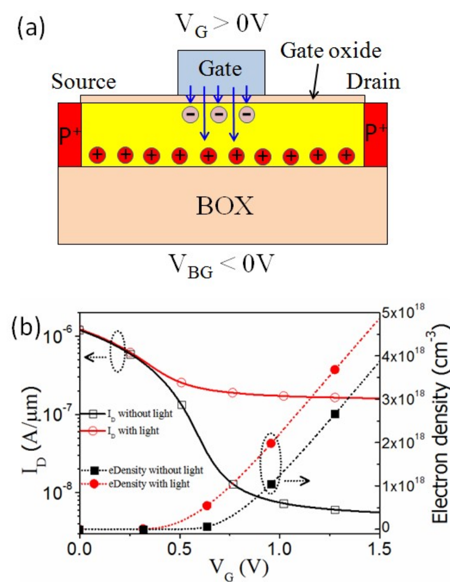

Fig. 1. Schematic of the simulated ICPD with L_G = 1 μm gate length, 2 μm gaps, 200 nm top silicon film and 500 nm BOX. (b) Simulation results comparing the evolution of drain current (I_D) and electron concentration *vs.* V_G in the dark and under illumination (light source at 520 nm wavelength with 50 μW/cm^2 intensity).

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The operation of the device is also similar to that of a p-type JFET. The electron layer induced by V_G at the top interface functions as the JFET gate controlling the bottom channel induced by V_{BG}. The light-generated electrons accumulating at the top interface reduce the potential of the field-induced JFET's gate, see the comparison between Fig. 2(a) and (b). This is similar as applying a negative bias on the gate of the JFET, which increases the hole current at the bottom channel, see Fig. 2.

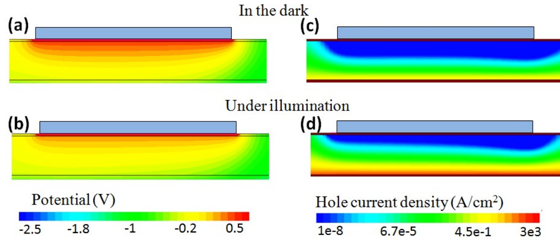

Fig. 2. Distribution of channel potential under the front gate in the dark (a) and under illumination (b), and their corresponding hole current density (c), (d). The device is under $V_G = 1.5$ V, $V_{BG} = -6$ V and $V_D = -1$ V.

Figure 3(a) compares the transient response of devices with various L_G and a fixed $L_{TOT} = 5$ µm to a light pulse, which reveals the benefit of inserting ungated regions around L_G. For the device with gate covering most of the channel ($L_G = 4$ µm), the photoresponse is low and slow. Reducing L_G from 4 to 1 µm increases the photoresponse by a factor of nearly 3 and reduces the response time dramatically. Figure 3(b) summarizes the impact of L_G on the responsivity and rise/fall time. Reducing L_G increases the transconductance of the MOSFET and thus improves the photoresponsivity, although too small an L_G induces short channel effects and thereby degrades the responsivity. Shorter gate length also leads to smaller gate capacitance and thus reduces the charging and discharging times.

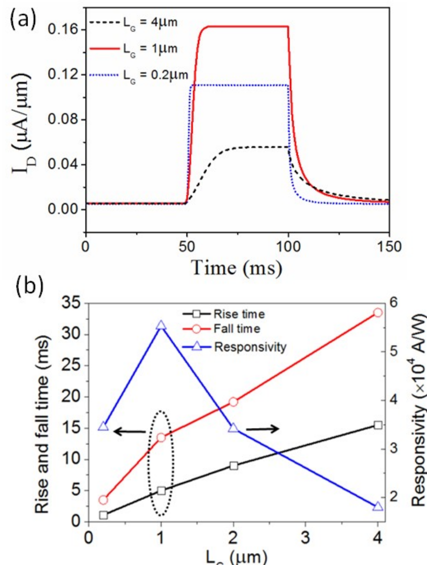

Fig. 3. (a) Transient response of devices with various L_G to a 50 ms light pulse with intensity of 50 µW/cm^2. Note that the V_{BG} of each device is adjusted to have the same dark current. (b) The relation between L_G and ICPD performances.

Unlike other SOI-based photodetectors, where thinning down the top silicon layer typically leads to low quantum efficiency and reduces the photoresponse, the ICPD shows the opposite trend, see Fig. 4(a). As the top silicon layer (T_{si}) is reduced from 300 to 100 nm, the photoresponsivity increases dramatically thanks to stronger interface coupling in devices with thinner T_{si}, albeit with slower response due to lower light-generated electron current, as summarized in Fig. 4(b). However, for devices with ultra-thin T_{si} = 20 nm, the photoresponsivity degrades due to strong recombination between top electron and bottom hole layers.

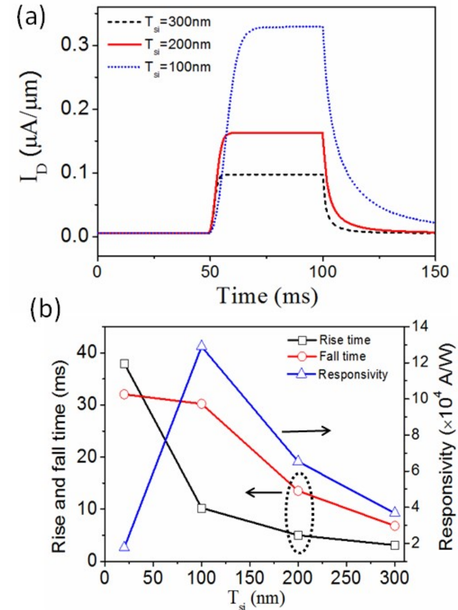

Fig. 4. (a) Transient response of devices with various T_{si} to a 50 ms light pulse with intensity of 50 µW/cm^2. Note that the V_{BG} of each device is adjusted to have the same dark current. (b) The relation between T_{si} and ICPD performances.

III. EXPERIMENTAL RESULTS

The device shown in Fig. 5 was fabricated with a simplified structure and process flow. After formation of mesa isolation by lithography and wet etching in TMAH, aluminum (Al) is deposited directly on source/drain to form Schottky contacts to undoped source/drain regions. Then, a 30 nm Al_2O_3 gate oxide is deposited by atomic layer deposition. Due to the availability of material in our lab, 150 nm Al is used as the gate electrode (instead of a transparent gate material like ITO, which can achieve better performance). The structure is finally annealed at 500 ^oC for 30 minutes in nitrogen. This simplified process requires neither S/D implantation nor high-temperature annealing, and thus has good compatibility with novel materials, such as organic or 2D atomically thin semiconductors. Electrical characterization on the fabricated device is shown in Fig. 6(a). The I_D-V_{BG} of the reference device without a front gate exhibits *p*-type characteristics due to the low Schottky barrier height between Al and the valence band of Si [13]. Further, it shows a relatively low photoresponsivity (< 0.4 A/W).

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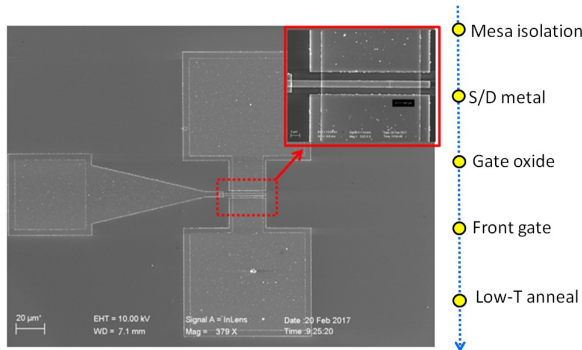

Fig. 5. Top-view SEM image of the fabricated device and a simplified process flow.

The measurement on the fabricated ICPD in Fig. 6(b) shows much improved photoresponse and the V_{BG} can be used to tune the compromise between photoresponsivity and dark current. The responsivity obtained in the experiment is estimated as 3.3×10^4 A/W at $V_G = 1.5$ V and $V_{BG} = -6$ V.

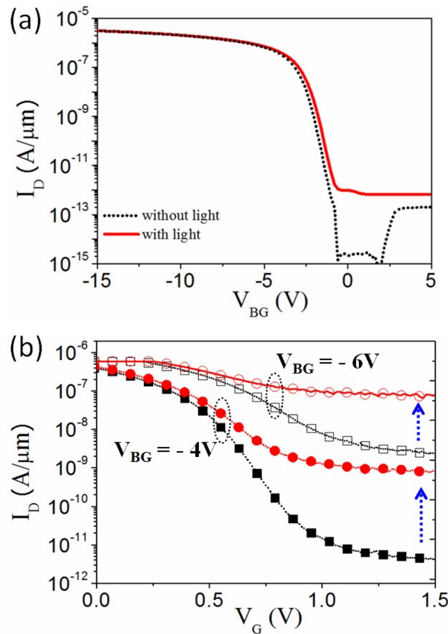

Fig. 6. (a) I_D-V_{BG} characteristics of the fabricated prototype device without a front gate in the dark dark and under illumination. (b) Measurement of the fabricated ICPD at two V_{BG} values, showing improved photoresponse similar to the simulation results.

IV. Conclusions

In this paper, we have reported a novel photodetector built on an SOI substrate. The device utilizes the interface coupling effect and shows extremely high responsivitivty. A simplified fabrication flow is developed for a proof-of-concept prototype device structure. Experimental photoelectric measurements shows responsivity as high as 3.3×10^4 A/W, a record value for a CMOS-compatible SOI photodetector despite an unoptimized fabrication process.

Acknowledgments

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