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Channel scaling and field-effect mobility extraction in amorphous InZnO thin film transistors

Sunghwan Lee [a,*], Yang Song [b], Hongsik Park [d], A. Zaslavsky [b,c], D.C. Paine [c]

[a] Department of Mechanical Engineering, Baylor University, Waco, TX 76798, USA
[b] Department of Physics, Brown University, Providence, RI 02912, USA
[c] School of Engineering, Brown University, Providence, RI 02912, USA
[d] School of Electronics Engineering, Kyungpook National University, Daegu 702-701, Republic of Korea

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ABSTRACT

Amorphous oxide semiconductors (AOSs) based on indium oxides are of great interest for next generation ultra-high definition displays that require much smaller pixel driving elements. We describe the scaling behavior in amorphous InZnO thin film transistors (TFTs) with a significant decrease in the extracted field-effect mobility μ_{FE} with channel length L (from 39.3 to 9.9 $cm^2/V{\cdot}s$ as L is reduced from 50 to 5 μm). Transmission line model measurements reveal that channel scaling leads to a significant μ_{FE} underestimation due to contact resistance (R_C) at the metallization/channel interface. Therefore, we suggest a method of extracting correct μ_{FE} when the TFT performance is significantly affected by R_C. The corrected μ_{FE} values are higher (45.4 $cm^2/V{\cdot}s$) and nearly independent of L. The results show the critical effect of contact resistance on μ_{FE} measurements and suggest strategies to determine accurate μ_{FE} when a TFT channel is scaled.

1. Introduction

Amorphous oxide semiconductors (AOSs) based on In_2O_3 are technologically promising due to high carrier mobility [1–3] and excellent optical transmittance [1] in the visible. Therefore, AOS materials have been integrated as active layers [2,4] and electrodes [2,5,6] into a variety of electronic devices, such as high performance thin film transistors [2,7] (TFTs) and fast photodetectors [8,9]. This class of materials has been gaining particular attention in next generation displays due to their much higher TFT field effect mobility μ_{FE} (>10 $cm^2/V{\cdot}s$ *vs.* 1 $cm^2/V{\cdot}s$) [1–3] and low temperature (T) processability (RT–100 °C *vs.* ~300 °C) [1–4] compared to conventional amorphous Si (a-Si)-based TFTs. Additional advantages of AOSs include isotropic wet etch characteristics [7] and compatibility with mass production [10], all of which make this material suitable for large area, flexible, and transparent devices on inexpensive polymer substrates [11].

To date, many researchers have extensively contributed to the development of high-performance and stable AOS TFTs. These efforts include studies of thermal [12] and bias stress [13,14] stability, the elucidation of doping mechanisms [15,16], threshold voltage stability [12–14,17], the investigation/improvement of channel/metallization contact properties [2,18,19], and amorphous phase stability [12,20]. Therefore, some AOS materials such as InGaZnO (IGZO) are now being deployed in high performance and flexible active-matrix liquid crystal displays and active-matrix organic light emitting diode technologies [10]. Compared to industrialized IGZO TFTs, IZO TFTs have shown markedly higher field-effect mobility [4,12], making them promising for high-current devices in future technologies.

An important future technological challenge is the downscaling of AOS TFTs for ultra-high definition (UHD) displays. Since these next-generation technologies utilize much smaller pixel sizes for UHD resolution, AOS TFTs employed as pixel driving elements must be scaled down as well. When the dimensions of TFT devices (e.g., channel length L and width W) are reduced, important device characteristics such as the field-effect mobility μ_{FE}, threshold voltage V_T, and device saturation behavior are expected to be affected by scaling, like conventional metal-oxidesemiconductor field effect transistor (MOSFET) devices. Previous studies by Jeong et al. [21] and Barquinha et al. [22] reported that the field-effect mobility of sputter-processed amorphous IGZO TFTs decreased from ~10 $cm^2/V{\cdot}s$ to 3.5 $cm^2/V{\cdot}s$ (IZO source/drain or S/D) and

* Corresponding author.
E-mail address: Sunghwan_Lee@baylor.edu (S. Lee).

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~24 cm^2/V·s to 10 cm^2/V·s (IZO, Ti/Mo S/D) as channel length L was downscaled. They attributed these μ_{FE} decreases to the effect of increasing parasitic resistance. Hu et al. [23] found a similar behavior in solution-processed ZnSnO TFTs, where μ_{FE} decreased from 8 to 6 cm^2/V·s (Mo S/D) and from 6 to 1 cm^2/V·s (Ti/Au S/D) as L was scaled down from 300 μm to 3 μm, again attributing the decrease in μ_{FE} to contact resistance. In the reports by Jeong [21] and Barquinha [22], the difference between Mo and Ti/Au metallized devices was attributed to the formation of TiO_2 in the Ti/Au S/D case. These reports are in basic agreement with our previous study [12] that suggested metallization strategies for AOS-based TFTs to ensure low contact resistance. However, while the previous reports [21–23] described the channel scaling-induced μ_{FE} reduction, a method to correctly evaluate μ_{FE} in downscaled AOS-based TFTs was not provided.

In this study, we report on the effect of channel downscaling in amorphous InZnO (a-IZO) TFTs on the device performance. Backgated devices with various L and W were fabricated, and the output and transfer characteristics were compared as a function of L. We have found that the extracted μ_{FE} decreases strongly with L: from 39.3 cm^2/V·s (L = 50 μm) to 9.9 cm^2/V·s (L = 5 μm), while the threshold voltage V_T became more negative in small L devices and, furthermore, smaller devices required a larger drain bias V_D to achieve drain current saturation and show higher off-state currents. Transmission line model (TLM) measurements and a modified extraction procedure were used to evaluate the effect of contact resistance at the channel/metallization interface and its subsequent impact on the extraction of μ_{FE} in a-IZO TFTs with channel scaling.

2. Experimental details

In our a-IZO TFTs, the channel, source/drain (S/D), and gate contact electrodes were deposited at room temperature using dc magnetron sputtering with a target-to-substrate distance of 10 cm. Before all depositions, the sputter chamber was pumped down to a base pressure lower than 6×10^{-6} Torr and the target was presputtered for 1000 s to remove surface contamination and to ensure homogeneous distribution of process gas in the sputter chamber. To investigate the channel IZO and the channel scaling behavior without the added complications due to the processing of gate dielectric layers, a bottom-gated device structure was used. We note that top-gated devices with near-zero threshold voltage using the same IZO channel material were reported by Song and co-workers previously [24]. The a-IZO TFTs were fabricated on heavily-doped single-crystal n-Si substrates (0.003–0.005 Ω cm) covered with a 50 nm thermally grown SiO_2 layer that was used as gate dielectric. The 10 nm thick channel IZO films were sputtered from a commercially available 90 wt% In_2O_3-10 wt% ZnO target (Idemitsu Corp., Japan) using a dc power density of 0.22 W/cm^2 at 280 V with deposition rates of ~0.035 nm/s, a chamber pressure of 2 mTorr, and an Ar/O_2 gas volume fraction of 86/14. For S/D contact pads (100 × 100 μm) Mo metal films (~100 nm) were deposited at 0.88 W/cm^2 at 350 V at a deposition rate of 0.09 nm/s. The channel and S/D regions were defined using a conventional photolithography and a lift-off with positive photo-resist (S-1818) and negative photo-resist (AZ-5214), respectively. The back side of the wafer was wet-etched with buffered HF to remove any oxides and then a Mo contact metallization was sputter-deposited at the same condition as for the S/D electrode metallization. Transistor transfer and output characteristics were measured using an Agilent 4155C semiconductor parameter analyzer in a light-tight probe station. To minimize the effect of photoconductivity in the IZO channel, the device performance was evaluated after resting at least 10 min in the light-tight probe station.

3. Results and discussion

The drain current–voltage (I_D-V_D) output characteristics were measured by sweeping V_D from 0 to 15 V at fixed V_G that ranged in 2 V steps from −10 to 10 V. An inset in Fig. 1(a) shows a top view schematic (not to scale) of IZO TFTs used in the present study, where the Mo S/D electrode length is 100 μm. Fig. 1(a–d) presents the typical I_D-V_D plots of the a-IZO TFTs with W/L = 100/50, 100/20, 100/10 and 100/5 μm, respectively, showing the significant effect of the channel downscaling on the output characteristics. It is evident in Fig. 1 that the drain current increases for shorter L due to a decrease in the channel resistance and, therefore, I_D saturation behavior is not observed for V_D < 15 V when L = 10 and 5 μm. Further, the devices with L < 50 μm cannot be fully turned off by the application of the relatively large V_G of −10 V.

The transfer characteristics of these a-IZO TFTs are presented in Fig. 2. The transfer I_D-V_G plots, measured at V_D = 0.2 V are plotted in Fig. 2(a) as a function of channel length L. While on- and off-state drain currents both slightly increase with decreasing L, the on/off I_D ratio is similar (~10^7) regardless of TFT channel length. The field effect mobility μ_{FE} and threshold voltage V_T of the IZO TFTs were determined in the linear regime using the conventional MOSFET equation for $V_D << (V_G - V_T)$:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \quad (1)$$

$$\approx \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_T)V_D \quad (2)$$

where C_{ox} is the oxide capacitance (6.90×10^{-8} F/cm^2 for 50 nm-thick SiO_2) used in our IZO TFTs. In Fig. 2(b), the extracted field effect mobility decreases as the channel length decreases from 39.3 ± 2.6 cm^2/V·s (L = 50 μm) to 9.9 ± 2.3 cm^2/V·s (L = 5 μm). Since the devices were fabricated simultaneously on the same Si substrate, the changes observed in the transfer characteristics and field effect mobility are solely attributed to channel downscaling. Additional backgated TFT devices were fabricated with the channel width W scaled down together with L in order to maintain the TFT aspect ratio of 20 (*i.e.*, TFTs with W/L = 1000/50, 500/25, 200/10, and 100/5 μm). Those devices exhibited the same trend in extracted μ_{FE} as shown in Fig. 2. A similar decrease in μ_{FE} with decreasing L was also observed in top-gated a-IZO TFTs [24].

To examine the performance variation in our IZO TFTs with channel length, TLM measurements were made on more than 48 IZO TFTs as a function of L and W. The TLM analysis allows the determination of both the channel resistivity and contact resistance through the equation [2,25] $(R_{Total}\cdot W) = (2R_C\cdot W) + (R_S\cdot L)$, where R_{Total} is the total resistance measured in the Ohmic (linear) regime of the output curve (at V_D = 0.2 V in this study), R_S is the channel sheet resistance, and R_C is the metallization/channel contact resistance. Detailed principles and procedures to extract contact resistances and the channel resistivity can be found elsewhere [2,7,25]. The total resistance normalized to channel width ($R_{Total}\cdot W$) is displayed in Fig. 3 as a function of L. The contact resistance is determined from the y-axis intercept ($2R_C\cdot W$), whereas the channel resistivity is calculated from the slope of the linear plot and the thickness (10 nm) of the channel IZO. The channel resistivity (ρ) of all IZO TFTs in this study is determined by the single slope of the plot in Fig. 3 and is found to be nearly identical as 2.03×10^{-2} Ω cm, as expected since the devices were fabricated simultaneously using the same processing sequence. Therefore, we conclude that the changes in the TFT performance shown in Fig. 2 with decreasing channel length is not associated with the alteration in channel conductivity, but rather the contact resistance. The inset in Fig. 3 shows a magnified ($R_{Total}\cdot W$) *vs.* L plot

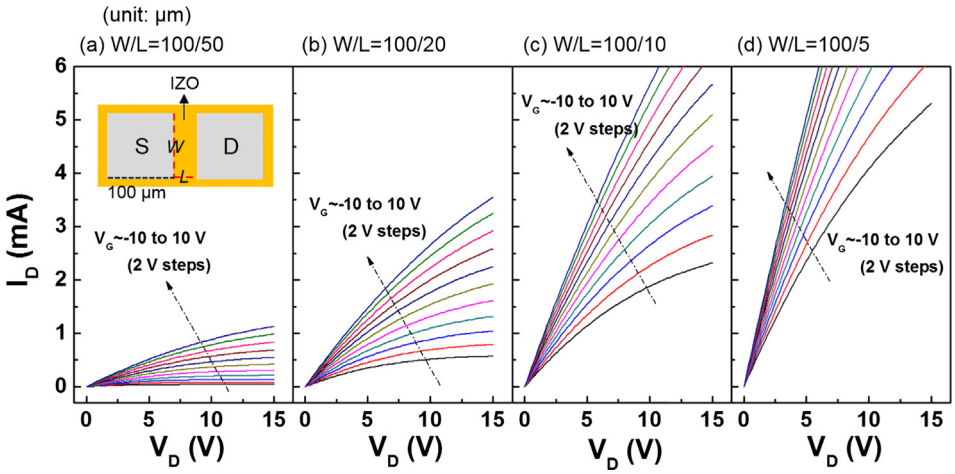

Fig. 1. Typical room-temperature (I_D-V_D) output characteristics of a-IZO TFTs at fixed V_G in the −10 to 10 V range for channel W/L ratios of 100/50 (a), 100/20 (b), 100/10 (c) and 100/5 μm (d). The inset in (a) shows a schematic top view of the device (not to scale).

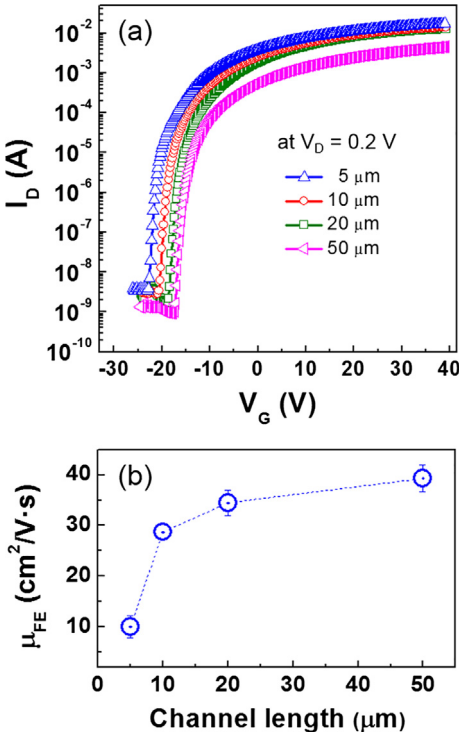

Fig. 2. (a) Typical transfer characteristics of the IZO TFTs measured at V_D = 0.2 V as a function of channel length L. (b) Extracted field effect mobility *vs.* channel length L showing a significant decrease with channel downscaling.

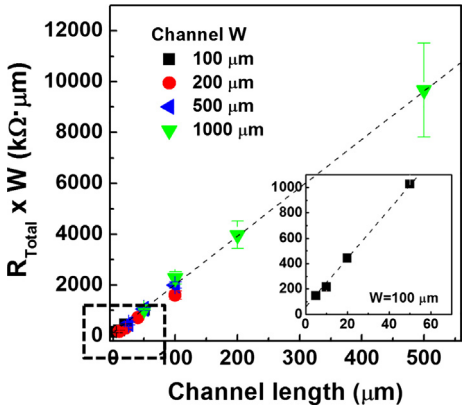

Fig. 3. Plot of channel width-normalized R_{Total} *vs.* channel length L from TLM analysis where the linear slope indicates that the channel resistivity is constant regardless of the TFT dimensions. Inset shows the magnified results of the dotted rectangle for W = 100 μm devices. The channel resistivity and the specific contact resistance are determined to be $2.03 \times 10^{-2}\,\Omega\,cm$ and $6.26 \times 10^{-5}\,\Omega\,cm^2$, respectively.

for W = 100 μm devices. From the y-axis intercept (~25.6 kΩ μm) of the IZO TFTs with W/L = 100/5, 100/10, 100/20 and 100/50 μm. The specific contact resistance (ρ_c) of the devices is found to be $6.26 \times 10^{-5}\,\Omega\,cm^2$. This ρ_c is significantly lower than those of our previous studies [2,4] of approximately 0.1–100 Ω cm², which is attribute to the much larger carrier density of ~7.7×10^{18}/cm³ in the present study than 4.6×10^{16}/cm³ of the TFTs with higher ρ_c, where the carrier density was estimated applying $\rho = (qn\mu_{FE})^{-1}$.

Continuing with the TLM analysis, Fig. 4(a) plots the ratio of $2R_C$ to R_{Total}. It should emphasized that the $2R_C/R_{Total}$ ratio increases with decreasing L: for instance, at V_G = 0, the $2R_C/R_{Total}$ ratio in the L = 5 μm is 16.4%, roughly a factor of 8 higher than the 2.1% value in the L = 50 μm device. This trend is obviously explained by the reduction in channel resistance with L and hence an increase of the $2R_C$ component of R_{Total}. We also observe an effect of the gate bias magnitude on the $2R_C/R_{Total}$ ratio, which increases as V_G becomes more positive (*e.g.*, at V_G = 10 V, $2R_C/R_{Total}$ = 4.5% and 31.0% for L = 50 and 5 μm, respectively). This is due to the V_G-controlled injection of electrons into the IZO channel that leads to a decrease in channel resistance and consequently R_{Total}. The results shown in Fig. 4(a) clearly show that the effective (not the absolute value applied on drain) source-drain V_D decreases significantly as channel scales down. Defining the contact resistance-corrected effective drain voltage V'_D as follows:

$$V'_D = V_D[1 - (2R_C/R_{Total})] \quad (3)$$

we can use the plots shown in Fig. 4(a) to recalculate the corrected output characteristics, shown in Fig. 4(b) and (c) for the IZO TFTs with L = 50 μm (longest in this study) and 5 μm (shortest), respectively. The dotted lines represent the corrected curves, showing an increase of I_D compared to the measured characteristics that are affected by contact resistance. Since the $2R_C/R_{Total}$ ratio increases strongly as L decreases, the correction is much more prominent for L = 5 μm IZO TFTs. Note that the validity of the corrected curves is limited to the linear regime (i.e., V_D <~ 5 V for

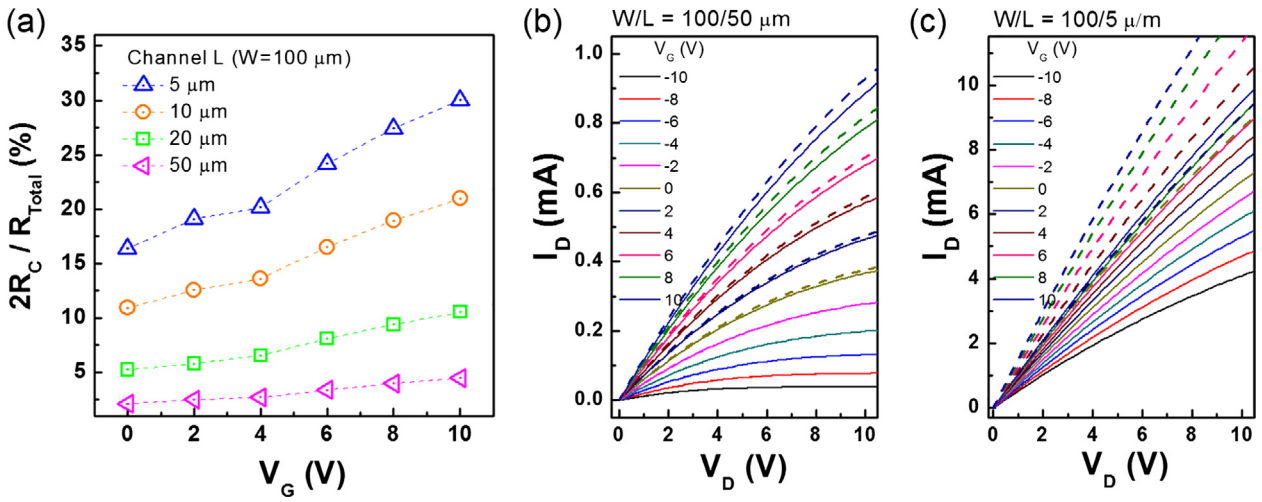

Fig. 4. (a) The $2R_C/R_{Total}$ ratio *vs* V_G as channel length scales down and a comparison of the series resistance-corrected I_D-V_D (dashed) and measured (solid) curves for $L = 50$ μm (b) and 5 μm (c).

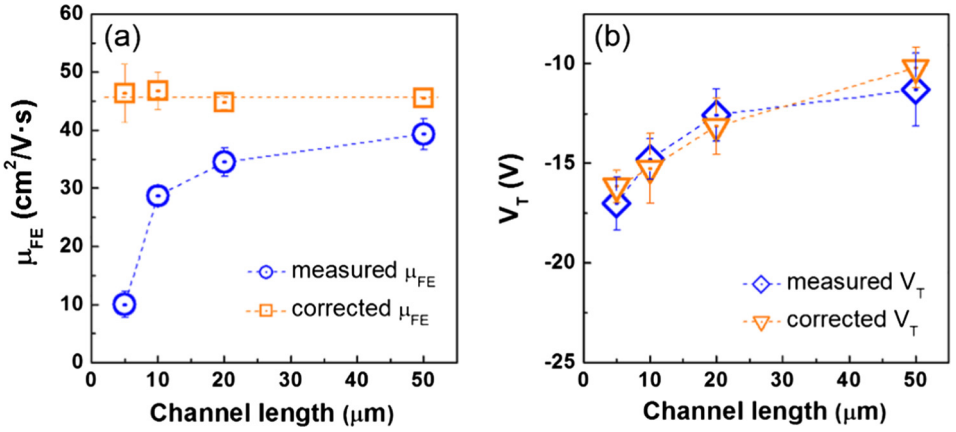

Fig. 5. Comparison of the corrected (a) field-effect mobility and (b) threshold voltage with their directly extracted values as a function of channel length L.

$L = 50$ μm and ~10 V for $L = 5$ μm) where the TLM analysis was performed.

In order to consider the effect of contact resistance on μ_{FE} and V_T as channel scales down and to determine the corrected values, Eq. (1) should be rewritten in terms of the contact-resistance corrected drain voltage V'_D and V'_G, where V'_G is the actual gate-to-source bias defined as $V_G' = V_G - V_D(R_C/R_{Total})$. In the linear regime, Eq. (2) becomes:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V'_G - V_T)V'_D$$
$$= \mu_{FE} C_{ox} \frac{W}{L}\left[\left\{V_G - V_D\left(\frac{R_C}{R_{Total}}\right)\right\} - V_T\right]\left[V_D\left(1 - 2\frac{R_C}{R_{Total}}\right)\right] \quad (4)$$

Eq. (4) can be rewritten by combining relevant terms as:

$$I_D = \left\{\mu_{FE}\left(1 - 2\frac{R_C}{R_{Total}}\right)\right\} C_{ox} \frac{W}{L}\left[\left\{V_G - V_D\left(\frac{R_C}{R_{Total}}\right)\right\} - V_T\right]V_D \quad (5)$$

According to this analysis and Eq. (5), the experimentally extracted field-effect mobility shown in Fig. 2(b) is actually $\mu_{FE}(1 - 2R_C/R_{Total})$, which clearly underestimates the true μ_{FE}. Further, when correcting μ_{FE}, V'_G needs to be recalculated as well, additionally increasing the corrected mobility, particularly for shorter channel devices because the (R_C/R_{Total}) factor is significantly higher, see Fig. 4(a). Unlike the underestimation of the extracted field effect mobility, no significant changes are expected for the threshold voltage after modification of the MOSFET equation: $V_D(R_C/R_{Total})$ is as small as ~0.002–0.03 V at the small $V_D = 0.2$ V used to measure the transfer characteristics. Instead, the change in threshold voltage visible in Fig. 2(a) is likely due to the instability of IZO TFTs under dc gate voltage bias: it has been reported that the V_T of IZO TFTs changes after stressing [26–28]. Here, IZO TFTs with larger L were measured first and, since all the TFTs shared the same back gate, TFTs with smaller L experienced a longer cumulative gate stress, leading to a larger V_T shift.

The corrected field-effect mobility and the threshold voltage values, extracted from Eq. (5) and the corrected I_D-V_D plots in the linear regime at small $V_D = 0.2$ V, are plotted in Fig. 5(a) and (b), respectively. The uncorrected μ_{FE} and V_T values are also presented for comparison. The corrected mobility of $L = 50$ μm TFTs is only slightly higher (45.4 ± 1.4 cm^2/V·s) than the uncorrected 39.3 ± 2.6 cm^2/V·s value. On the other hand, significant μ_{FE} differences are observed in shorter channel TFTs: corrected μ_{FE} values are much higher than uncorrected values and nearly identical (~46 cm^2/V·s) for all L. Therefore, the apparent collapse of the measured field-effect mobility in the shorter channel TFTs is mainly due to the larger contribution of contact resistance to the total resistance and the resulting decrease in effective V_D and V_G (a similar mobility collapse was noted in top-gated IZO TFTs and attributed to contact resistance [24], but no experimental validation was possible due to the lack of TLM patterns). Clearly, the modified Eq. (5) is useful in accurately analyzing the field-effect mobility of oxide TFTs, particularly as L is scaled down.

The comparison of the V_T between the corrected and uncorrected results is presented in Fig. 5(b). As theoretically discussed in connection with Eq. (5), recalculated threshold voltages are similar to the experimentally measured uncorrected V_T values. Therefore, threshold voltage shifts cannot be attributed to contact resistance issues, but rather to intrinsic voltage stress instabilities of the IZO TFTs [26–28].

4. Conclusion

In conclusion, as the channel length L of IZO TFTs is scaled down, direct experimental extraction of the field-effect mobility severely underestimates it due to increasing series contact resistance effects. The increasing R_C/R_{Total} ratio leads to a decrease in effective V_D and V_G. The TLM measurements and theoretical analysis provide the corrected I_D-V_D curves, from which the corrected field-effect mobility can be extracted. In our backgated IZO TFTs, this corrected field effect mobility is as high as $\sim$46 $cm^2/V{\cdot}s$ and nearly identical regardless of channel length L. No significant contact-resistance-induced correction in threshold voltage is observed. Our findings regarding the channel scaling may be useful in the analysis of other amorphous oxide TFTs, especially since future ultra-high definition displays will require downscaled TFTs with high current drive.

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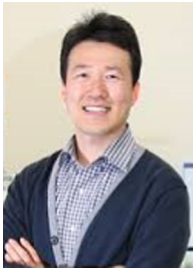
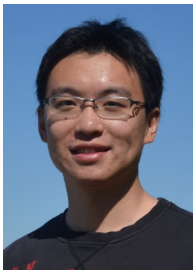
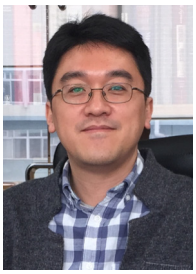


Sunghwan Lee received the Ph.D. degree from Brown University in 2013. He was a post-doctoral scientist at MIT and Harvard University from 2013 to 2015. He joined Baylor University in the Fall, 2015, where he is currently an Assistant Professor of Mechanical Engineering and Materials Science. His research interests are focused on transparent and flexible electronics, thin film transistors and energy conversion devices.



Yang Song received his ScB in physics from Nanjing University, 2012. He is currently pursuing his PhD at Brown University. His research interests are focused on amorphous oxide semiconductors, thin film transistors and semiconductor devices.



Hongsik Park received the Ph.D. degree from Brown University in 2011. He was a researcher at Samsung Advanced Institute of Technology, Korea from 1999 to 2006. He also worked at IBM T. J. Watson Research Center as a research staff member from 2011 to 2014. He is currently an associate professor at the School of Electronics Engineering at Kyungpook National University, Korea. His research interests are focused on integration of nanomaterial-based devices with conventional Si devices for Si photonics and integrated sensor applications.

Alexander Zaslavsky received the Ph.D. degree from Princeton University in 1991. He was a post-doctoral scientist with IBM T. J. Watson Research Center from 1991 to 1993. He joined Brown University in 1994, where he is currently a Professor of Engineering and Physics. He has also been a visiting Senior Chair at the Grenoble Polytechnic Institute 2009-12. His research interests are focused on semiconductor device and nanostructure physics, particularly tunneling and hot-electron devices.

David C. Paine received the Ph.D. degree from Stanford University in 1988. He joined Brown University in 1989, where he is a Professor of Engineering in the Materials Science group. His research interests are currently focused on transparent conducting oxides, amorphous oxide semiconductors, electron microscopy and thin film deposition and processing.