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Temporal and voltage stress stability of high performance indium-zinc-oxide thin film transistors

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ABSTRACT

Thin film transistors (TFTs) based on transparent oxide semiconductors, such as indium zinc oxide (IZO), are of interest due to their improved characteristics compared to traditional a-Si TFTs. Previously, we reported on top-gated IZO TFTs with an *in-situ* formed HfO_2 gate insulator and IZO active channel, showing high performance: on/off ratio of $\sim 10^7$, threshold voltage V_T near zero, extracted low-field mobility $\mu_0 = 95\ cm^2/V{\cdot}s$, and near-perfect subthreshold slope at 62 mV/decade. Since device stability is essential for technological applications, in this paper we report on the temporal and voltage stress stability of IZO TFTs. Our devices exhibit a small negative V_T shift as they age, consistent with an increasing carrier density resulting from an increasing oxygen vacancy concentration in the channel. Under gate bias stress, freshly annealed TFTs show a negative V_T shift during negative V_G gate bias stress, while aged (>1 week) TFTs show a positive V_T shift during negative V_G stress. This indicates two competing mechanisms, which we identify as the field-enhanced generation of oxygen vacancies and the field-assisted migration of oxygen vacancies, respectively. A simplified kinetic model of the vacancy concentration evolution in the IZO channel under electrical stress is provided.

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1. Introduction

Over the past decades, transparent amorphous oxide semiconductors (AOSs)—such as In-Zn-O (IZO) and In-Ga-Zn-O (IGZO)—have been widely studied as superior materials in making high-performance thin film transistors (TFTs). Compared to traditional amorphous silicon, AOSs have shown high field-effect mobility, high transparency in the visible wavelength region, room-temperature deposition capability on arbitrary substrates, high surface planarity, controllable carrier density and acceptable threshold voltage stability [1–7]. These superior characteristics have made AOSs very attractive for the display industry, where one type of AOS (IGZO) is already industrialized in making TFTs for backplane applications of active matrix organic light-emitting diodes (OLEDs). The need for practical application in display industry requires AOS TFTs to have stable characteristics, with threshold voltage V_T, on-state current I_{ON}, and on/off ratio I_{ON}/I_{OFF} remaining relatively unaffected due to aging, electrode biasing or environmental exposure. Several research groups have studied the V_T stability of IZO and IGZO TFTs under V_G gate bias stress [8–14] with varying results due to the complex mechanisms involved. The stability of the threshold voltage V_T in AOSs TFTs can depend on stress time and the magnitude of the V_G-induced electric field [8–15], AOS channel deposition technique and TFT structure [13,14], ambient atmosphere [11,12], thickness of the channel material [9] and different passivation materials [15]. Generally speaking, longer stress times and larger V_G-induced electric fields yield larger V_T shifts. These shifts could be related to creation of defect states near channel/dielectric interface [4] or the trapping of charges in the dielectric layer [4,8,10], which further depend on the quality of dielectric layer. A passivation layer is known to improve TFT stability because AOS material may be sensitive to ambient atmosphere [15], with reports of hydrogen/water and oxygen shifting transfer curves in opposite ways during gate bias stress [11,12]. Due to these complications, when measuring threshold stability in amorphous material, researchers often use empirical power-law or stretched-exponential equations to fit experimental data [16].

In this paper, we will report on both the temporal and the voltage stress stability of our high-performance of top-gated IZO TFTs with a HfO_2 dielectric gate insulator. We find that as our IZO TFTs age (in darkness at room temperature), they exhibit a V_T shift towards negative voltages, indicative of increasing oxygen vacancy concentration in the IZO channel material (where oxygen vacan-

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cies are the primary donor species [17]). Then voltage stress stability of IZO TFTs is investigated, where two different directions of V_T shift under negative V_G stress are observed on freshly-annealed TFTs and aged TFTs, indicating two different competing mechanisms. Based on experimental results, we identify these two mechanisms as the field-assisted creation of oxygen vacancies (increasing channel doping and making the channel more difficult to deplete, leading to a negative V_T shift) and field-induced migration of positively-charged oxygen vacancies towards the top interface (leading to a positive V_T shift). A preliminary theoretical analysis of both mechanisms, consistent with the experimental data, will be provided later in this paper.

2. Fabrication

The fabrication processes for TFTs shown in Fig. 1(a) and (b) are similar since they have similar structures. For the first structure in Fig. 1(a), the detailed fabrication process follows our previous publication [18]. To further reduce gate leakage and improve gate dielectric material reliability, an additional layer of high quality HfO_2 can be deposited between e-beam deposited HfO_2 and top gate contact by atomic layer deposition (ALD). This modified structure of IZO TFTs is shown in Fig. 1(b). For both types of devices we started with a silicon wafer coated with 500 nm thermally grown SiO_2, on top of which we deposited 20 nm of IZO sputtered from a 90 wt.% In_2O_3-10 wt.% ZnO target by dc magnetron sputtering at room temperature. During IZO deposition, the distance between sputter target and silicon wafer was 10 cm; the dc bias was 280 V with a power density of 0.22 W/cm^2; the ambient gas flow was kept at a volume ratio Ar/O_2 = 86/64. Then, the IZO active channel was patterned by using conventional photolithography, followed by dilute HCl etching. After IZO active channel deposition, the source and drain metal electrodes were patterned by photolithography and lift-off: the contact metal stack was 50 nm Mo, 10 nm Cr and 100 nm Au, sequentially deposited by e-beam evaporation. After that, Hf metal was deposited on gate area using the same e-beam evaporation technique, while there was a small oxygen flow at ~1 sccm and relatively high chamber pressure of $\sim 2 \times 10^{-5}$ Torr. Due to the existence of oxidants in the chamber, after Hf deposition, there was a 16 nm partially oxidized layer of HfO_x on top of IZO. Then, in the case of devices of Fig. 1(b), an additional 24 nm layer of HfO_2 was deposited by using ALD from a $Hf(N(CH_3)_2)_4$ precursor at 200 °C within 2 h, to provide a better gate dielectric insulator stack as well as a passivation layer for the exposed IZO layer between the top gate and source/drain electrodes. Finally, a photolithographically-defined top-gate electrode consisting of 10 nm Cr and 70 nm Au was deposited by e-beam evaporation and lifted off. The final TFTs had width W = 200 µm and gate lengths L_G = 50, 100, or 150 µm.

As described in our previous publication [18], the TFTs show transistor characteristics only after annealing for 4 h at 300 °C in air, because before annealing, those TFTs do not have a sufficiently good dielectric/IZO interface to permit gate control of the carriers in the IZO channel. Annealing allows the partially oxidized layer of HfO_x to react with the IZO channel to form a fully oxidized HfO_2 insulator layer in the near-interface region. This reaction-formed interface has been shown [18] to provide a high interface quality and excellent device results. The reaction and formation of HfO_2 at the gate/channel interface is predicted, in the absence of kinetic constraints, by the negative free energy of reaction between Hf metal and indium oxide ($\Delta G = -807.6$ kJ/mol at 200 °C) [19].

After annealing, both types of IZO TFTs were characterized by using a Hewlett-Packard multi-frequency LCR meter (model 4275A, to measure capacitance) and Agilent 4155C semiconductor parameter analyzer (to measure current-voltage characteristics). In addition to room-temperature measurements, the TFTs were also measured as a function of temperature in the T = 200–350 K range by using a variable-temperature cryostat.

3. Experimental results

The TFT characteristics were measured using a semiconductor parameter analyzer in a light-tight box with the substrate grounded. Fig. 2(a) shows the transfer curves of TFTs without additional ALD-deposited HfO_2 passivation, as in Fig. 1(a), measured 15 days after annealing in air, showing an on/off ratio about 10^7, with no apparent threshold shift between the two curves at different drain voltage (V_D = 0.1 and 1.0 V). Instead of estimating the saturation mobility, often reported in TFT characterization [20], we use the Y-function to calculate a more reliable low-field channel mobility μ_0 [21]:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L_G}\mu_0 C_{ox} V_D (V_G - V_T)} \quad (1)$$

where $g_m = \partial I_D / \partial V_G$ is the transconductance, μ_0 is the low-field mobility, and C_{ox} is the gate capacitance per unit area. The estimated threshold voltage is $V_T = -0.02$ V and low field mobility is $\mu_0 = 95$ cm^2/V·s. The subthreshold slope is remarkably small: SS ~ 62 mV/decade, close to the room temperature theoretical limit of $2.3k_BT/e$ = 60 mV/decade. The corresponding transistor characteristics of devices with an added ALD-deposited HfO_2 layer, shown in Fig. 1(b), are presented in Fig. 2(b). Again, we observe excellent transistor characteristics, with SS ~ 67 mV/decade. The measured

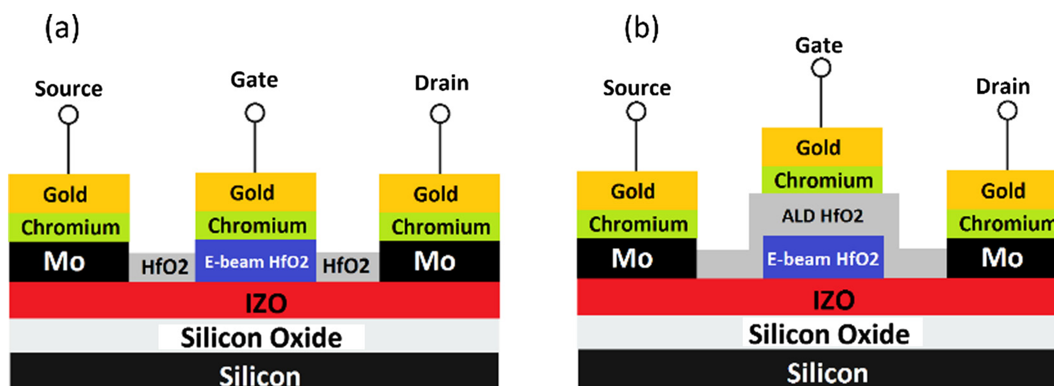

Fig. 1. Schematic cross sectional view of IZO TFTs with e-beam deposited and *in-situ* reacted HfO_2 gate dielectric without (a) and with (b) an additional ALD-deposited HfO_2 layer underneath the gate electrode.

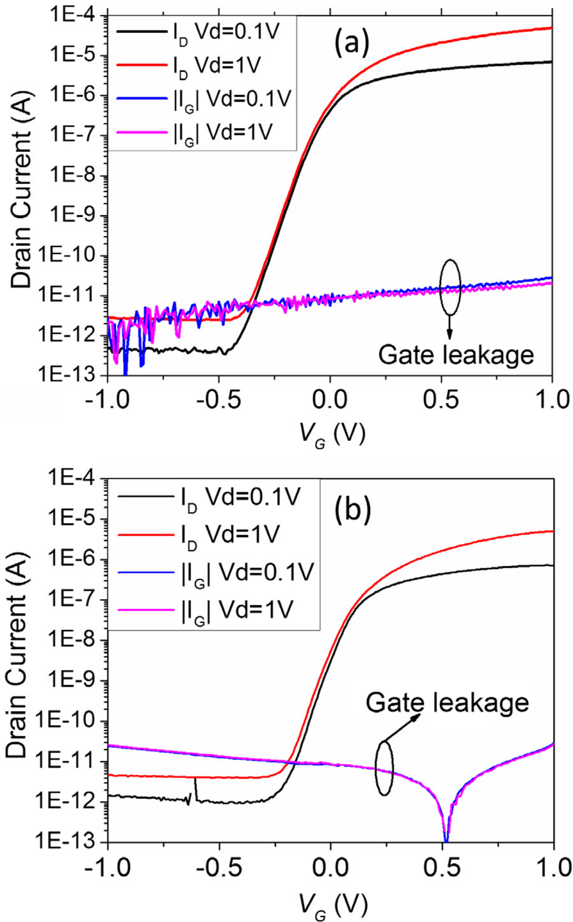

Fig. 2. (a) Transfer I_D–V_G curves of IZO TFTs shown in Fig. 1(a) at V_D = 0.1 and 1 V, with W/L_G = 200/50 μm. The subthreshold slope SS ~ 62 mV/decade. Gate leakage I_G is also shown; (b) Transfer I_D–V_G curves of TFTs with additional ALD-deposited HfO_2 shown in Fig. 1(b), with W/L_G = 200/50 μm and SS ~ 67 mV/decade.

gate leakage shown in Fig. 2 is acceptably small, consistent with the expected conduction band offset in the HfO_2/IZO heterostructure [22]. Furthermore, the yield of functional devices with negligible I_G reaches 100% (of 10 devices measured).

While the performance of our IZO TFTs is high, in this paper we focus on the stability of these devices. After 4-h-annealing, IZO TFTs that have structure showing in Fig. 1(a) were kept at room temperature in a light-tight box up to ~100 days in order to study their "on-shelf" stability. From day 1 to 101, the corresponding transfer curves are shown in Fig. 3, with a clear negative V_T shift as the device ages: the shift is pronounced during the first week and then slows. It is worth mentioning that while the V_T shifted as the TFT aged, neither the near-perfect SS ~ 62 mV/decade nor the I_{ON}/I_{OFF} ratio degrade with time. Fig. 3(b) shows an increase of I_D measured at V_D = 0.1 V at the same gate overdrive ($V_G - V_T$) = 0.5 V from 9 μA on day 1 to 85 μA at day 8, eventually stabilizing around 95 μA after 23 days, as V_T keeps shifting slowly to negative values. Finally, Fig. 3(c) plots the estimated oxygen vacancy density N_V in the channel, calculated by assuming a uniform volume distribution and using the measured low-field mobility μ_0 = 95 cm^2/V·s. The observed increase in N_V as devices age [23] leads to higher effective channel doping and hence aged devices require a more negative V_G to deplete the electrons from the IZO channel.

It is well established [17,24] that native-defect doping by doubly-charged oxygen vacancies is the dominant source of carriers in IZO. The carrier density in IZO can, therefore, be controlled by tuning the oxygen partial pressure during the IZO deposition process [17], or by annealing in an oxygen ambient, or via a solid-state reaction [24,25]. Typically, in order to fabricate functional TFTs that can be depleted by acceptably low gate voltages, the oxygen vacancy (and hence the carrier density) of deposited IZO must be controlled at the 10^{17}–10^{18} cm^{-3} level. A study (similar to Brouwer analysis) of the pressure dependence of the equilibrium oxygen vacancy concentration in the IZO system [17] revealed that the equilibrium vacancy concentration at atmospheric pressure in this material is approximately 10^{20} cm^{-3}, which suggests that the carrier density in as-deposited materials will, subject to kinetic constraints, tend to increase with time, and that this increase can be accelerated by higher-temperature annealing [17]. A second source of carriers in the IZO channels of our devices is active during the solid-state *in-situ* formation of the channel/gate dielectric interface. This reaction, however, is likely to be self-limiting due to the slow diffusion of oxygen in stoichiometric HfO_2 and is unlikely to play a role in post-anneal room temperature aging.

In order to further elucidate the IZO TFT stability, gate capacitance C-V_G was measured as a function of V_G stress and temperature T. All the C-V_G measurements were conducted on TFTs with structure shown in Fig. 1(b). During C-V_G measurement, the TFT was kept in darkness in a variable-temperature cryostat, with the source, drain and substrate all connected. An LCR meter with a 40 kHz testing signal was used to measure gate capacitance. In one complete C-V_G hysteresis curve measurement, the gate voltage V_G was swept from −3 V to 3 V then back to −3 V. To investigate IZO TFTs stability under dc gate bias stress, we used the following measurement procedure: first, before any stress, a C-V_G hysteresis curve was measured as a reference curve; then a V_G = −3 V stress was applied to the gate for 25 min, followed by another C-V_G hysteresis curve trace; finally, a V_G = 3 V stress was again applied for 25 min, followed by a final C-V_G hysteresis curve (to see whether the observed V_T shifts could be recovered). The same procedure was repeated at different temperatures T.

Interestingly, the shifts observed in our TFTs depend on the device age. The results of the voltage stress measurements for relatively fresh devices (day 4) are shown in Fig. 4, whereas the corresponding results on aged devices (day 24) are presented in Fig. 5. In fresh devices we observed that at T = 300 K, the V_T shifts strongly in the negative direction after the 25 min V_G = −3 V stress and this ΔV_T ~ 0.5 V shift is not recovered by the subsequent V_G = 3 V stress. We define the ΔV_T shift as the change in V_G at the midpoint of the capacitance curve, *i.e.* the change in V_G at $C = (C_{min} + C_{max})/2$. At lower T the shifts are much weaker, with no visible ΔV_T at T = 200 K or below. The inset in Fig. 4(c) plots the ln|ΔV_T| against the inverse measurement temperature 1/T, from which an activation energy E_a ~ 0.15 eV can be extracted. Similar measurements on aged TFTs (older than one week), result in the opposite V_T shifts after negative stress. In Fig. 5 we reproduce similar data on a 24 day-aged device. Now we observe positive V_T shifts as a function of negative V_G stress. The ΔV_T is also smaller in aged samples, as can be seen by comparing the T = 300 K traces in Figs. 4(c) and 5(b), and no visible shifts in aged samples can be seen at T = 220 K. However, by extending our measurement temperature range up to T = 350 K, we are able to construct the activation plot shown in the inset of Fig. 5(c). We find that the trend is similar, but the activation energy is somewhat larger, around ~0.2 eV.

To sum up, we observe opposite V_T shifts in fresh and aged IZO TFTs: in fresh devices, shortly after the in-air annealing, we see a negative V_T shift under negative V_G stress; then as TFT ages, the magnitude of negative V_T shift becomes smaller; finally, in aged (more than a week after annealing) TFTs, the V_T shifts to positive voltages in response to negative V_G stress. In all cases, the subsequent application of a positive V_G stress does very little to change V_T. More interestingly, we can observe both positive and negative

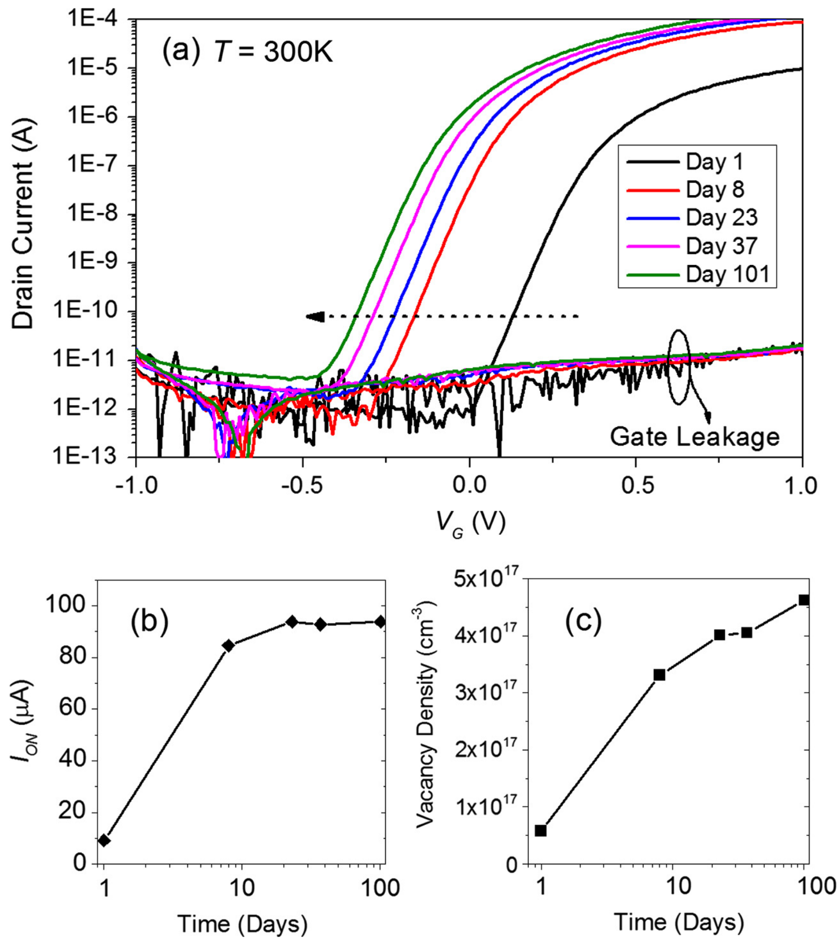

Fig. 3. (a) TFT I_D–V_G transfer curves at V_D = 0.1 V *vs.* age after in-air annealing, from freshly annealed (day 1) onwards, showing a negative V_T shift and an increase in I_{ON}; (b) I_D measured at V_D = 0.1 V at the overdrive voltage (V_G – V_T) = 0.5 V *vs.* age; (c) corresponding estimated vacancy density N_V in the IZO channel.

V_T shifts at the same time in the same sample: this is illustrated in a day 6 TFT where we maintained V_G at −1.5 V, near the midpoint of the original C-V_G curve (shown in Fig. 6(a)), and measured capacitance against stress time. As we see in Fig. 6(b), the capacitance first decreased (equivalent to a positive V_T shift) and then began increasing after ∼100 s (equivalent to a negative V_T shift). Clearly, there are two different mechanisms governing the stability of IZO TFTs.

4. Analysis of V_T stability

Since there are two different and competing mechanisms governing V_T stability in freshly annealed and aged IZO TFTs, here we will discuss these two processes theoretically.

4.1. In fresh IZO TFTs—oxygen vacancy generation

There are several possible mechanisms for the negative V_T shift after negative stress observed in freshly-annealed IZO TFTs. As mentioned above, the most obvious is the creation of additional doubly-charged oxygen vacancies [17] that are responsible for doping the IZO channel and providing the mobile electrons. Clearly, a greater vacancy density N_V effectively increases the channel doping, meaning a more negative V_G is required to deplete the channel and shut off the current I_D. However, there are other possible mechanisms. For example, positive charge trapping near the gate dielectric layer/IZO channel interface [4,10] can also lead to a negative V_T shift, as can charge injection into the gate dielectric layer, which usually happens at a high stress voltage [8]. Under high electric field, positive or negative charges can tunnel and get trapped in the dielectric layer. During negative stress, if there are more positive charges trapped in dielectric layer, V_T would also shift towards negative voltages.

Based on experimental results, we believe that only the first mechanism—creation of additional oxygen vacancies—is consistent with the negative V_T shift after negative V_G stress that we observe in fresh samples. For the second and third mechanism (positive charge trapping near the dielectric interface or positive charge injection into the dielectric layer), would require positively charged mobile carriers (holes) in IZO. But no significant hole density can exist in an oxygen vacancy-doped high-bandgap material. Furthermore, if hole trapping were a major effect, V_T shift should also change under positive gate stress, but this does not agree with our observations of a large V_T shift happened after −3 V stress, but very little V_T shift after a 3 V gate stress.

To describe the oxygen vacancy generation process, we can start by assuming a thermally-activated oxygen-metal bond breakage assisted by the local electric field [26,27]:

$$G = G_0 exp\left(-\frac{E_a - Fb}{k_B T}\right) \quad (2)$$

where G is the oxygen vacancy generation rate, G_0 is a constant, E_a is the vacancy generation activation energy, F is the electric field inside the IZO channel when it is depleted (under negative stress), b is the polarization factor of IZO material, k_B is the Boltzmann con-

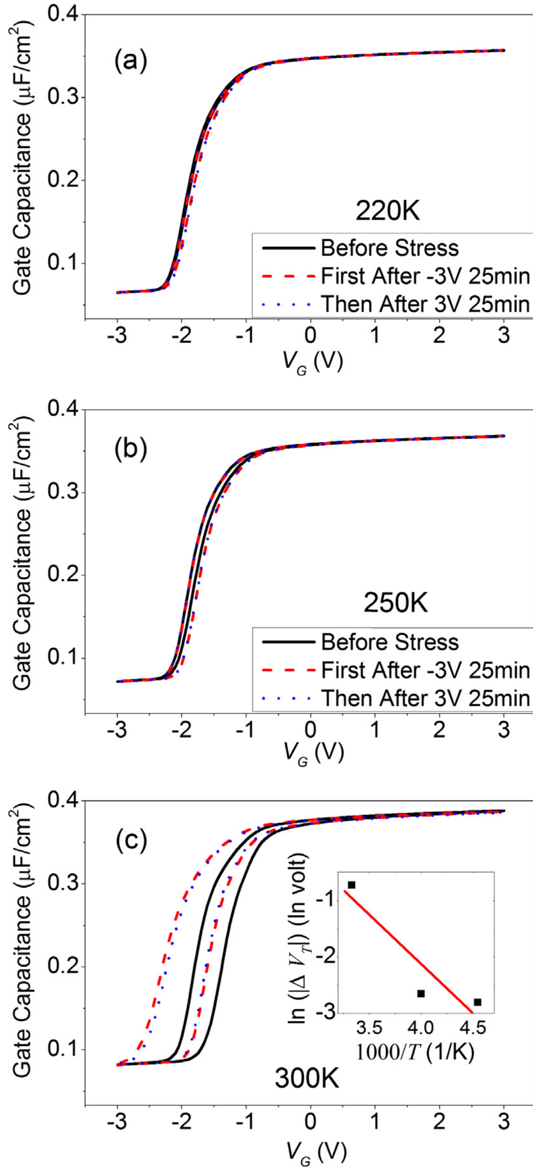

Fig. 4. C-V_G curves measured on freshly annealed (day 4) IZO TFTs at different temperatures: $T = 220$ K (a), 250 K (b), and 300 K (c) showing the temperature-dependent negative V_T shift after -3 V stress. Inset in (c) plots the shift ΔV_T *vs.* $1/T$, from which an activation energy ~0.15 eV is estimated.

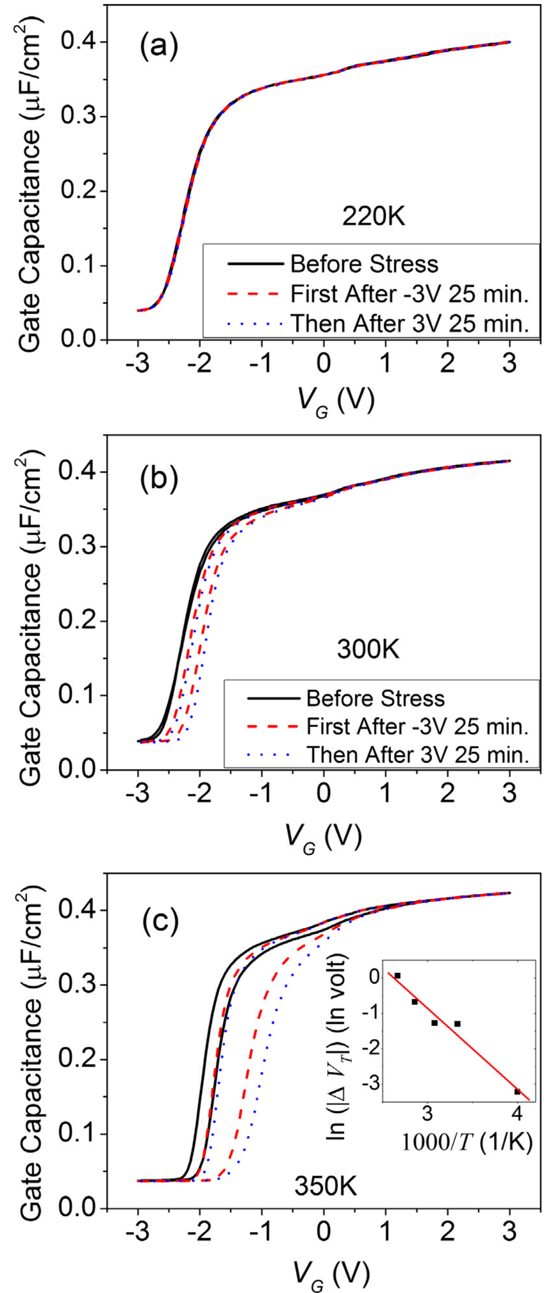

Fig. 5. C-V_G curves measured on an aged (day 24) IZO TFTs at $T = 220$ K (a), 300 K (b), and 350 K (c), where we observe a positive V_T shift in response to negative V_G stress. The inset in (c) plots ΔV_T *vs.* $1/T$, from which an activation energy ~ 0.2 eV is estimated.

stant. The polarization factor can be estimated using the following expression [26]:

$$b = P_o \frac{2 + \varepsilon_{\mathrm{IZO}}}{3} \tag{3}$$

where

$$P_o = N\left(\frac{Valence}{2}\right) * e * \frac{d_{M-O}}{3} \tag{4}$$

Assuming the number of active metal-oxygen dipoles $N = 4$–6 [28], metal-ion valence state of 3, bonding distance $d_{M-O} = 0.2$ nm, and assuming IZO has a similar static relative dielectric constant as ITO [29] $\varepsilon_{\mathrm{IZO}} \sim 10$, yields a polarization factor $b = 16$–24 eÅ.

Given the vacancy generation rate G of Eq. (2), we then assume the vacancy concentration N_V can be described by a standard generation-relaxation equation with some characteristic relaxation time τ:

$$\frac{dN_V}{dt} = G - \frac{N_V}{\tau} \tag{5}$$

with a solution:

$$N_V(t) = G_0 \exp\left(-\frac{E_a - Fb}{k_B T}\right)\tau\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] \tag{6}$$

As follows from Eq. (6), the oxygen vacancy concentration increases with time, initially linearly and then more slowly, eventually reaching an equilibrium value after a time t ≫ τ:

$$N_V(+\infty) = G_0 \exp\left(-\frac{E_a - Fb}{k_B T}\right)\tau. \tag{7}$$

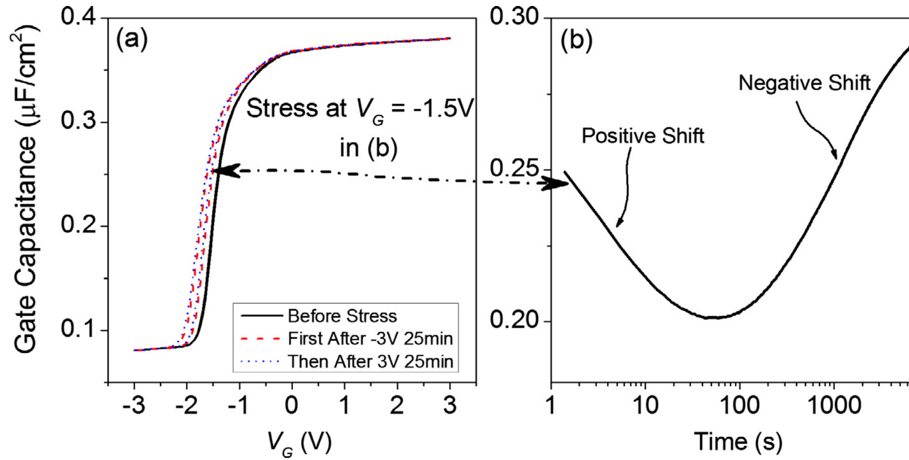

Fig. 6. (a) C-V_G curves on TFTs aged 6 days after annealing, measured at T = 300 K; (b) change of capacitance *vs.* stress time at a fixed $V_G = -1.5$ V near the midpoint of the C–V_G trace, demonstrating two opposite V_T shift directions.

In standard depletion-mode transistors, if the doping density in the channel is uniform, the V_T depends linearly on channel doping:

$$V_T \propto \left(\frac{t_{\mathrm{IZO}} * t_{\mathrm{HfO2}}}{\varepsilon_{\mathrm{HfO2}} * \varepsilon_0} + \frac{t^2_{\mathrm{IZO}}}{2 * \varepsilon_{\mathrm{IZO}} * \varepsilon_0}\right) * N_V * 2e \quad (8)$$

where t_{IZO} and t_{HfO2} are the thicknesses of IZO channel and HfO_2 layer, $\varepsilon_{\mathrm{HfO2}}$ and $\varepsilon_{\mathrm{IZO}}$ are the relative permittivities of IZO channel and HfO_2 layer, and ε_0 is the permittivity of vacuum. In IZO, the dopants are oxygen vacancies. If we assume the oxygen vacancy concentration $N_V(t)$ to be uniform in the IZO channel at all times, then by plotting $-V_T \sim N_V(t)$ against time in Fig. 7 we can obtain the relaxation time τ, which we infer to be $\tau \sim 15$ days. It is worth pointing out that relaxation time τ need not be a constant and could depend on temperature and applied stress. However, if all the other conditions are kept constant, we can assume a constant τ, and estimate it from the experimental data on unstressed devices in Fig. 3 as $\tau \approx$ 15 days. Further, assuming $\tau = \tau_0 \exp\left(\frac{E_r}{k_B T}\right)$ with $\tau_0 \approx 10^{-12}s$, corresponding to typical atomic vibrational frequencies, we can evaluate the relaxation activation energy $E_r \approx 1.1$ eV.

As shown in Fig. 4, the activation energy of the process that yields a negative shift under gate bias is found to be $E' \sim 0.15$ eV. According to Eq. (7), $E' = E_a - Fb - E_r$. Using estimated above values of the polarization factor, b, and the relaxation activation energy, E', one can estimate the vacancy formation energy $E_a = E' + Fb + E_r \approx (1.3–1.4)$ eV. This is significantly less than the activation energy reported [17] for carrier density increases associated with charged vacancy creation and annihilation. In the context of an amorphous oxide, it is assumed that charged vacancies are associated with In-O coordination defects in the amorphous solid. The lower activation energy that we measure here suggests that a second, irreversible oxygen vacancy generation process exists in freshly deposited IZO. This irreversible change is, we speculate, associated with metal-oxygen coordination defects that exist in the as-deposited materials and which, over time, are consumed as the amorphous solid undergoes relaxation to a more stable state. This more stable state includes indium-oxygen coordination and bond angles changes that, in effect, lower the activation energy for the formation of oxygen vacancies. In this way, the increase in carrier density via the formation of charged oxygen vacancies is initially facilitated by the relaxation of the amorphous solid. As the as-deposited IZO TFT ages and stabilizes, the vacancy generation process slows down and, eventually, V_T stops shifting towards negative values under negative V_G stress. At this point another mechanism, one associated with the migration of oxygen vacancies, starts to dominate V_T stability.

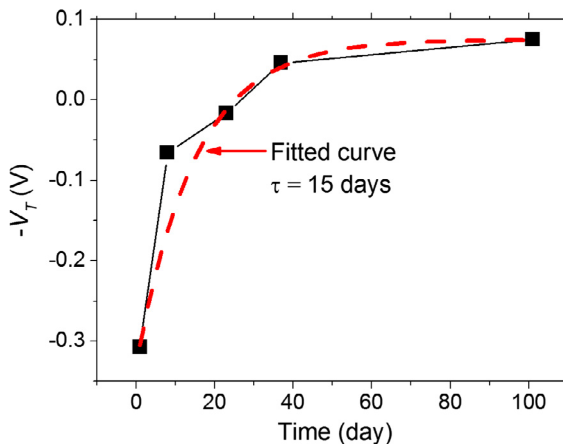

Fig. 7. Based on transfer curves shown in Fig. 3, change of threshold voltage V_T is shown as a function of storage time. The red dashed line is the fitted curve using Eq. (6) with a relaxation time $\tau \sim 15$ days.

4.2. In aged IZO TFTs—migration of oxygen vacancies

The above model for the relaxation of amorphous IZO assumes that the vacancy density N_V in the IZO channel changes in time but is uniformly distributed. However, unlike dopants in single-crystal semiconductor TFTs, charged vacancies can migrate in an electric field. Field-driven vacancy migration is, in fact, the mechanism to which we attribute the positive V_T shifts observed under negative V_G stress in aged TFT samples (in which N_V has reached a stable higher value, as in Figs. 7 and 3(c)).

Generally, if the total number of vacancies in the channel is assumed to have reached steady state, a plausible mechanism for the observed positive V_T shifts under a negative V_G stress is vacancy migration. The charged vacancies can move towards the dielectric/IZO interface driven by the vertical electric field F in the channel. As a result, the doping profile of IZO will be changed, shifting the mobile electrons towards the dielectric/IZO interface from the IZO body, which makes it easier to deplete the IZO channel. In other words, V_T will shift towards positive values after negative V_G stress. At the same time, under positive V_G the IZO channel is flooded with electrons, so there is almost no vertical F and the vacancies can only be redistributed through the much slower diffu-

sion process. Migration of oxygen vacancies thus explains why major V_T shifts happen only after negative stress, whereas the subsequent positive stress does not induce a large change in V_T.

Redistribution of positively-charged oxygen vacancies under a vertical electric field F can be described by the following diffusion equations:

$$\frac{\partial N_V(x,t)}{\partial t} = -\frac{\partial J_V}{\partial x} \tag{9}$$

$$J_V = -D_V \frac{\partial N_V}{\partial x} + N_V \frac{D_V}{k_B T} 2eF \tag{10}$$

where x is the position away from the dielectric/IZO interface, J_V is vacancy current flux, and D_V is the vacancy diffusion coefficient. In Eq. (10), vacancy current flux is assumed to have two parts: a diffusion current and a drift current, where the Einstein relation is used to further simplify the equation.

The time-dependent solution of vacancy density $N_V(x, t)$ can be solved by numerical calculation, which is beyond the scope of this paper. Instead, we will consider the steady state distribution $N_V(x)$ after a long time. In this case, in a steady state, Eq. (10) becomes:

$$\frac{\partial N_V}{\partial x} = N_V \frac{1}{k_B T} 2eF \tag{11}$$

Assuming the total number of oxygen vacancies is fixed, we can integrate the Gauss' law relation between F and $N_V(x)$:

$$\frac{dF}{dx} = \frac{2e * N_V(x)}{\varepsilon_{IZO}}. \tag{12}$$

to obtain:

$$F_0 = \int \frac{2e * N_V(x)}{\varepsilon_{IZO}} dx \tag{13}$$

where F_0 is the electric field in IZO at the $x = 0$ dielectric/IZO interface. Then, combining Eqs. (11)–(13), the steady-state distribution of vacancies is given by:

$$N_V(x) = \frac{\varepsilon_{IZO}}{k_B T} F_0^2 \frac{B}{(B+1)^2}, \tag{14}$$

where

$$B = B_0 \exp\left(\frac{2eF_0 x}{k_B T}\right) \tag{15}$$

where the constant B_0 is determined by the total number of vacancies. For large F_0, we have $B \gg 1$, so Eq. (14) can be further simplified as follows:

$$N_V(x) \approx \overline{N_V} \exp\left(-\frac{2eF_0 x}{k_B T}\right) \equiv \overline{N_V} \exp\left(-\frac{x}{l}\right) \tag{16}$$

Under large negative stress, $V_G = -3$ V, F_0 is of order of 10^5 V/cm, resulting in a very small $l = k_B T/2eF_0 \sim 1$ nm. Such a small value of l means the almost all the vacancies are within few nanometers from the dielectric/IZO interface. As a result, it is easier to deplete the IZO channel, meaning V_T will exhibit a positive shift. If we assume that before stress, oxygen vacancies had a uniform distribution with $N_V \sim 10^{18}$ cm^{-3}, the change of $N_V(x)$ from a uniform to an exponential distribution of Eq. (16) would result in a threshold shift $\Delta V_T \sim 1$ V, which agrees with the experimental results in Fig. 6.

5. Conclusion

We presented the temporal and voltage stress stability of two types of high-performance IZO TFTs with an e-beam deposited and *in-situ* reacted gate HfO_2 insulator layer. The TFT transfer characteristics were found to evolve with time, with the threshold voltage shifting towards negative values as the devices aged (in darkness at room T). Further, we observed that negative dc gate bias stress led to threshold shifts in opposite directions in freshly annealed and aged IZO TFTs, suggesting two competing mechanisms underlying the lack of threshold voltage stability. We attribute the observed shifts to oxygen vacancy generation (which occurs naturally with time but is accelerated by a large electric field), as well as to the field-driven migration of positively charged vacancies, and present kinetic models of both mechanisms, subject to a number of simplifying assumptions.

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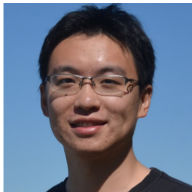

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