# Novel photodetector based on FD-SOI substrate with interface coupling effect


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## Abstract

We have proposed and demonstrated experimentally a novel semiconductor photodetector based on fully depleted silicon-on-insulator (FD-SOI) substrate. The device utilizes the interface coupling effect uniquely found in FD-SOI MOSFET, in which the photo-generated electrons accumulate at the top interface modulate the hole current at the bottom interface. The responsivity of this device reaches more than $1\times10^4$ A/W and, unlike other photodetectors based on SOI substrate, increases as the top silicon layer thickness reduces.


## 1. Introduction

Compared to the metal-oxide-semiconductor field-effect-transistor (MOSFET) built on bulk substrate, MOSFET built on SOI substrate has less short channel effect thanks to the thin body of the top silicon device layer. Besides, the MOSFET based on SOI has low parasitic capacitance and low leakage current, and thus attracts lots of interests in very large scale integrated circuit (VLSI) for radio frequency and low power consumption applications [1-5]. The MOSFET built on SOI also exhibits strong radiation hardness and can find applications in radiative environments, such as in aerospace and nuclear reactor.

The photodetector, as a bridge connecting electronic and photonic devices, plays important role in various systems, such as optical communication, imaging and spectrum analysis. Photodetector integrated on SOI substrate benefits from the advantages of the SOI. However, conventional photodiode (PD) based on SOI substrate suffers from low responsivity due to the poor absorption coefficient of the top thin Si layer [6]. Especially in advanced FD-SOI technology node, the Si device layer is reduced below 6 nm in order to effectively suppress the short channel effect [7].

Various methods have been explored to tackle this issue. Techniques, such as nano-structure inducing surface plasma and back-side reflection, are employed in the SOI photodetector to improve the light absorption coefficient [8, 9]. On the other hand, devices with internal gain have been demonstrated to effectively amplify the low photo-generated current in the top Si layer. For example, MOSFET, bipolar junction transistor and junction field effect transistor are used to largely increase the responsivity and obtain high output photocurrent [10-12] . A body-gate tied MOSFET built on silicon-on-sapphire (SOS) substrate can reach up to $2.2\times10^5$ A/W, thanks to the high internal gain and low loss of light through sapphire substrate [13-15]. Most recently, FD-SOI based MOSFET with embedded photodiode has been demonstrated with interesting photosensing performances [16, 17].

In this work, we propose a novel photodetector on SOI named interface coupled photodetector (ICPD). The photodetector utilizes the interface coupling effect in FD-SOI MOSFET, where the carrier at one interface affects the threshold voltage ($V_{th}$) and current at the other interface [18, 19]. The operation principle of the device is confirmed by the TCAD simulation. The device is fabricated with a simplified process followed by a photoelectric measurement, demonstrating a responsivity up to $1\times10^4$ A/W.

## 2. TCAD simulation and operation principle

The design of the ICPD structure and study of its operation principle are conducted with TCAD simulation in Synopsys Sentaurus. A schematic of the designed device is shown in Fig. 1(a) with a SOI substrate of 200 nm top Si layer and 500 nm buried oxide (BOX). The channel is lightly p-doped with concentration of $10^{15}$ $cm^{-3}$. The distance between source and drain is 5 µm and the gate length is 1um sitting at the middle of the source/drain gap. The bottom gate is negatively biased ($V_{BG} < 0V$) to accumulate holes and forms a source/drain conductive path at the bottom interface (top Si /BOX interface). The top gate partially covers the channel and is positively biased ($V_G > 0V$). The $V_G > 0V$ affects the threshold voltage ($V_{th}$) of the bottom conductive channel through the top Si film, known as interface coupling effect. The $V_G > 0V$ also accumulates electrons at the top interface, which screen the electric field from $V_G$, and thus reduce the controllability of $V_G$ on the bottom channel. When the device is subjected to illumination, the photogenerated electrons are accumulated by the $V_G > 0V$ and thus increases the electron density at the top interface. This reduces the coupling of $V_G$ to the bottom interface, and reduces the $|V_{th}|$ of the bottom channel. The reduction of $|V_{th}|$ further translates to the increase of current which outputs as amplified photocurrent.


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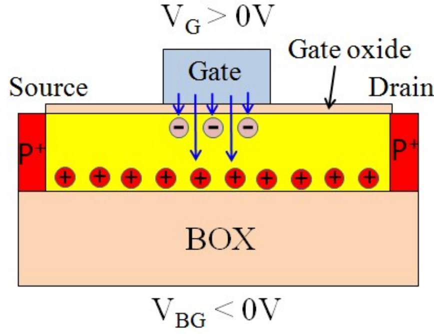


Fig. 1. Schematic view of the proposed ICPD structure and explanation of the interface coupling effect.

Figure 2(a) shows the simulated $I_D$-$V_{BG}$ characteristics of the device under various illumination conditions. The $V_G$ is constantly biased at 1.5V and $V_D$ = -1V. Compared to the device in the dark, the device under the illumination of a light source with wavelength of 520 nm and intensity of 50 μW/cm$^2$ has lower $|V_{th}|$ and thus higher current. The photoresponsivity can be derived as $(I_{ph}-I_{dark})/P$, where the Idark and Iph are the drain currents without and with illumination respectively, and P is the optical power received by the active region of the device. The relation between responsivity and $V_{BG}$ is shown in Fig. 2(a). The responsivity increases dramatically and peaks at about -9V with a value over $2.2\times10^4$ A/W. After, the responsivity (R) reduces with further reduction of $V_{BG}$ below -9V. Such R-$V_{BG}$ trend is similar to the transconductance curve of a conventional MOSFET. This can be easily understood, since the increase of current can be estimated as $|V_{th}|$ shift multiplying the transconductance.

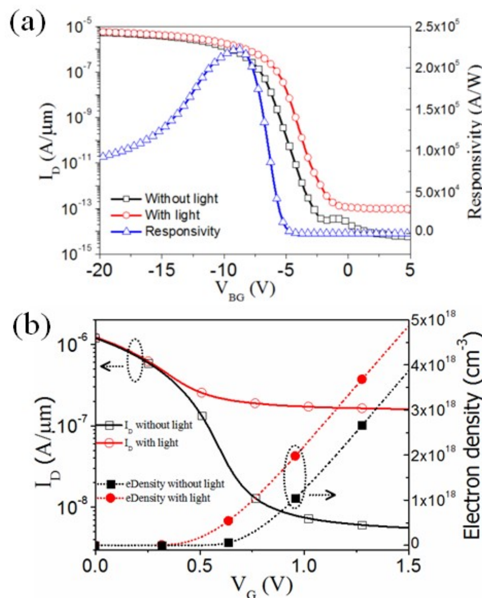


Fig. 2. (a) Simulated $I_D$-$V_{BG}$ and (b) $I_D$-$V_G$ curves of the ICPD in the dark and under illumination. Its corresponding responsivity and electron concentration can be observed in Fig. 2(a) and (b) respectively.

A high enough $V_G > 0$ is the key for the operation of this device, as indicated in Fig. 2(b). Figure 2(b) compares the ID-VG curves of the device in the dark and under illumination. Under low VG, the difference of the current in these two cases is negligible. As $V_G$ increases, the dark current reduces dramatically due to interface coupling effect, whereas the current under illumination decreases only slightly. Thus, a big difference and high photocurrent is obtained under high $V_G$. This effect can be understood by comparing the electron concentration at the top interface between these two cases, see Fig. 2(b). The electron concentration is extracted at 1 nm below the top interface. As $V_G$ increases, the electron concentration increases accordingly, due to the top surface inversion. However, the electron concentration under illumination is apparently higher than that in the dark, especially at high $V_G$. This is due to that a high $V_G$ can effectively accumulates the photogenerated electron under the top interface and reduces the interface coupling.

Unlike conventional SOI photodetector, in which the thinning of top Si layer reduces the responsivity due to poor quantum efficiency, the ICPD has higher responsivity with reduced top Si thickness. Figure 3(a) compares the R-$V_{BG}$ relation of ICPDs with 3 different Si thickness ranging from 100 nm to 300 nm. The peak of the responsivity significantly increases from $1.5\times10^5$ A/W to $4.5\times10^5$ A/W as Si layer reduces from 300 nm to 100 nm. This is due to the increase of interface coupling effect in thin Si layer device, which is helpful to enhance the internal gain. Figure 3(b) shows the trend of the peak responsivity as Tsi decreases from 300 nm to 20 nm. The responsivity

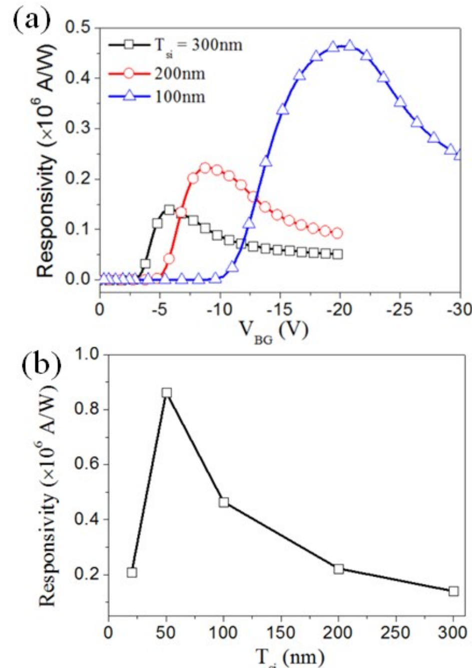


Fig. 3. (a) Responsivity – $V_{BG}$ relations of the ICPDs built on various Tsi. (b) The trend of peak responsivity as Tsi decreases from 300 nm towards 20 nm.

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increases to almost $9\times10^5$ A/W with $T_{si}$ of 50 nm, then falls down dramatically as $T_{si}$ reduces to 20 nm. Since the operation of ICPD needs coexistence of electron and hole in the channel, too thin of a Si layer induces high recombination between top electron and bottom hole, and thus reduces the internal gain.

### 3. Device fabrication and characterization

A simplified process has been developed to fabricate the device. As scheme in Fig. 4 shows, the process starts with a SOI wafer with 200 nm top Si layer and 500 nm BOX, same as that in the simulation. After, the active region of the device is formed by ultra-violet (UV) photolithography followed by wet etching. The source and drain contacts are further defined by photolithography and thermal evaporation of Aluminum (Al). Instead of using doping, we use direct Schottky contact in source/drain to avoid implantation and high temperature anneal for dopant activation. This is helpful to not only reduce the cost but also obtain good compatibility with other novel semiconductor materials, such as 2-D material and polymer which cannot be effectively doped and favor low temperature process. After the definition of source/drain contact, atomic layer deposition (ALD) is used to deposit a 30 nm $Al_2O_3$ on the device as the gate oxide. The top gate is placed at the middle of the source/drain gap by e-beam lithography and thermal evaporation of Al. The Al is used as the top gate instead of transparent material, such as indium tin oxide (ITO), due to the availability of material in our lab. Figure 5 shows the top-down view of the fabricated device by scanning electron microscope (SEM). The device has 10 µm width and 10 µm gap between source and drain electrodes. The gate width is 1 µm as the inset zoom-in image shows.

The fabricated device is measured with a Keithley 4200 transistor analyzer. The $I_D$-$V_{BG}$ curves under various $V_G$ and illumination conditions are shown in Fig. 6. From Fig. 6, it can be seen that the $|V_{th}|$ of the back channel is largely increased as $V_G$ increases from -1V to 1.5V. This indicates a strong interface coupling effect, where the top gate effectively tunes the $|V_{th}|$ of the back channel. Under illumination of a light source with wavelength of 520 nm and intensity of 700 µW/cm$^2$, the $|V_{th}|$ of the device with $V_G$ = 1.5V is largely reduced. However, with $V_G$ = -1V, the illumination does not cause apparent change to the $|V_{th}|$ and current. As explained previously in part. 1, a high $V_G$ is needed to effectively accumulate the photoelectron and achieve large $|V_{th}|$ shift. With $V_G$ = -1V, the photogenerated electron cannot be accumulated under the top interface, and thus it does not cause apparent $|V_{th}|$ shift.

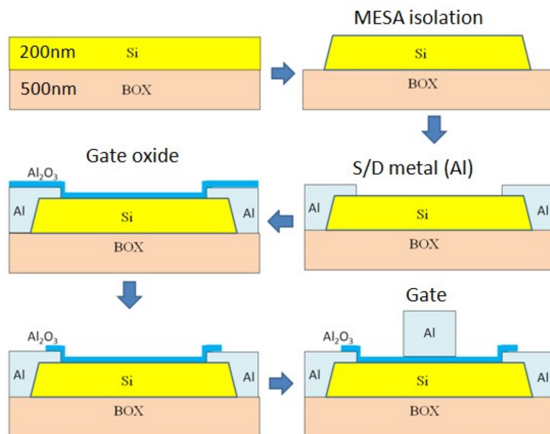


Fig. 4. Schematic view of the fabrication flow of the proposed ICPD.

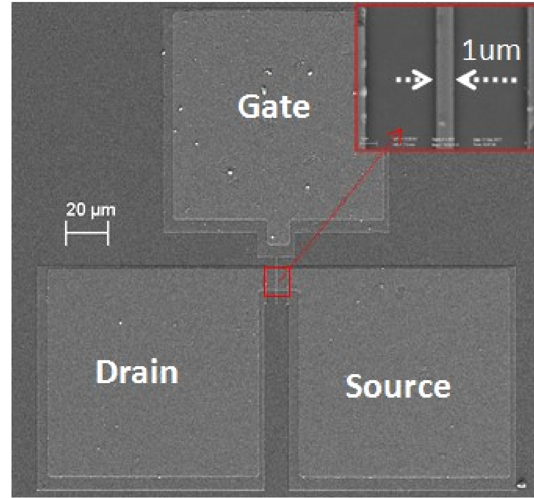


Fig. 5. SEM image of the top-down structure of the fabricated ICPD. The inset image shows the details of the gate.

The responsivity of the device is extracted and presented in Fig. 7 with both linear and logarithm scales. Similar to that predicted by our TCAD simulation in Fig. 2(a), the responsivity increases dramatically from $V_{BG}$ = -5V and reaches over $10^4$ A/W at $V_{BG}$ = -12V. The curve in logarithm scale reveals an exponential increase of responsivity with $V_{BG}$ > -5V. This is due to that the transconductance of MOSFET increases exponentially in the subthreshold region.

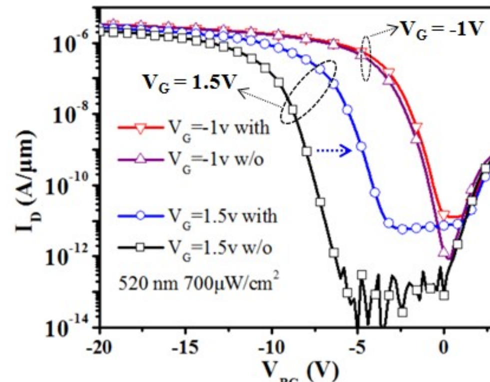


Fig. 6. $I_D$-$V_{BG}$ characterization of the fabricated ICPD under various $V_G$ and illumination conditions with $V_D$ = -1V.

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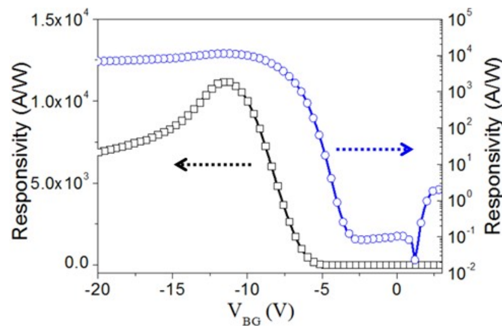


Fig. 7. Relation between responsivity and $V_{BG}$ of the device in linear and logarithm scales.

## 4. Conclusions and Summary

In this work, we have proposed a novel photodetector on SOI substrate using interface coupling effect. TCAD simulation has been used to confirm the physics of the device and revealed that the responsivity of the device increases with reduced top Si layer thickness, opposite to the trend in other SOI based photodetectors. A simplified process has been developed featuring low process temperature and no need of doping. The photoelectric measurements on the device agrees well with the TCAD simulation and demonstrate a responsivity up to $10^4$ A/W.

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