A highly sensitive photodetector based on deep-depletion effects in SOI transistors

M. Arsalan[1], XY. Cao[1], BR. Lu[1],YF. Chen[1], A. Zaslavsky[2], S. Cristoloveanu[3], M. Bawedin[3] and J. Wan[1]*
[1]State key lab of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai, China
[2]Department of Physics and School of Engineering, Brown University, Providence, RI 02912, USA
[3]IMEP-LAHC, INP-Grenoble/Minatec, CS 50257, Grenoble 38016, France
Email: jingwan@fudan.edu.cn

***Abstract* — This work reports a transient effect found in silicon-on-insulator (SOI) substrates, where the current of the transistor changes slowly under a back-gate voltage pulse. We show via TCAD simulation that the operating principle arises from deep depletion in the SOI substrate. This effect is further used for photodetection with extremely high 7.3×10^6 A/W responsivity and signal read-out without need for charge transfer.**

I. Introduction

A remarkable advantage of FD-SOI MOSFETs is that the backgate voltage (V_{BG}) can be used to flexibly tune the threshold voltage (V_t) and switch the circuit between high performance and low-power consumption modes [1, 2]. The back-biasing capability is also useful for new device concepts (memory, photodetectors, *etc.*) [3-6].

Photodetectors built on SOI can be fully compatible with SOI-based CMOS and photonic circuits, and have found many applications in low-power optical communication and imaging system [6-9]. Various SOI photodetectors, such as *p-n* diodes [7], embedded *p-n* diodes in substrate [8, 9], and transistors with high internal gain have been demonstrated [6].

In this work, we report and analyze an interesting transient effect triggered by backgate pulsing. TCAD simulation is conducted to confirm that the transient is due to the deep depletion in the SOI substrate. We further exploit this effect for photodetection with high responsivity and no need of charge transfer.

II. Device Fabrication and Characterization

Figure 1 (a) shows the top-down scanning electron microscope (SEM) image of the fabricated device. The fabrication starts from a SOI substrate with 145 nm buried oxide (BOX) and 100 nm top Si layer, as indicated in Fig. 1(b). The substrate is p^--doped at 10^{15} cm^{-3}. Mesa isolation is formed by photolithography followed by wet etching in TMHA. The source/drain electrodes are formed by photolithography and deposition of 10/110 nm Cr/Au by evaporation. The contacts are annealed at 300 °C for 10 min. The length (gap between source and drain) and width of the channel are both 10 μm, see Fig. 1(a). The device is essentially a Schottky barrier FET (SB-FET) controlled by the backgate V_{BG}, similar to a pseudo-MOSFET [1, 2].

Figure 1(c) shows the transfer characteristics of the device from direct-current (DC) measurements as V_{BG} is swept from 5 to –20 V. The device behaves like a conventional *p*-type MOSFET because the workfunction of Cr is close to the valence band of the Si. However, when the device is subjected to a sharp V_{BG} pulse, with V_{BG} changed from 0 to –18 V over 0.1 ms at fixed V_D = –1 V, the drain current I_D does immediately follow V_{BG} pulse but rather reaches its static value of –3.2 μA/μm in about 150 s, see Fig. 1(d). Similar backgate-induced transients in MOSFETs and pseudo-MOSFETs have been reported earlier and used to determine the carrier lifetime [10].

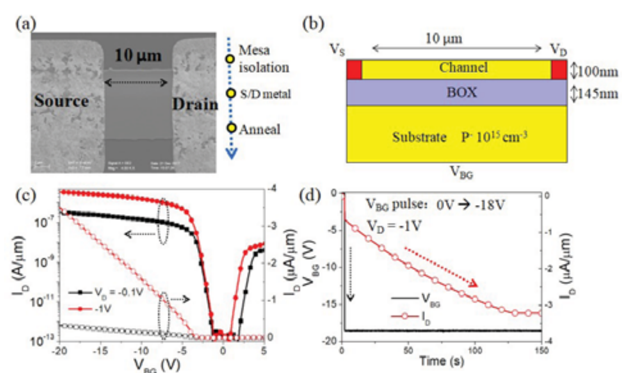

Fig. 1 (a) Top-down SEM image of the fabricated device; (b) schematic device cross-section: 100 nm top Si, 145 nm BOX and gate length of 10 μm; (c) static I_D–V_{BG} characteristics of the device in linear and log scales; (d) evolution of I_D with time under a rapid V_{BG} pulse from 0 to –18 V.

III. TCAD simulation and operation principle

TCAD simulation in Synopsys Sentaurus is performed to understand the discrepancy between DC and transient characteristics. Schottky-Read-Hall (SRH) model is used for carrier generation and recombination. In order to match our experimental results in Fig. 1(d), the carrier lifetime was set to 0.1 ms. Figure 2(a) shows the evolution of I_D under a V_{BG} pulse of –18 V. The simulation reproduces the experimental results very well, with negative I_D increasing slowly to its steady-state value instead of following the V_{BG} pulse.

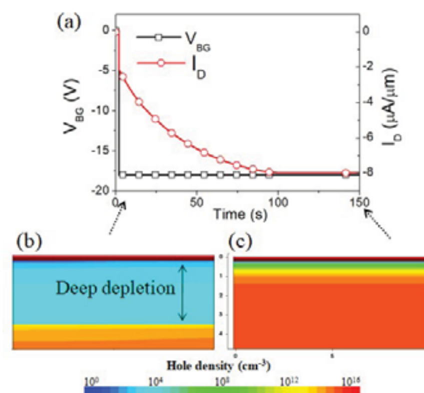

Fig. 2 TCAD simulation showing (a) evolution of drain current under V_{BG} pulse and the hole density after (b) 2 s and (c) 150 s.

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The hole density distributions are compared between time $t = 2$ s, soon after the V_{BG} pulse down to –18 V, and $t = 150$ s when I_D reaches the steady-state value. As shown in Fig. 2(b), a deep depletion region extending down to 3.5 μm is formed in the substrate right after the V_{BG} pulse. The thermal generation in deep depletion region produces electrons, which accumulate at the BOX/substrate interface and reduce the potential, as shown in Figs. 2(c) and 3. The reduced potential in the substrate gradually induces holes in the Si film. Figure 3 compares the evolution of hole and electron densities at channel/BOX and BOX/substrate interfaces, respectively. The increase in the channel hole density follows the same trend as that of substrate electron density, and causes the gradual increase in I_D.

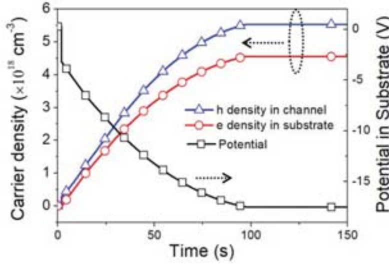

Fig. 3 Evolution of electron density and potential at the BOX/substrate interface, and hole density at channel/BOX interface

IV. PHOTODETECTION APPLICATION (EXPERIMENT)

The generation of electrons in the substrate can accelerated by light, leading to an efficient photodetector. Figure 4 shows the measured drain current under various illumination conditions applied after the V_{BG} is pulsed to –18 V between $t = 20$ and 120 ms. In the dark, I_D remains low, since the thermal generation produces only a few electrons on a 100 ms time scale. On the other hand, the current increases linearly during a light pulse from $t = 30$ to 110 ms at a fixed wavelength $\lambda = 520$ nm, as a function of light intensity, see Fig. 4(a). This is due to the generation of photoelectrons in the depletion region, which accumulate under the BOX/substrate interface and induce holes in the top Si channel, increasing I_D as explained in section III. Higher light intensity generates more photoelectrons, and thus causes a more rapid increase in I_D.

Figure 4 (b) shows the relation between light intensity and I_D for two different light pulse durations. With a light pulse that is 80 ms long, the negative I_D increases linearly as a function of light intensity in the 0–4 μW/cm^2 range. As enough photoelectrons accumulate, the deep depletion region is eventually eliminated. When the photo-generation and thermal recombination are balanced, the electron density and I_D saturate for an 80 ms light pulse of intensity higher than 4 μW/cm^2.

A responsivity as high as 7.3×10^6 A/W is obtained with a 80 ms light pulse. A shorter light pulse generates fewer photoelectrons, leading to lower responsivity. There is a trade-off between responsivity and response time that can be tuned by changing the duration of the light pulse (or the V_{BG} pulse). The deep depletion and charge accumulation in substrate are similar to that in a charge coupled device (CCD) image sensor. However, in our device, the photoelectrons in the substrate are directly read out by the current of the transistor in the top Si layer without need for charge transfer.

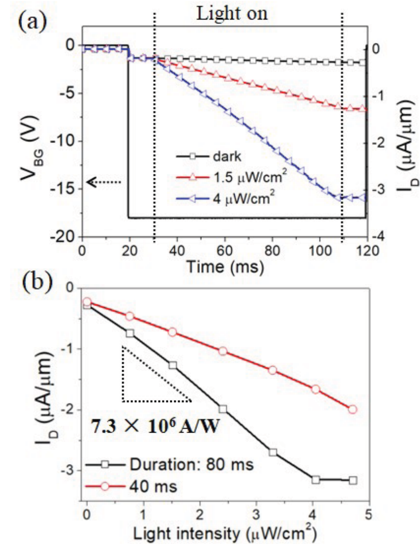

Fig. 4 (a) Evolution of I_D under various illumination conditions. (b) I_D at the end of the pulse *vs.* light intensity for pulses of 40 and 80 ms duration.

V. OPERATION OF SENSOR ARRAY (SIMULATION)

This photodetection mechanism can be further extended to the application of detection array, i.e. the image sensor. CMOS sensor is typically used for image detection, where each cell consists of one photodiode and three extra transistors in order to achieve random access. A novel one-transistor active pixel sensor (1T-APS) is proposed based on the aforementioned operation mechanism. In order to selectively read a certain cell, top gate is added to the device so that it looks similar to a conventional MOSFET, see Fig. 5. The shallow trench isolation (STI) with 500 nm depth and 200 nm width is used to isolate different cells.

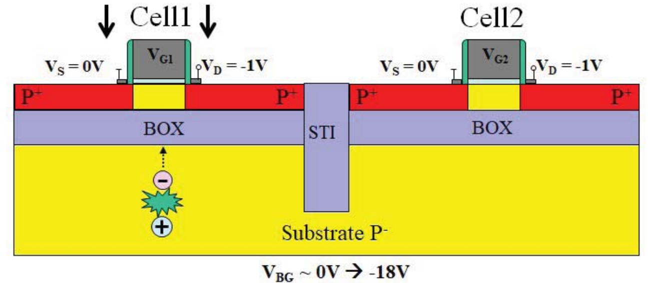

Fig. 5 1T-APS image sensor array with 2 cells based on the deep depletion mechanism in SOI substrate

In order to evaluate the ability of random access and crosstalk between different cells, TCAD simulation is performed with the simplified 1T-APS structure with 2 cells. After the reset of the sensor cells with a V_{BG} pulse from 0V to -18 V, cell1 is exposed to a light pulse with 80 ms duration and various intensities. Thereafter, voltage pulse is applied on top gates of cell1 and cell2 in order to read the optical signal. Figure 6 shows the waveforms of the gate voltage pulses and read-out current. As the gate1 (V_{G1}) pulses from 1 V to – 1 V, cell 1 is turned on and the output drain current shows apparent modulation by the light intensity. However, no apparent change of current is seen as negative V_{G2} pulse turns on the cell2. This is attributed to that only cell1 is exposure to the light signal while cell2 is kept in dark, so that photoelectrons accumulate under the

BOX and modulate drain current only in cell1. This demonstrates the integration of all functions needed in a APS sensor, including photosensing, charge integration, signal amplification and random access in just one transistor. Besides, the crosstalk with STI isolation is negligible between different cells, see the read-out current in cell2 under various light intensities in Fig. 6.

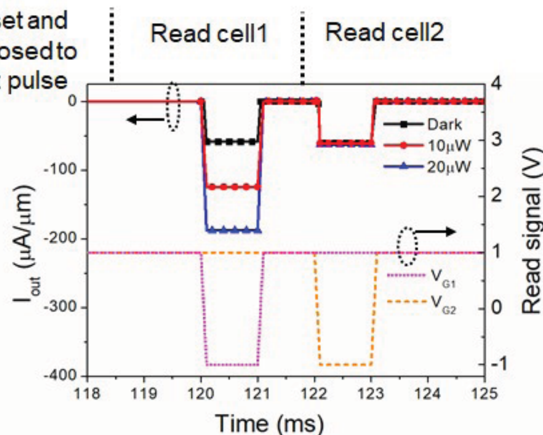

Fig. 6 Waveforms of the applied gate voltage pulses and readout current of the 1T-APS image sensor with 2 cells

Conclusions

A significant current transient effect in SOI transistors due to deep depletion under backgate pulsing has been investigated experimentally and confirmed via TCAD simulation. This deep depletion effect is modulated by light and can be used for photodetection with high responsivity and *in-situ* readout of the photoelectron charge. A concept of 1T-APS image sensor is further proposed with this deep depletion mechanism in SOI. TCAD simulation demonstrates the operation of the sensor array and negligible crosstalk between different cells. Compared to conventional CMOS sensor which needs one photodiode and three transistors in each cell, the 1T-APS based on the deep depletion mechanism in SOI substrate needs only one transistor and thus has higher fill factor.

Acknowledgments

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