Photodiode with Low Dark Current Built in Silicon-on-Insulator by Electrostatic Doping

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***Abstract*—In this work, we demonstrate experimentally a novel photodiode built in the silicon-on-insulator (SOI) substrate. Compared to conventional photodiode, where the p-n junction is formed by diffusion or ion implantation, the p-n junction in our work is formed by electrostatic doping induced by top and bottom gates. The fabricated device used for photodetection at λ = 520 nm, shows a dark current 3 decades lower than a conventional photodiode. Furthermore, the device can be switched between photodiode mode with low reverse current and resistor mode with much higher current. This unique property can be exploited in the operation of a photodetector array.**

Keywords- silicon-on-insulator; photodetector; ultraviolet; electrostatic doping

I. INTRODUCTION

Silicon-on-insulator (SOI) devices have attracted much research interest due to low leakage current, low parasitic capacitance and radiation hardness [1-5]. Compared to bulk Si, SOI-based integrated circuits (ICs) show better performance in low-power, radio frequency and memory applications [6-13]. Further, SOI-based photodiodes are promising for electronic and photonic integrated circuits (EPICs) and optical communication systems, due to their high speed and low power consumption [4, 14-21]. Even in specific application areas like aerospace, SOI devices are more popular and widely used owning to its excellent radiation resistance[22]. In SOI devices, conventional ion implantation typically used to form the photodiode p-n junction is challenging because the top thin Si layer can be severely damaged, degrading the photodiode performance in some aspects.

Previously, we have demonstrated a photodetector with a field-induced diode in the SOI substrate and obtained high responsivity [23]. In which backgate voltage(V_{BG}) is employed to induce the junction in the substrate without the need of ion implantation. Besides, the field-induced doping junction technology can be also used for light emitting[24]. In this work, a photodiode is formed in the top Si layer by electrostatic doping from the gate voltage biasing, instead of implantation. The operation principle of the device is similar to that in Hocus-Pocus diode [25], where the top and bottom gates can induce different doping levels in the channel. In our device, the source and drain doping are also removed and replaced by Schottky contacts. With appropriate gate biasing, our fabricated devices behave like standard p-n diodes with fairly low reverse current and a photo-response similar to a conventional doped photodiode. Without need for ion implantation and the following high-temperature annealing process, the electrostatically doped photodiode is advantageous in terms of lower damage to the Si layer, more flexible，lower production cost, and compatibility with novel two-dimensional (2D) and polymer semiconductors that are difficult to dope physically. Furthermore, the electrostatically doped diode can transform into a resistor with relatively low resistance by changing the gate biasing, is an import feature useful for achieving random access in a photodiode array.

II. DEVICE STRUCTURE AND FABRICATION

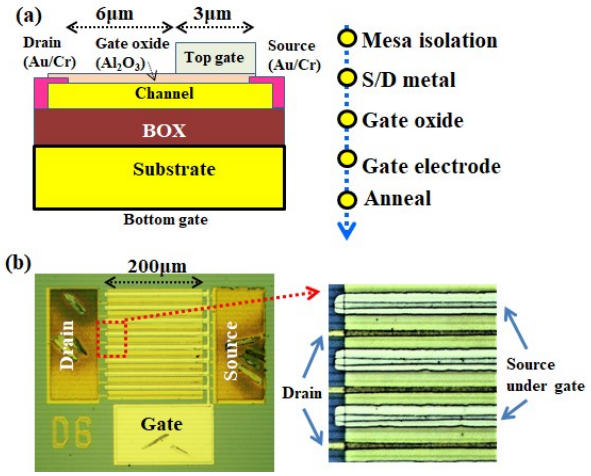

Fig. 1. (a) Schematic view and simplified fabrication process flow of the device. (b) Top-down optical view of the fabricated device.

The device is fabricated on the SOI platform with 100 nm top Si layer and 145 nm buried oxide (BOX). Figure 1(a) shows schematically the device structure and a simplified process flow. First, mesa isolation is achieved by photolithography and wet etching in diluted tetra-methylammonium hydroxide (TMAH). The source/drain regions are then formed by depositing a 10 nm Cr/80nm Au metal stack using thermal evaporation to form the Schottky contacts to the undoped Si channel. Thereafter, a 30 nm Al_2O_3 layer is deposited as the gate oxide via atomic layer deposition (ALD) system. The gate electrode is formed by lithography followed by metal deposition and lift-off. The 3 μm long gate

overlaps the source and leaves a 6 μm gap between drain and gate, see Fig. 1(a). Throughout the whole fabrication process, there is no ion implantation involved as in a conventional manufacturing process.

Figure 1(b) shows the top-down view of the fabricated device under an optical microscope. The device has interdigitated source/drain electrodes with 16 fingers on top of a 200 × 200 μm active region. The stripes of gate fully cover the source electrodes in order to simplify the fabrication.

III. Electrical Characterization

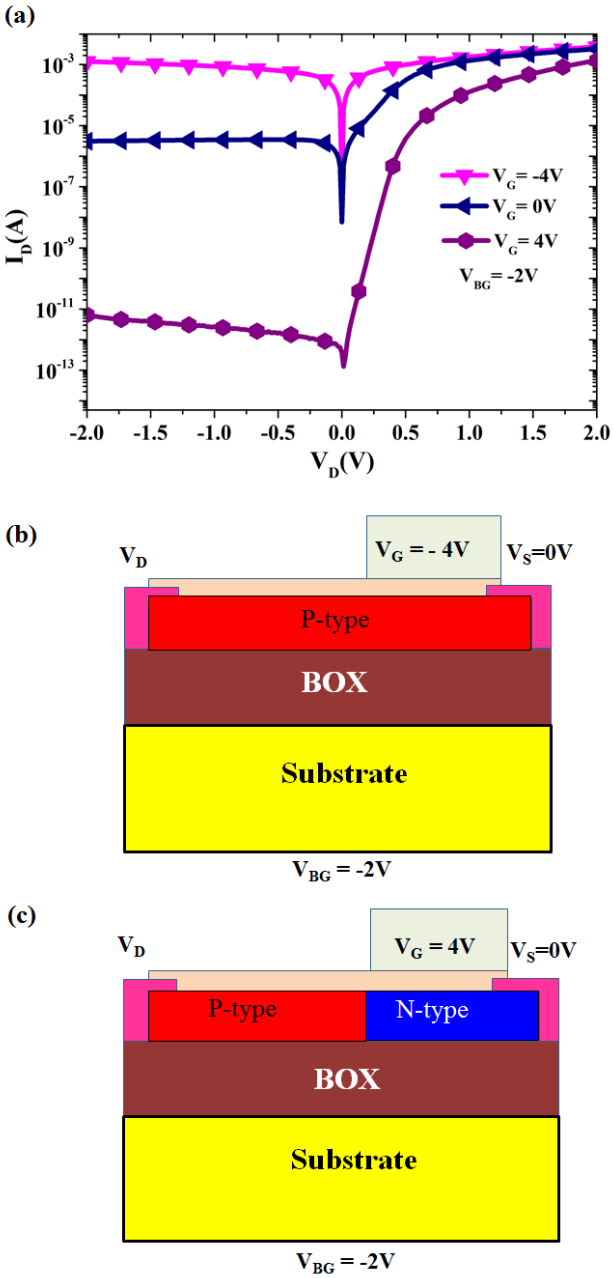

Fig. 2. (a) I_D-V_D characteristics of the fabricated device *vs.* top gate bias V_G at V_{BG} = –2 V. Schematic view of device operated as (b) a resistor and (c) a p-n junction diode.

The I_D-V_D characteristics are measured under a constant V_{BG} = –2 V as a function to top gate bias V_G, see Fig. 2(a). For V_{BG} = –2 V and V_G = –4 V, the entire channel is electrostatically doped p-type due to the negative top and bottom gate biasing. Since the Cr/Au electrode has a workfunction close to Si valence band, the device behaves as a resistor with almost symmetrical I_D-V_D characteristics, as illustrated in Fig. 2(b). However, as V_G is increased to 4 V, the device turns into a conventional p-n diode with ~10^8 rectification between the forward and reverse current. The positive V_G induces n-doped region under the front gate and forms a p-n junction with the region uncovered by the front gate, see Fig. 2(c).

The reverse current at $V_D < 0$ is significantly reduced from 1 mA to around 1 pA at V_D = –1 V. This corresponds to a dark current density of 2.5 nA/cm^2, which is 3 decades lower than that reported in ion-implanted SOI photodiodes [26]. We attribute the lower dark current to the undamaged Si layer that does not see ion implantation in our device.

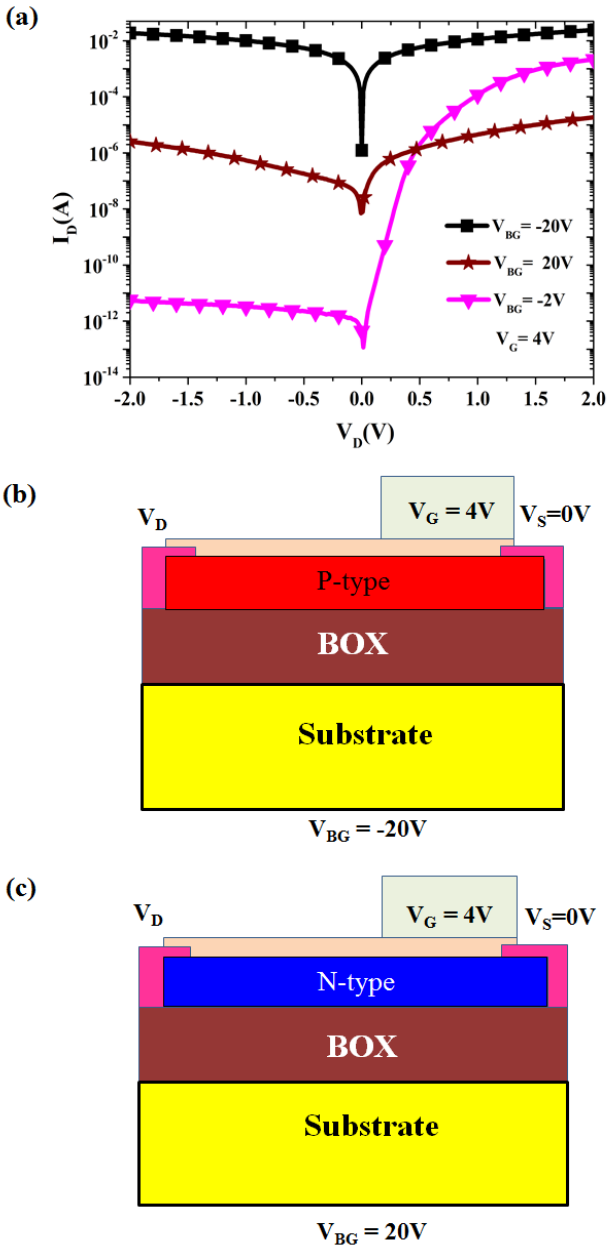

Fig. 3. (a) I_D-V_D characteristics of the fabricated device *vs.* backgate bias V_{BG} at V_G = 4 V. Schematic view of device when (b) V_{BG}= -20V and (c) V_{BG}= 20V.

Besides, we investigate the output characteristics of this device at a fixed V_G = 4 V under various backgate voltages. V_{BG} is biased at -20 V, -2 V, and 20 V with a constant V_G= 4

V, as shown in Fig. 3(a). When V_{BG} is negatively biased as low as -20 V, the channel is induced into p-type. Though V_G = 4V is applied on front gate, the channel under the front gate is still converted to p-type due to the much lower V_{BG}, schematically shown in Fig. 3(b). Thus, the device behaves as a resistor under this bias. On the other hand, as V_{BG} = 20V is applied, the whole channel is electrostatically doped to n-type, see Fig. 3(c). As a consequence, the device also produces nearly symmetrical output curve without significant rectification behavior, as shown in Fig. 3(a). We notice that the drain current under V_{BG} = -20V is much higher than that under V_{BG} = 20V. This is due to that the workfunction of Cr/Au in source/drain is close to the Si valence band, and thus it has lower contact resistance with the hole channel than that with the electron channel. Only a moderate V_{BG} = 4V is able to electrostatically form the p-n diode in the channel.

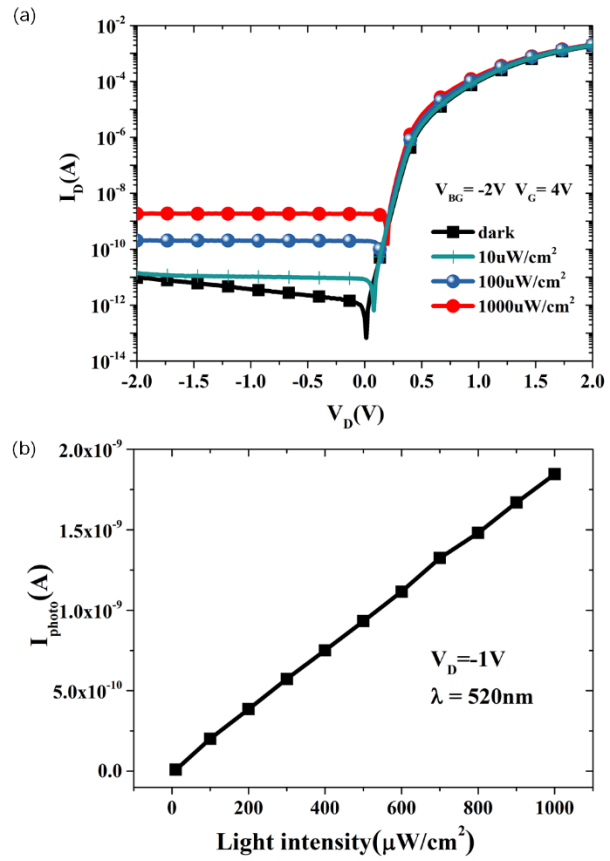

Fig. 4. (a) I_D-V_D characteristics of the device under λ = 520 nm light as a function of intensity up to 1000 μW/cm^2. (b) The relation between photocurrent and light intensity under the light with 520 nm wavelength when V_D= -1 V.

The extremely low dark current of the electrostatically doped p-n diode in SOI is very attractive for photodetection, as it improves the signal/noise ratio and detectivity of the photodiode. Figure 4(a) shows the same device measured under various illumination intensities with a light of 520 nm wavelength. The reverse current clearly increases with higher illumination intensity. As in a conventional photodiode, the open-circuit voltage (V_D when I_D = 0) shifts towards positive V_D values in proportion to the light intensity. Due to the low dark current, the photocurrent is almost 10 times higher than the dark current even with light intensity down to 10 μW/cm^2, indicating an excellent signal/noise ratio.

In Fig. 4(b), we explore the change of photocurrent under a fixed reverse bias of V_D = -1V. As the light intensity increases from 0 to 1000 μW/cm^2 with a step of 100 μW/cm^2, the photocurrent increases to almost 1.8 nA with very good linearity. The responsivity of the device extracted from the slope in Fig. 4(b) reaches 8.5 mA/W, equivalent to a quantum efficiency of 2.1%. This fairly low responsivity is mainly due to the thin top Si layer of SOI, which absorbs light weakly. However, the responsivity increases to 27.2 mA/W under λ = 300 nm illumination corresponding to a quantum efficiency of 11.2%, thanks to better absorption of shorter wavelengths in the top Si layer. This property might be attractive for ultraviolet (UV)-selective detection.

IV. Conclusion

A novel p-n diode has been demonstrated in SOI, in which the p and n regions are formed by electrostatic doping via the top and bottom gate biasing. Due to the absence of implantation damage, the device shows extremely low reverse-bias dark current down to 2.5 nA/cm^2. It has been used for photodetection and shows good signal/noise ratio. Besides, the device can be switched between resistor and diode modes. The flexibility is very useful in the photodetection array, in which a specific cell can be selected by the top gate.

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