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Dynamic Coupling Effect in Z^2-FET and Its Application for Photodetection

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ABSTRACT In this paper, the application of the zero subthreshold swing and zero impact ionization FET (Z^2-FET) for photodetection is studied with TCAD simulation. Dynamic coupling effect is utilized to form carrier injection barriers in the partially depleted silicon-on-insulator (PD-SOI) film. Photoelectron accumulation at the front gate interface lowers the hole injection barrier and modulates the turn-on voltage. The light-triggering threshold of the device can be tuned by the front gate voltage, which controls the injection barrier height. We explore two operation modes suited to different applications, and demonstrate the operation of a one-transistor active pixel sensor array. Unlike other image sensors that utilize only one type of carrier, the Z^2-FET photodetector uses photo-generated holes to induce high electron currents through internal amplification, leading to a high sensitivity of up to 1.8×10^5 e-/(lux·s).

INDEX TERMS Z^2-FET, dynamic coupling effect, silicon-on-insulator, photodetection.

I. INTRODUCTION

The ultra-thin body and buried oxide (UTBB) silicon-on-insulator (SOI) technology is extensively used in advanced integrated circuits (ICs) due to its remarkable advantages [1]–[4]. Devices on SOI substrates obtain performance gains via reduced parasitic capacitance and leakage current, as well as threshold voltage tuning [5], [6]. Thus, the SOI platform is of great interest in many application fields, such as SOI-based electron-photonic integrated circuits (EPICs) and next-generation systems-on-chip with low power consumption and high speed [7]–[9]. Besides, thanks to their high tolerance to transient radiation effects, SOI substrates are also favored in aerospace applications [10]. Other applications, such as optical communication, image sensing, and photodetection are also widely explored in SOI because of high radiation hardness, as well as compatibility with SOI electronics and photonics [11]–[14]. Thus, photodetectors based on various operation mechanisms, using diodes, transistors and interface coupling effects (ICPDs) have been demonstrated in SOI technology [15]–[18].

Developed in fully depleted SOI (FD-SOI), the Z^2-FET naturally retains many of the above-described advantages of SOI-based devices. The Z^2-FET is a forward-biased p-i-n diode partially covered with a top gate. Based on the band-modulation operation mechanism, it shows pronounced sharp-switching characteristics [19], [20]. Essentially, the band modulation in Z^2-FET triggers a positive feedback between the flow of carriers and their injection barriers, achieving outstanding electrical performance with low subthreshold swing and high I_{ON}/I_{OFF} ratio [21]. Besides, the Z^2-FET exhibits gate-controlled hysteresis in its output characteristics. Thanks to these unusual properties, the Z^2-FET has shown promise in a series of applications, such as electrostatic discharge (ESD) protection [22], [23], dynamic random access memory (DRAM) [24], [25], and novel flash memory [26].

In this work, we extend the application of the Z^2-FET to photodetection, systematically studied with TCAD simulation in Synopsys Sentaurus. Instead of using an FD-SOI substrate, partially-depleted SOI (PD-SOI) with a thicker T_{Si} top Si layer is exploited to improve light absorption. The dynamic coupling effect [27] is investigated and utilized in the Z^2-FET to rebuild carrier injection barriers. Under illumination, photogenerated electrons accumulate under the top

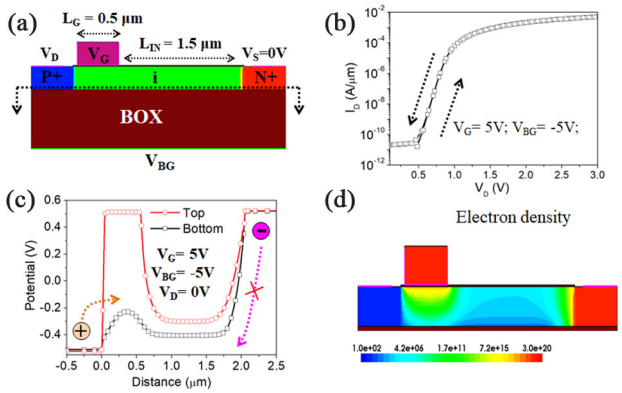

FIGURE 1. (a) Schematic view of the simulated Z^2-FET with L_G = 0.5 μm, L_{IN} = 1.5 μm, 200 nm top silicon film (T_{Si}) and 500 nm buried oxide (T_{BOX}). (b) Simulated output characteristics with forward and backward sweeps under V_G = 5 V and V_{BG} = −5 V. (c) Potential barriers along the channel direction near the top and bottom interfaces. (d) Electron density distribution in the device, showing electron inversion under the front gate.

gate and screen the coupling. This lowers the carrier injection barrier and eventually triggers the positive feedback that turns on the device. We explore different operation modes suited to multiple potential applications and study the impact of photo-generated hole density and T_{Si} on sensitivity. Finally, we simulate one-transistor active pixel sensor (APS) array operation and benchmark our device against other reported CMOS-based photodetectors.

II. DYNAMIC COUPLING EFFECT IN PD-SOI Z^2-FET

A. DEVICE STRUCTURE AND OPERATING PRINCIPLE

The conventional Z^2-FET is built on the FD-SOI platform with an ultrathin top Si layer (T_{Si}). The front and back gate biasing effectively creates hole and electron injection barriers next to the drain and source electrode respectively. However, an FD-SOI substrate with ultra-thin T_{Si} suffers from poor light absorption efficiency. The absorption depth in Si is larger than 200 nm in the visible and increases with wavelength λ [28], so T_{Si} needs to be relatively large for effective photodetection purpose. At the same time, a thicker T_{Si} will reduce front-gate V_G control of the bottom interface, thereby degrading the turn-on voltage V_{ON}. As a result, our simulations use a compromise value T_{Si} = 200 nm for illumination at λ = 500 nm. A systematic study of T_{Si} in our Z^2-FET photodetector is presented in Section VI.

Figure 1(a) shows the partially-depleted Z^2-FET structure we use in our simulations, with T_{Si} = 200 nm as in [15], [18] and a p-type doping concentration of 10^{15} cm^{-3}. The front gate length is L_G = 0.5 μm and intrinsic length (region not covered by front gate) is L_{IN} = 1.5 μm. The thicknesses of BOX and front-gate oxide are 500 and 10 nm respectively (making it possible to apply V_G up to 9 V without gate leakage). Our simulations use electric field and doping-dependent mobility, and SRH thermal generation-recombination with a doping-dependent carrier lifetime of 0.1 μs. A direct current (DC) simulation of the output characteristics by sweeping V_D from 0 to 3 V and then back, at fixed V_G = 5 V and V_{BG} = −5 V is shown in Fig. 1(b). In contrast to the FD-SOI based Z^2-FET with ultrathin T_{Si}, the output characteristics of the device based on PD-SOI substrate show neither sharp switching nor gate-controlled hysteresis. This can be understood by investigating the potential profiles along the channel direction extracted at 1 nm below the gate oxide/channel interface (top interface) and 1 nm above channel/BOX interface (bottom interface), shown in Fig. 1(c). The electron injection barriers due to negative V_{BG} are high at both top and bottom interfaces. In contrast, the hole injection barrier created by V_G is high only at top interface, but not at the bottom interface. This is due to the screening of the $V_G > 0$ electric field by inversion electron charge accumulating at the top interface, as shown in Fig. 1(d). As a result, the top gate exerts little control over the bottom interface of the channel compared to $V_{BG} < 0$, leading to a very low hole injection barrier and eliminating the feedback process and the sharp switching characteristics.

To rebuild the hole injection barrier and recover sharp switching characteristics, we use the dynamic coupling effect triggered by voltage pulse applied on the front gate. In Fig. 2(a), a V_G pulse rising from 0 to 5 V in 0.1 ms is applied 0.1 ms after the V_{BG} is pulsed to −5 V. Under a fast V_G pulse, thermal generation is too slow to produce enough electrons at the top interface and screen the electric field. This non-equilibrium condition results in deep depletion in T_{Si}, which rebuilds the hole injection barrier, as shown in Fig. 2(b). This is essentially the same dynamic coupling effect used in SOI-based MOSFETs for DRAM applications [27]. With the rebuilt hole injection barrier, a forward and backward sweep of V_D from 0 to 3 V, shortly after the V_G pulse, shows output characteristics with sharp switching and hysteresis, similar to that of a conventional Z^2-FET, see Fig. 2(c).

B. IMPACT OF BIAS PULSE SEQUENCE ON INJECTION BARRIERS

The sequence of the V_G and V_{BG} pulses plays a key role in rebuilding the carrier injection barriers, as illustrated in Fig. 3. An unexpected result is observed when order between V_G and V_{BG} pulses is swapped, see Fig. 3(b). In this case, V_G is first pulsed up to 5 V, followed by a V_{BG} pulse down to −5 V 0.1 ms later (reversing the sequence of Fig. 2(a)). As shown in Fig. 3(c) this reversed sequence fails to rebuild the potential barrier, see the red curve in Fig. 3(c), and suppresses the sharp switching and hysteresis, as shown in Fig. 3(d).

This can be understood by investigating the electron current density distribution inside the device. In the reversed bias sequence, the earlier positive V_G pulse draws electrons from the N$^+$-doped source into the channel. These electrons flow to the front gate interface, as shown in Fig. 4(a). As a result, the accumulated electrons reach equilibrium (steady-state) condition, screen the control from the top gate on the bottom interface, and eliminate the sharp switching. With the correct sequence, the $V_{BG} < 0$ pulse is applied

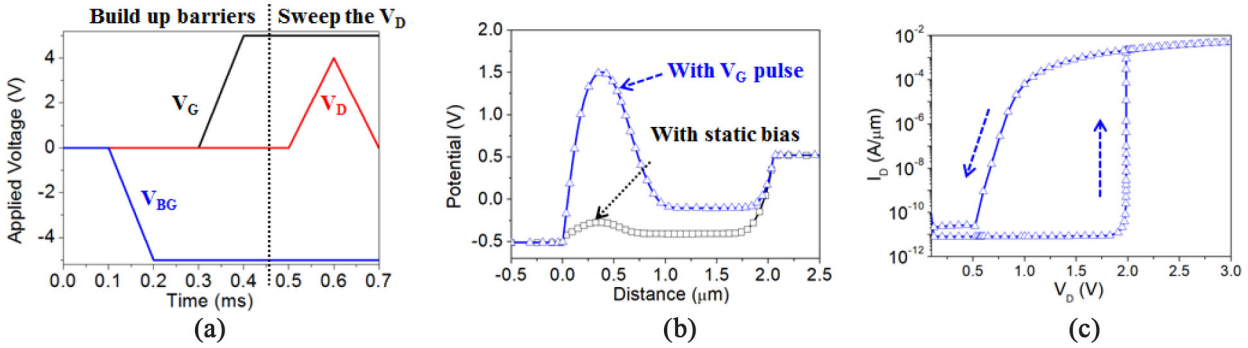

FIGURE 2. (a) Bias waveforms applied to the device. (b) Comparison of potential distributions of the device under static and pulsed front-gate biasing. (c) Simulated I_D-V_D characteristics of the device under pulsed V_G operation.

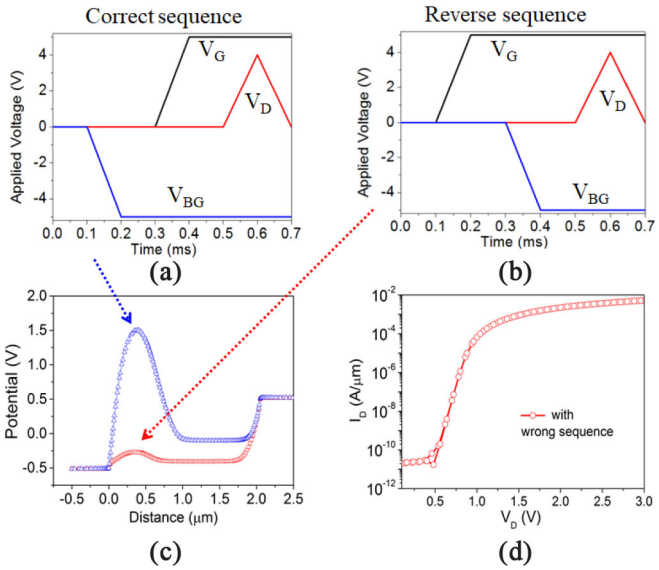

FIGURE 3. (a) Correct and (b) reversed pulsed sequences for dynamic coupling effect in PD-SOI Z^2-FET. (c) Comparison of potential profiles from two different bias sequences. (d) I_D-V_D characteristics of the reversed sequence, showing no sharp switching.

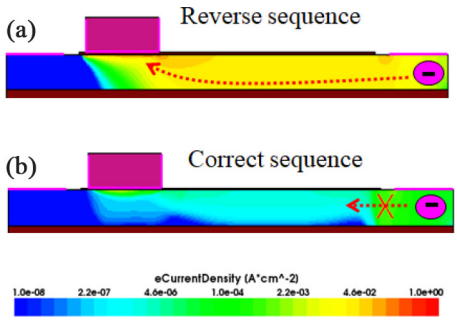

FIGURE 4. Electron current density and flow during the ramp of V_G when the device is biased with (a) reversed and (b) correct pulse sequences of Fig. 3.

first, preventing electron injection into the intrinsic region, so that the $V_G > 0$ pulse cannot attract electrons from the doped source, as shown in Fig. 4(b). Without electrons at the front interface, V_G builds up the barrier at the bottom of the film successfully.

C. IMPACT OF V_G MAGNITUDE ON INJECTION BARRIERS

Besides the bias pulse sequence, the front gate voltage can also impact the barrier height and thus modulate the turn-on voltage (V_{ON}) of the device. In a conventional FD-SOI Z^2-FET, V_{ON} is linearly controlled by front gate voltage V_G. The PD-SOI Z^2-FET based on dynamic coupling exhibits a similar dependence on V_G magnitude. Figure 5(a) compares potential profiles along the bottom interface for three different V_G pulses of 3, 5, and 7 V respectively. With higher V_G pulses, the hole barrier gets taller. As a result, the turn-on voltage V_{ON} also increases, see Fig. 5(b). Figure 5(c) summarizes the impact of V_G on hole injection barrier height and V_{ON}. As V_G magnitude increases from 3 to 9 V, the hole potential barrier increases linearly from 1.6 to 2.7 V and the V_{ON} increases linearly from 1.5 to 2.8 V. The modulation ratio R between V_{ON} and V_G is 0.22. The gate-controlled sharp-switching characteristic of the PD-SOI Z^2-FET is helpful for photo- detection. It can directly convert the exposure to a well-defined V_{ON} without additional amplification. Further, the high internal gain responsible for sharp switching also leads to the high sensitivity of the Z^2-FET photodetector, as discussed in detail in Sections V and VIII of this paper.

III. APPLICATION OF Z^2-FET IN PHOTODETECTION

The dynamic coupling effect that forms the hole injection barrier can interact with photo-generated carriers, and thus be used for photodetection. Figure 6 shows the impact of light on our PD-SOI Z^2-FET. In our simulation, a ray tracing model is used for the optical part of the simulation using conventional boundary conditions. The optical generation is based on a quantum yield with step function model and default complex refractive index of Si is used in the Synopsys Sentaurus. The device is first biased with V_{BG} and V_G pulses to form the carrier injection barriers. Shortly thereafter, the device is exposed to light pulses of various intensities at the fixed $\lambda = 500$ nm wavelength, see Fig. 6(a).

The evolution of I_D is recorded after illumination, as shown in Fig. 6(b). In the dark, the device remains in the

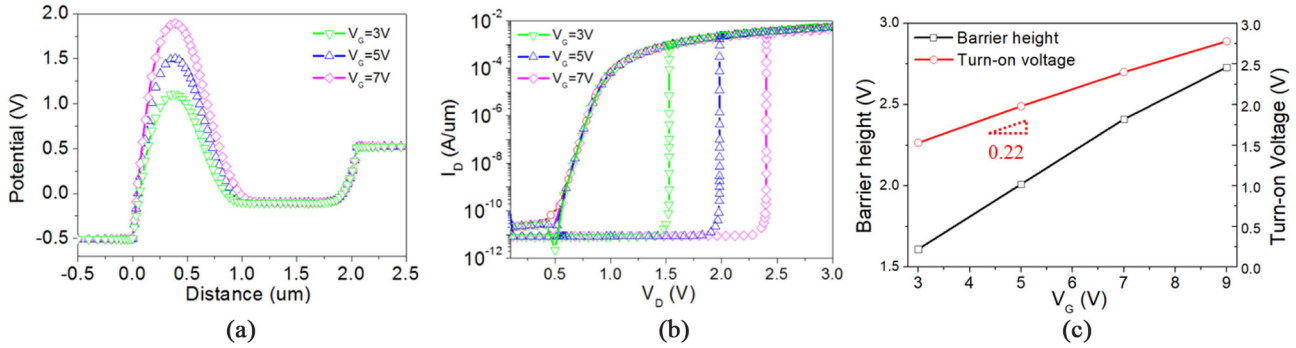

FIGURE 5. (a) Potential profile at the bottom channel *vs.* V_G; (b) I_D-V_D characteristics at fixed V_G values; (c) impact of V_G on barrier height and turn-on voltage V_{ON}.

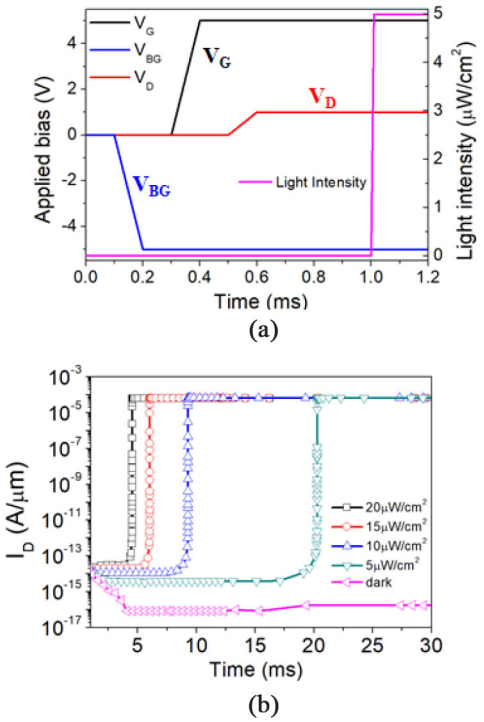

FIGURE 6. (a) Waveforms of applied V_G, V_{BG}, V_D and light exposure. (b) Evolution of I_D after light pulses of various intensities.

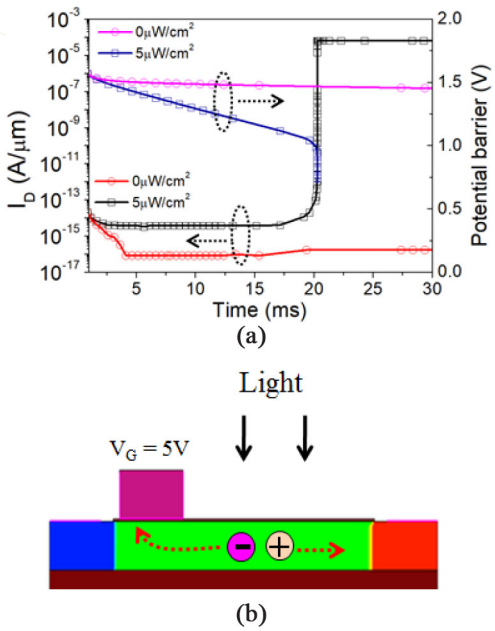

FIGURE 7. (a) Evolution of hole injection barrier and I_D in the dark and under illumination. (b) Schematic flows of photo-generated electrons and holes.

I_{OFF} state, since V_D = 1 V is too low to overcome the injection barrier built by V_G pulse. However, as the device is exposed to the light, it turns on after a certain exposure time, see Fig. 6(b).

As the light intensity is increased from 5 to 20 μW/cm^2, exposure time to turn on the device falls from 20 to about 5 ms. This indicates that the PD-SOI Z^2-FET built on PD-SOI substrate is sensitive to the light exposure and can be used for photodetection purpose.

The photoresponse of the Z^2-FET can be understood by investigating the evolution of hole injection barrier with the exposure time. Figure 7(a) compares the time-dependent hole barriers in the dark and under a light of intensity 5 μW/cm^2. In the dark, the hole barrier is high (∼1.5 V) and does not change in this short period of time (30 ms), due to the slow thermal generation of electrons. However, under illumination, photo- generated electrons are attracted by the positively biased V_G and accumulate at the front gate interface, as schematically shown in Fig. 7(b). This gradually reduces the hole injection barrier at the bottom interface due to screening of V_G by the photoelectrons at the front gate interface. As the hole injection barrier is lowered from 1.5 V to 1 V, the holes from the P$^+$-doped drain are injected into the channel and trigger the feedback process. This collapses both barriers and turns on the device sharply, see Fig. 7(a).

The duration of the exposure that is needed to turn on the device (turn-on time) can be modulated by the V_G. Higher V_G induces a taller potential barrier, and thus a longer exposure time is needed to generate enough photoelectrons and turn on the device. This can be observed in Fig. 8(a) where

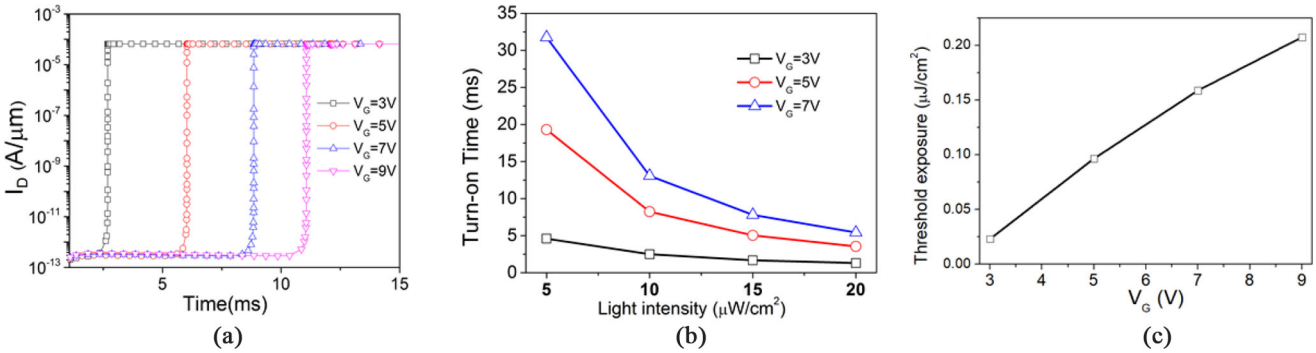

FIGURE 8. **(a) Evolution of I_D under a fixed light intensity of 15 μW/cm² and various V_G from 3 V to 9 V. (b) Relation between exposed light intensity and exposure time to turn on the device as a function of V_G. (c) Modulation of threshold exposure that triggers the device by applied V_G under a light intensity of 5μW/cm².**

the turn-on time increases from about 2.5 ms to about 11 ms as V_G increases from 3 V to 9 V.

The turn-on time is also modulated by the light intensity, since higher light intensity generates photoelectrons faster and thus shortens the exposure time needed. Figure 8(b) shows the relation between turn-on time and light intensity as a function of V_G. In fact, it is the exposure that determines the density of generated photoelectrons and thus the turn-on time of the device. Figure 8(c) summarizes the relation between threshold exposure dose needed to turn on the device and the applied V_G pulse. The threshold exposure increases almost linearly as V_G increases. Thanks to the sharp switching and high I_{ON} of the Z^2-FET, this property might be attractive in application as exposure-triggered switch [29]–[31].

IV. AN ALTERNATIVE OPERATION MODE

Though the Z^2-FET used as a sharp switch triggered by a light exposure dose is attractive, in many other applications, such as image sensing, the exposure dose needs to be read out as an output voltage. Conventional CMOS active pixel sensors combine one photodiode with three transistors in order to achieve several functions: photosensing, charge integration, buffer amplification needed to converts the photoelectrons to an output voltage, and random access for sensor array operation. Here, we demonstrate that the Z^2-FET is actually a single-transistor active pixel sensor (1T-APS), where only one transistor is needed to include all these functions.

In order to achieve this, an alternative operation mode is developed, where the exposure dose is read out as an output voltage. Figure 9(a) shows the waveforms of the applied bias pulses and the light pulse. Similar to the exposure-triggered switch discussed above, V_{BG} and V_G pulses are applied sequentially to build up the injection barriers. The device is then exposed to a light pulse of 5 ms duration (simulating the shutter in an image sensor) with light intensity varying from 5 to 20 μW/cm². After exposure, a V_D pulse up from 0 to 3 V is applied in order to read out the exposure dose. Figure 9(b) shows the I_D-V_D output characteristics of the device under various illumination conditions. In the dark, a $V_D \sim 1.8$ V is needed to turn on the device due to high hole barrier formed by $V_G = 5$ V pulse. However, V_{ON} is markedly reduced after exposure to a light pulse. This is due to the accumulation of photoelectrons under the gate, resulting in a lower potential barrier. The reduction of V_{ON} with exposure dose is almost linear, see Fig. 9(c). The sensitivity S_1 of the sensor is defined as the change of V_{ON} with exposure per unit area. It reaches 9 V per μJ/cm² under $V_G = 3$ V and increases to 13.4 and 14 V/(μJ/cm²) under $V_G = 5$ and 7 V, respectively. This sensitivity is higher than that of conventional CMOS sensors, considering the small device area, see Section VIII below. At higher V_G, the V_{ON}-exposure curve shifts upward due to higher injection barrier, as shown in Fig. 9(c).

Unlike conventional CMOS active pixel sensors, where additional transistors are used to convert the photoelectrons to an output voltage, Z^2-FET photodetector converts the light exposure directly to a voltage signal (V_{ON}) with high output current. Besides, the Z^2-FET can achieve random access with the combination of V_G and V_D pulses during the read phase, which has been discussed in the context of its DRAM capabilities [32], [33]. Thus, the Z^2-FET can be used as a one-transistor active pixel sensor, which is more compact than a conventional CMOS sensor.

V. IMPACT OF PHOTO-GENERATED HOLES ON THE SENSITIVITY

Classical image sensors, such as charge-coupled devices (CCDs) and CMOS sensor, employ only photoelectrons, whereas the photo-generated holes are typically discarded. In the Z^2-FET sensor, the photo-generated holes play a key role. Figure 10(a) compares the relation between exposure rate and V_{ON} for two different simulations. Both use $V_G = 7$ V and other bias values as in Fig. 9(a). In one simulation, both photoelectrons and holes are included, and the sensitivity reaches 14 V/(μJ/cm²). In the other simulations, the holes are ignored, which suppresses the exposure-induced shift of V_{ON} and lowers the sensitivity to only 0.85 V/(μJ/cm²).

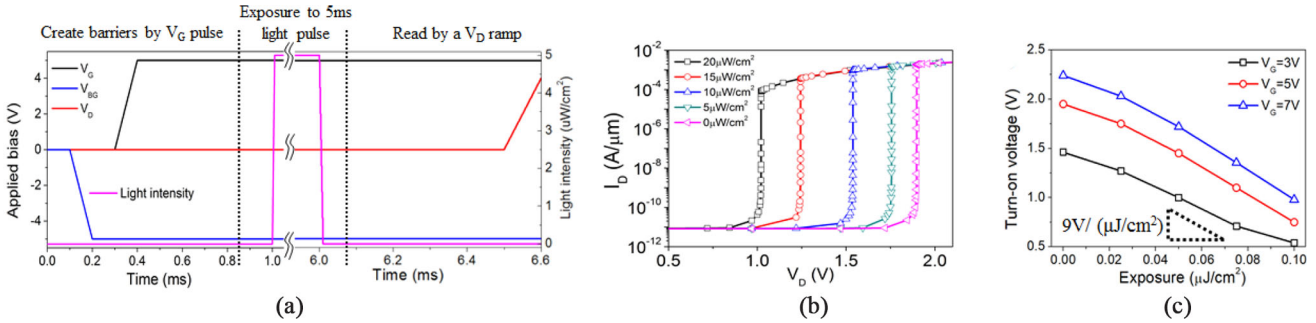

FIGURE 9. (a) Waveforms of applied bias and light pulses on the Z^2-FET for the alternative operation mode. (b) I_D-V_D characteristics during the ramping up of V_D after exposure to light of various intensities. (c) Relation between turn-on voltage and exposure under various V_G.

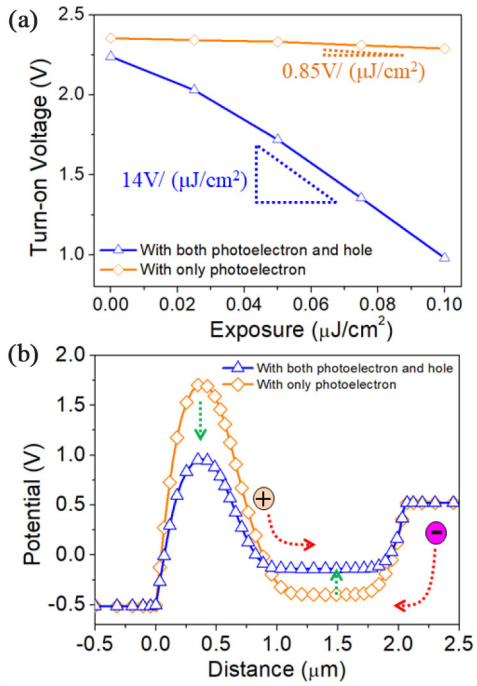

FIGURE 10. (a) Comparison of V_{ON}-exposure relations between simulations in which photo-generated holes are or are not included. (b) Comparison of potential profiles between these two cases, and schematic view of photo-generated holes flowing to the intrinsic region and electrons injected out of the N$^+$-doped source.

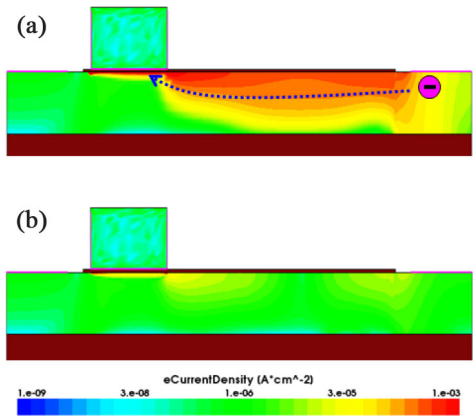

FIGURE 11. (a) Electron current density considering both photo-generated electron and hole, and (b) that considering only photoelectron.

In order to understand this mechanism, potential profiles at the bottom interface are compared in these two cases at $t =$ 6.1 ms after exposure to the light. Apparently, compared to the simulation with photoelectrons only, the device with both photoelectrons and holes shows reduced hole and electron injection barriers, see Fig. 10(b). In fact, the photogenerated holes flow to the intrinsic region and raise its potential. This reduces electron barrier and causes the injection of electrons from the N$^+$-doped source into the channel. The electrons then flow to the front-gate interface, as shown in Fig. 10(b).

The electron current density has been simulated to confirm this aspect. Figure 11 compares the electron current density extracted at the middle of exposure ($t = 3.5$ ms) in simulations that do and do not consider the holes. After electron-hole pair generation, high electron current is observed in Fig. 11(a) flowing from N$^+$ doped source to the front-gate interface. This markedly reduces the V_{ON} and thereby leads to high sensitivity. In contrast, in simulations including only electrons, the electron current is very low, see Fig. 11(b).

In fact, the comparison in Fig. 10(a) reveals that photo-generated holes play a more important role than photo-electrons in the operation of the Z^2-FET photodetector. According to the feedback mechanism in the Z^2-FET, where hole flows trigger the flow of additional electrons, the photo-generated holes flowing into the source can induce additional electron injection. Due to the internal gain, the electron injection from the N$^+$-doped source to the front interface is much stronger than direct electron photogeneration. Thanks to this internal amplification, sensitivity up to 14 V/(μJ/cm^2) is achieved even with small device area.

VI. IMPACT OF TOP SI THICKNESS ON THE SENSITIVITY

The top Si thickness T_{Si} has a major impact on the sensitivity of the Z^2-FET photodetector. Figure 12(a) compares the evolution of V_{ON} with the exposure dose in devices with three different T_{Si} values. Apparently, thinner T_{si} induces higher V_{ON} and lower sensitivity S_1. The sensitivity, extracted from the slope in Fig. 12(a), degrades from 14 V/(μJ/cm^2) down

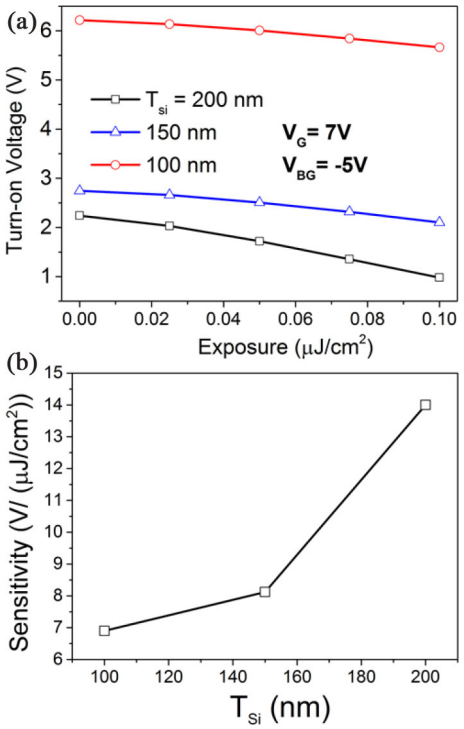

FIGURE 12. **(a) Comparison of V_{ON}-exposure relations between devices with three different T_{Si} values; (b) Sensitivity S_1 *vs.* T_{Si}.**

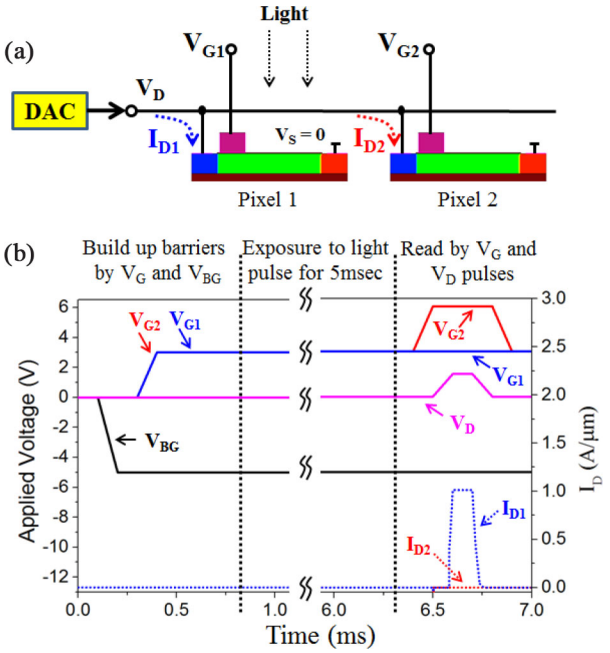

FIGURE 13. **(a) Schematic diagram of a proposed Z^2-FET APS array; (b) TCAD simulation of a 1×2 Z^2-FET array, including readout waveforms.**

to 6.8 V/(μJ/cm^2) as T_{Si} is reduced from 200 to 100 nm, see Fig. 12(b).

The dynamic coupling effect and screening by photo- generated electrons also occur in an FD-SOI Z^2-FET, as seen in the T_{Si} = 100 nm curves in Fig. 12(a). However, due to the thin top Si layer, the sensitivity is reduced. The degradation of sensitivity with thin Si layer is due to the poor absorption of light in the thin T_{Si}. Thus, a PD-SOI structure with relatively thick T_{Si} is preferable, in which the dynamic coupling effect is the dominant mechanism, as discussed in Section II. However, a T_{Si} that is too thick decreases V_{ON} due to weak coupling, and reduces the dynamic range of the detector, see Fig. 12(a).

VII. OPERATION OF SENSOR ARRAY

A conventional CMOS APS normally combines one photodiode and three transistors in order to perform photosensing, charge integration, amplification and enable random pixel access [34], [35]. Thus, conventional CMOS sensors have a complicated pixel architecture design and low quantum efficiency. However, the Z^2-FET naturally has random access capability, as discussed in its DRAM application [32], [33].

Figure 13(a) shows the architecture of our proposed Z^2-FET detector array. A 1×2 array is simulated to emulate sensors in the same row. Since pixels in the same row share the same V_D signal, the random access of a certain pixel can only be achieved by using V_G to select a certain column. Figure 13(b) shows the applied voltage waveforms and the drain currents of the two pixels. As in Fig. 9(a), V_{BG} is pulsed from zero down to −5 V, followed by V_{G1} and V_{G2} both pulsed from zero up to 3 V to build up barriers in both pixels. Then, only pixel 1 is exposed to a light pulse for 5 ms, whereas pixel 2 is kept in the dark. After exposure, in order to read photoelectrons accumulating in pixel 1 without affecting pixel 2, the V_{G2} rises up to 6 V and V_{G1} is kept at 3V. Thus, the potential barrier in pixel 2 is raised, which keeps the pixel 2 in I_{OFF} state during the readout operation by the V_D pulse. As V_D is pulsed from zero to 1.5 V, it only turns on pixel 1 in which V_{ON} has been shifted by the light exposure, see Fig. 13(b).

VIII. DISCUSSION

Compared to conventional CMOS sensors, the Z^2-FET-based APS has two unique advantages:

1) As demonstrated in Fig. 13, Z^2-FET integrates all functions, including photosensing, charge integration, amplification and random access in one transistor, and thus it is a true one-transistor APS. Thus it is more compact and design-friendly than conventional CMOS sensors.

2) Thanks to its near-zero SS, the Z^2-FET turns on sharply from I_{OFF} to I_{ON} and has a well-defined turn-on voltage V_{ON}. The exposure of the sensor can be directly read out by measuring V_{ON}. This can be achieved by using a digital-to-analog converter (DAC) to scan the V_D and register the digital value of V_D as the device is turned on, as shown schematically in Fig. 13(a). In a standard CMOS sensor, the output voltage is converted to a digital value by an analog-to-digital converter (ADC). Conventionally, design of high-performance DAC is easier than that of ADC.

The performance of the Z^2-FET photodetector obtained in our simulations is compared with conventional CMOS

TABLE 1. Performance comparison between Z^2-FET and other CMOS sensors from literature [35]–[38].

Parameter	Ref [35]	Ref [36]	Ref [37]	Ref [38]	This work
Pixel area (μm^2)	34.3	1.25	30.25	2.04	2.2
Sensitivity (e-/lux·s)	17,500	6,700	/	7922	180,000
Conversion gain (μV/e-)	30.3	63.2	20	76.6	19.4
Full well capacity (e-)	30,500	5000	25,000	9700	32,000
Operating voltage	3.3 V	2.7 V	3.3 V	2.9 V	3 V

sensors [35]–[38] collected in Table 1. The performance parameters of Z^2-FET photodetector were calculated using the device area of 2.2 μm^2. From Fig. 9(c) we find the sensitivity of Z^2-FET to be $S_1 = 9$ V/(μJ/cm^2) at $V_G = 3$ V. This can be converted into a CMOS-sensor sensitivity S in units of e-/(lux·s), defined as the number of photoelectrons that accumulate under the front gate due to 1 lux.s exposure, via:

$$S = \frac{S_1 \times C_{ox}}{R \times q}, \tag{1}$$

where C_{ox} is the capacitance of the front gate capacitor, q is the electron charge, and R is the ratio between V_{ON} and V_G, which is 0.22 according to Fig. 5(c). This leads to $S = 1.8\times10^5$ e-/(lux·s), much higher than conventional CMOS sensors, see Table 1. The high sensitivity originates from the feedback process, where the photo-generated holes trigger high electron injection as discussed in Section V.

The conversion gain G, which indicates the change in V_{ON} per photoelectron, is given by the ratio of S_1/S. We obtain G = 19.4 μV/e-, comparable to other CMOS sensors. Finally, the full well capacity (FWC), which determines the dynamic range of the sensor, can be estimated via:

$$FWC = \frac{V_G \times C_{ox}}{q}. \tag{2}$$

The FWC of Z^2-FET reaches 32000 electrons under $V_G = 3$ V, which is also comparable with other CMOS sensors.

IX. CONCLUSION

In this work, we have explored the dynamic coupling effect in the Z^2-FET built in PD-SOI substrate, which helps to rebuild the potential barriers and restore the sharp switching characteristics. This effect has further been used for photodetection, where photoelectrons accumulating at the top interface screen front gate control of the bottom interface of the channel. This reduces the hole injection barrier and triggers the device after a certain exposure. An alternative operation mode has been explored in which the exposure is directly converted to a turn-on voltage without the need for additional transistors. Unlike conventional image sensors, photo-generated holes are critical in the Z^2-FET sensor, inducing more electron accumulation and achieving sensitivity of up to $S = 1.8\times10^5$ e-/(lux·s) With high sensitivity and one-transistor compact cell architecture, the Z^2-FET is very promising for photodetection and image sensing applications.

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