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# Optimization of photoelectron *in-situ* sensing device in FD-SOI

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***Abstract* — Previously, we demonstrated a photoelectron *in-situ* sensing device (PISD) used as one-transistor active pixel sensor (APS) fabricated in advanced 22 nm FD-SOI technology. In this work, we employ TCAD simulation to systematically study the impact of device parameters on its performance. The buried oxide (BOX) thickness and active device length ($L_A$) exert a strong impact on the sensitivity and sensing range of the PISD.**

***Keywords—SOI, one-transistor, active pixel sensor, PISD***

## I. Introduction

Silicon-on-insulator (SOI) substrates have many advantages over conventional bulk Si, and thus they have been widely adopted in integrated circuits (ICs) with high operation frequency and low power consumption [1, 2] and are becoming attractive for sensor applications [3, 4]. Conventional CMOS image sensors (CISs) have been reported in SOI substrates for imaging and high-energy radiation detection [5, 6], but these devices typically combine a photodiode with three transistors to achieve photosensing, charge integration, buffer amplification and random access capability. This adds complexity to the circuit design and also reduces the effective sensing area.

Recently, we have explored the deep depletion effect in the SOI substrate and utilized it for photodetection [7]. The same operation mechanism was used to experimentally demonstrate a photoelectron *in-situ* sensing device (PISD) fabricated in advanced 22 nm FD-SOI technology [8]. The PISD integrates all functions in a single device, resulting in a one-transistor active pixel sensor (APS) with much more compact pixel structure than conventional CIS. Here we explore the impact of the device structural parameters on its performance via TCAD simulation with the goal of optimizing APS performance.

## II. Device Structure and Simulation Setup

The simulations were performed in Synopsys Sentaurus. Figure 1(a) schematically shows the simulated PISD structure. It is based on a conventional *n*-type FD-SOI MOSFET. The drain and gate of the device are biased at a constant 3.3 V and the source is connected to a $R_L$ = 5 kΩ load resistor. This essentially forms a source follower, in which the output voltage $V_{OUT}$ approximately equals the difference between $V_G$ and threshold voltage: $V_{OUT} \approx V_G - V_T$. Given a fixed 1 μm² pixel area (length $L_P$ = width $W_P$ = 1 μm), many structural parameters shown in Fig. 1(a) can impact the device performances. We focus on the role of BOX thickness ($T_{BOX}$) and active device length ($L_A$) of the sensor, while fixing the other parameters: gate oxide $T_{OX}$ = 5 nm, undoped Si channel thickness $T_{Si}$ = 6 nm, gate length $L_G$ = 50 nm, and *p*-type substrate doping $N_S = 10^{15}$ cm$^{-3}$.

When the backgate voltage $V_{BG}$ is pulsed down from zero to –5 V, a deep depletion region is formed in the substrate. Then, if the top surface is exposed to light (520 nm wavelength, 1 mW/cm² intensity), we find that $V_{OUT}$ decreases linearly as the exposure time increases, as seen in Fig. 1(b). This effect – the basis of PISD as a photodetector – is due to the increase in $V_T$ induced by photoelectrons that gradually accumulate at the BOX/substrate interface and eventually eliminate the deep depletion region [8]. After a certain exposure time, the amount of stored photoelectrons under the BOX/substrate interface reaches its maximum value, which causes the saturation of $V_{OUT}$, see Fig. 1(b).

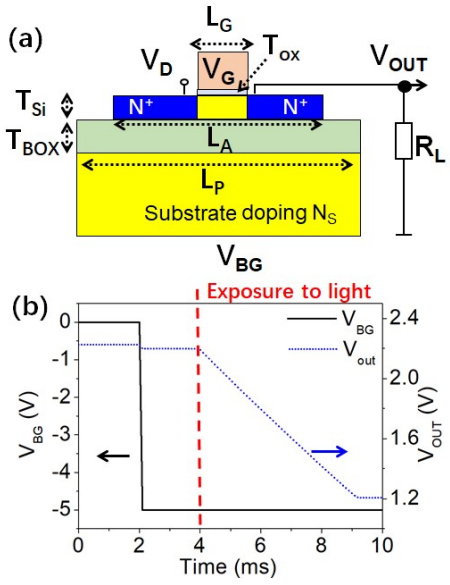


**Fig. 1** (a) Schematic view of the simulated device structure and the parameters which can impact the device performance; (b) Evolution of $V_{OUT}$ with time after $V_{BG}$ pulse applied at 2 ms and illumination applied after 4 ms.

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## III. Impact of Parameters on the PISD Performance

Figure 2(a) compares the relation between the exposure in μJ/cm$^2$ and the $V_{OUT}$ in devices with fixed $L_A = L_P = 1$ μm as a function of $T_{BOX}$. Thinner $T_{BOX}$ beneficially increases the maximum exposure before the $V_{OUT}$ saturates. The sensitivity and sensing range are plotted *vs.* $T_{BOX}$ in Fig. 2(b), where sensitivity is extracted from the slope of the linear part of the $V_{OUT}$ curve and the sensing range, defined as the total exposure needed to reduce $V_{OUT}$ by 90% of its full swing, directly determines the dynamic range of the sensor. A large increase of sensing range from 2.5 to 7.6 μJ/cm$^2$ is observed as $T_{BOX}$ decreases from 40 to 10 nm. Since it is the BOX capacitance ($C_{BOX}$) that stores the photoelectrons, the maximum photoelectron number that the device can accumulate, known as the full well capacity, roughly equals $C_{BOX} \times V_{BG}/q$. The $C_{BOX}$ increases with thinner $T_{BOX}$ and thus yields a larger sensing range without significantly impacting the sensitivity.

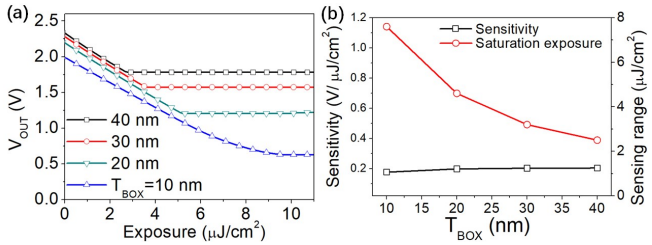


**Fig. 2** (a) $V_{OUT}$ as a function of exposure in devices with $T_{BOX}$ varying from 40 to 10 nm. (b) Sensitivity and sensing range *vs.* $T_{BOX}$.

Interestingly, reducing the active device length $L_A$ to a fraction of the pixel length $L_P = 1$ μm has significant impact on both sensitivity and sensing range. Smaller $L_A$ leads to higher sensitivity, with $V_{OUT}$ saturating faster, see Fig. 3(a). Figure 3(b) shows that the sensitivity increases from 0.2 to 1.05 V/(μJ/cm$^2$) as the $L_A$ is reduced from 1 μm down to 0.2 μm. Meanwhile, the sensing range degrades from 4.7 to 0.75 μJ/cm$^2$ with the reduction of $L_A$. Figure 4 compares the distributions of electron density in devices with $L_A = 1$ μm and 0.2 μm, after the same exposure of 1 μJ/cm$^2$. In Fig. 4(a), the photoelectrons are uniformly distributed under the BOX, as expected for $L_A = L_P$. By contrast, when $L_A = 0.2$ μm, photoelectrons generated throughout the pixel area are collected by the electric field from the top Si channel, see Fig. 4(b). Thus, the photoelectron density is higher, enhancing the sensitivity. The drawback of reducing $L_A$ is the reduction of the total $C_{BOX}$, which degrades the well capacity and hence the sensing range.

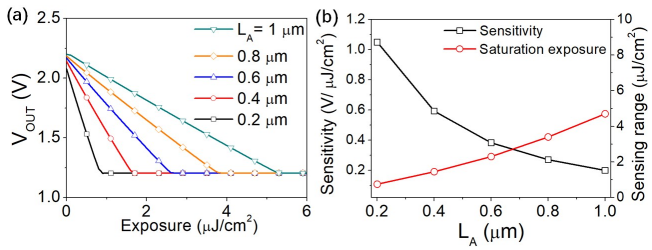


**Fig. 3** (a) $V_{OUT}$ as a function of exposure *vs.* $L_A$ in the 1 to 0.2 μm range (for $T_{BOX} = 20$ nm). (b) Sensitivity and sensing range *vs.* $L_A$.

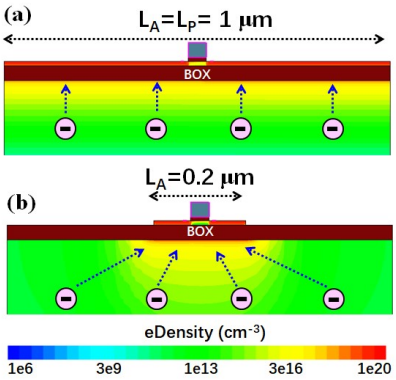


**Fig. 4** Comparison of electron density distributions in sensors with (a) $L_A = L_P = 1$ μm and (b) $L_A = 0.2$ μm, $L_P = 1$ μm. The flow of photoelectrons is indicated with arrows.

## Conclusions

We have investigated the impact of critical structural parameters on the sensitivity and sensing range of the PISD in FD-SOI. On one hand, reducing $T_{BOX}$ helps to increase the sensing range due to larger full well capacity. On the other hand, the sensitivity is markedly enhanced by shortening the active length $L_A$ within the same pixel size, thanks to higher photoelectron density at the cost of lower sensing range. This study provides guidance for the optimization of the PISD pixel performance.

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