Suppressing crosstalk in the photoelectron *in-situ* sensing device (PISD) by double SOI

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***Abstract*— In our previous work on silicon-on-insulator (SOI) photodetectors, we have used the deep-depletion effect in SOI substrates to construct the photoelectron *in-situ* sensing device (PISD). The PISD is a one-transistor active pixel sensor (1T-APS) that is more compact than conventional CMOS sensors. In this work, we study the crosstalk between different pixels in the PISD, which is severe in a conventional SOI substrate. Through TCAD simulations, the use of a double SOI (DSOI) substrate is shown to suppress crosstalk between PISD pixels. The on extra buried oxide layer completely separates the substrate into two parts which shield the movements of charges across the adjacent cells. The impact of top Si thickness and buried oxide thickness is observed.**

Keywords— DSOI, image sensor, crosstalk, TCAD simulation

I. Introduction

Silicon-on-insulator (SOI) substrates have many advantages compared to bulk Si technology, including suppressed short-channel effects and back-gate-modulated threshold voltage. The metal oxide semiconductor field effect transistor fabricated on SOI substrate has less short channel effect as compared to fabricated on bulk Si substrate[1-4]. The MOSFET built on SOI show less parasitic capacitance and low leakage current therefore it finds a lot of practical potential applications in very large-scale integrated circuits (VLSI) [4-6].

The unique features of fully depleted FD-SOI MOSFET technology such as aggressive down scaling with ultra-thin body and box structure, CMOS compatible capability, low power consumption and high RF performance circuits make it mainstream [7, 8].

Thanks to SOI structure where top thin Si film has good quantum efficiency of light photons. The buried oxide layer (BOX) between the top Si and bulk supporting Si substrate results in refractive index difference which appeals SOI substrate's application in photonics. Thus, SOI technology is widely used in electronics and photonics [9-14].

There are two main classes of image sensors compatible with silicon technology: CMOS image sensors (CISs) and charge-coupled devices (CCDs). Both of these devices have their pros and cons, but CISs have been gaining popularity due to advances in fabrication technology. However, CIS pixels combine a photodiode with extra three transistors, which results in high complexity and reduced fill factor.

Recently we have investigated the deep-depletion effect in SOI substrates and proposed its use for the photoelectron *in-situ* sensing device (PISD), which was subsequently experimentally demonstrated in advanced 22 nm FD-SOI technology [15, 16]. The PISD integrates all functionalities needed in an active pixel sensor (APS) into one transistor, including photon-electron conversion, charge integration, amplification and random access. Thus, it is more compact than conventional CISs. In this work, we show that the PISD has similar crosstalk effect as the CISs due to photoelectron migration to adjacent pixels [17-21]. To overcome this problem, we designed a modified PISD based on a double-SOI (DSOI) substrate, already available [22], where the isolation provided by the secondary buried oxide (BOX) suppresses the crosstalk between adjacent PISD pixels.

II. Operational mechanism and TCAD simulation

The device simulations were carried out in Synopsys Sentaurus. Figure 1(a) shows a schematic diagram of the PISD, where the source is connected to a load resistor of 5 kΩ. The gate and drain are biased at same constant voltage of 3.3 V. The length of source and drain extensions is 0.5 μm, respectively, and the gate length (L_G) is 30 nm. The top Si thickness (T_{Si}) is 6 nm and the buried oxide (T_{BOX}) is 20 nm thick. This scheme is essentially a source-follower circuit, in which the output voltage is $V_{out} \approx V_G – V_{th}$, where V_{th} is the threshold voltage. The substrate is lightly *p*-type doped at a concentration of 10^{15} cm^{-3}. In the dark, a negative back-gate voltage V_{BG} pulse of -5 V creates a large depletion region in the substrate that persists for seconds. In dark the V_{out} of both cells keeps low and straight, see the Fig1 (b) there is no deflection in output across the load resistor due to depletion

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region. The negative back-gate voltage evacuates the holes from substrate and create the potential for electrons. However, when the PISD is illuminated from time 4 s to 12 s, photoelectrons generated in the substrate accumulate under the BOX-substrate interface and increase the V_{th} linearly, thereby decreasing V_{out}. This effect is illustrated in Fig. 1(b), where illumination (wavelength λ = 520 nm, 2 mW/cm^2 intensity) is applied from 4 ms to 12 ms after the negative V_{BG} pulse. The change of V_{out} saturates after 7 ms, as the filling capacity of the well is completed. Figure 1(c) confirms that the Box/ depleted substrate interface is full of photoelectrons after exposure. These photoelectrons in depletion region induce the holes in upper si channel same as interface coupled effect.

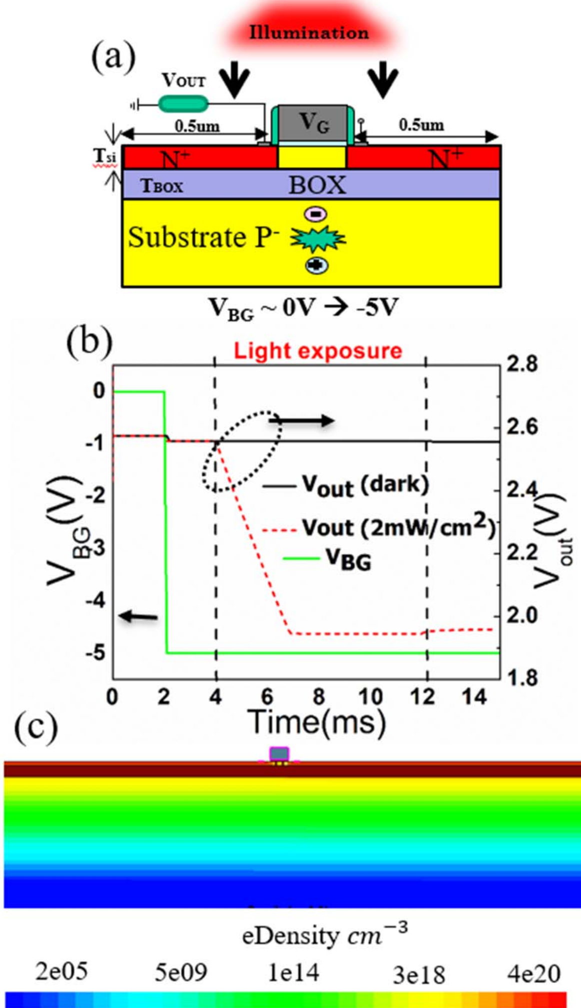

Fig. 1. (a) Schematic diagram of photoelectron *in-situ* sensing device (PISD); (b) plot of V_{BG} and V_{out} *vs.* time in the dark and under illumination; (c) simulated electron density distribution at 15 ms .

III. CROSSTALK EFFECT AND DOUBLE SOI STRUCTURE

Figure 2(a) demonstrates the structure of image sensor array. For simplicity, only two symmetric PISD pixels are simulated. The two cells are separated by shallow trench insulation (STI) and share the common substrate. In order to study the crosstalk effect, only cell 1 is illuminated. As in Fig. 1(b), the output voltage $V_{out}1$ of cell 1 decreases linearly due to photoelectron excitation, but after a short delay the same effect is observed in cell 2, even though it is kept in the dark – see the plot of $V_{out}2$ in Fig. 2(b).

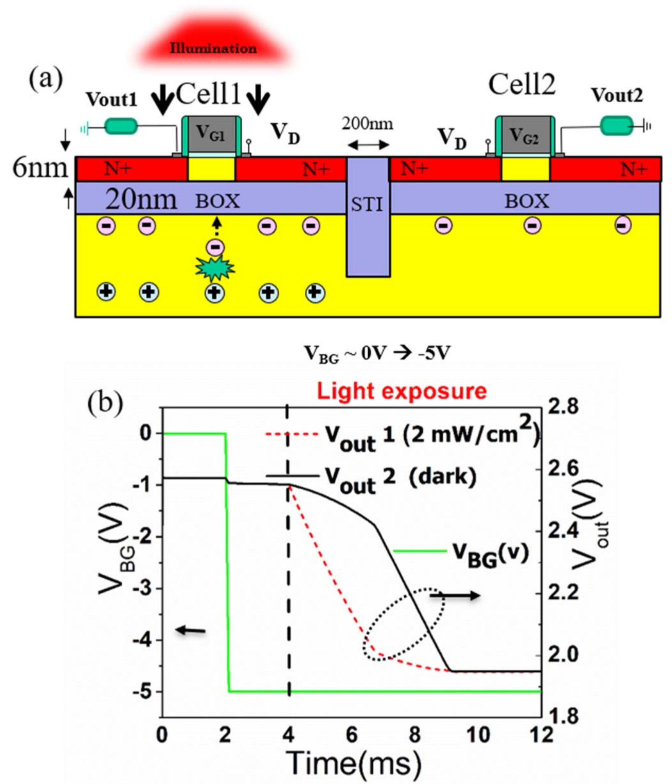

Fig. 2. (a) Schematic diagram of two cells in a sensor array; (b) evolution of V_{out} in both cells: red dashed line shows the output of cell 1 (under 2 mW/cm^2 illumination at 520 nm) and black solid line the output of cell 2 (dark).

This strong crosstalk effect indicates that some of photoelectrons generated in the cell 1 migrate to cell 2.

The photoelectrons generated under cell 1 substrate migrates towards the adjacent pixel substrate where they are not supposed to be. This migration of charges in common substrate causes the crosstalk effect. It disturbs the output of the adjacent pixels.

To suppress the crosstalk effect, we propose to build the PISD in a DSOI substrate, where the extra 20 nm buried oxide layer TBOX2 beneath the 1 µm thick Si film can completely separate the two cells, as shown in Fig. 3(a). Figure 3(b) shows that while the output voltage of cell 1 under illumination falls almost linearly, there is almost no change in the output of cell 2, indicating negligible crosstalk. The TBOX2 stops the migration of charges across the common substrate, it completely shields the photoelectrons movement and they can find the way.

Figure 4(a) is plotted for STI-isolated PISD pixels in standard SOI and shows that both cells have a high electron density in the substrate and its equally distributed, even though only cell 1 is illuminated. This is mainly due to the migration of the photoelectrons from cell 1 to cell 2, as indicated in Fig. 4(a). However, in the case of DSOI, the flow of photoelectrons from cell 1 to cell 2 is cut off by the extra BOX layer beneath the Si film, and the electron density in cell 2 remains low, as shown in Fig. 4(b). Therefore, the crosstalk effect is largely suppressed with DSOI structure.

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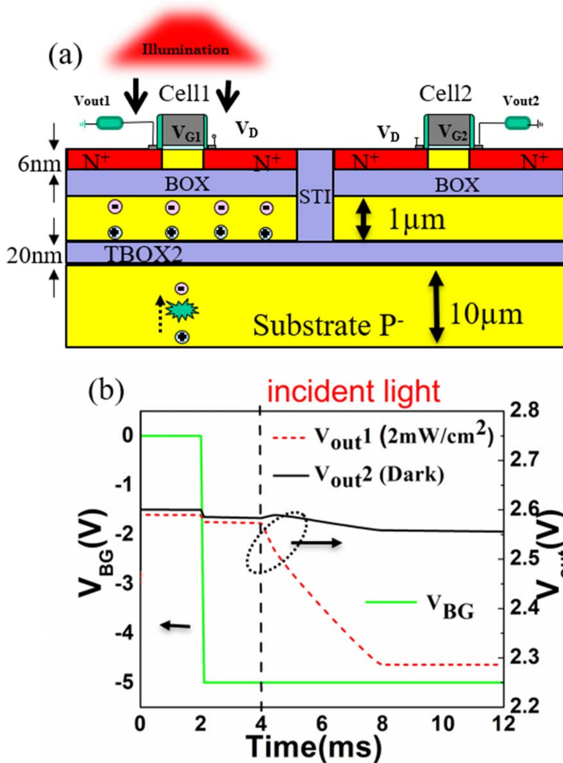

Fig. 3. (a) Schematic diagram of two adjacent PISD pixels built in DSOI; (b) evolution of output voltages from both cells as function of time, with cell 1 illuminated and cell 2 kept in the dark.

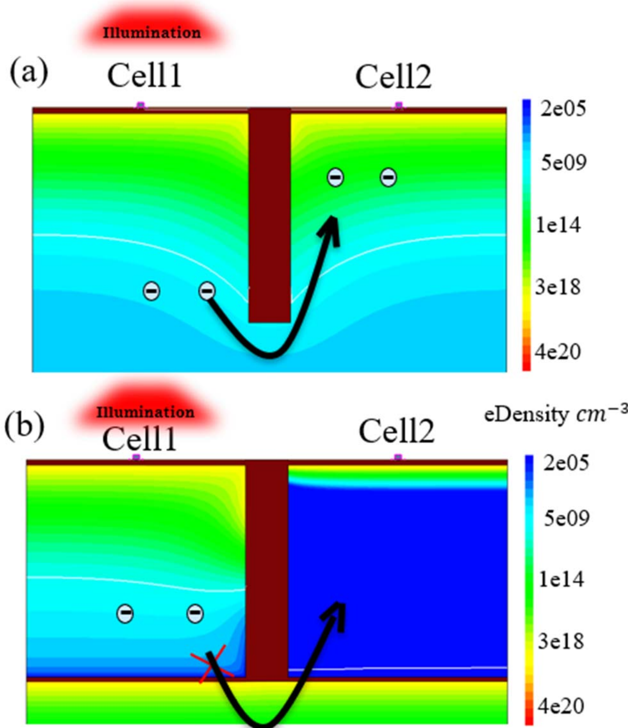

Fig. **4.** Comparison of electron density distributions in adjacent PISD pixels for STI isolation (a) and DSOI isolation (b) at 15 ms time. The STI-isolated structure in (a) shows a high electron density in both cells due to crosstalk, which is suppressed in (b) the DSOI structure.

To verify the structure optimization with DSOI substrate, we performed simulation with less advanced SOI structure to see the impact of top silicon and BOX thickness. Where the T_{Si} is 100 nm and TBOX1=TBOX2=145 nm the rest of architecture and biasing scheme is same as shown in Fig3 (a).

Figure 5 is the evolution of V_{OUT} of both cells where we see under light illumination the voltage drops across the load resistor of cell 1 does not show much deflection due to depletion region. The V_{out} 1 is nearly equal to V_{out} 2 which is under dark condition. The reason is filling well capacity has degraded with thick BOX. After light exposure few photoelectrons accumulate in BOX/substrate interface which results in weak interface coupled effect. The V_{th} does not change due to photoelectrons thereby the V_{out} does not drop.

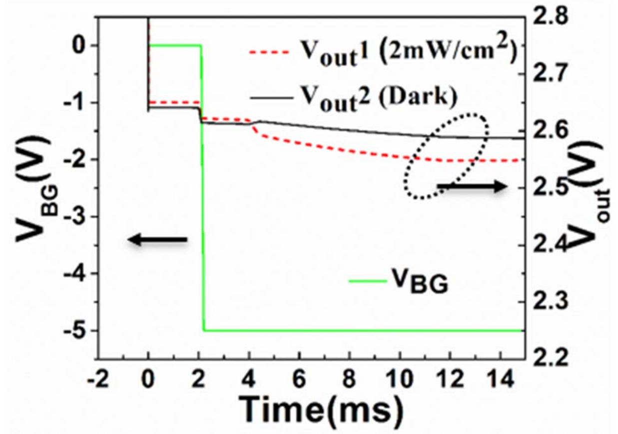

Fig. 5. Evolution of V_{out} in both cells: red dashed line shows the output of cell 1 (under 2 mW/cm^2 illumination at 520 nm) and black solid line the output of cell 2 (dark) for less advanced SOI.

Conclusions

We have proposed a double SOI structure to suppress the crosstalk effect between adjacent cells in a PISD array. The simulation results show that migration of photoelectrons between adjacent cells leads to strong crosstalk even if only one of the cells is illuminated. However, an additional BOX layer beneath the Si film used for sensing confines photoelectrons to the illuminated pixel, suppressing the crosstalk. The T_{si} and T_{BOX} thickness impact on the V_{OUT} of prosed DSOI.

Acknowledgments

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