Deep-Depletion Effect in SOI Substrates and Its Application in Photodetectors With Tunable Responsivity and Detection Range

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***Abstract*— We present an interesting transient effect found in silicon-on-insulator (SOI) transistors, where the drain current responds slowly to a back-gate voltage (V_{BG}) pulse. This transient mechanism is due to the deep-depletion region in the SOI substrate induced by the V_{BG} pulse and has been validated by experimental and TCAD simulation results. The deep-depletion characteristic can be employed for photodetection in a fully depleted (FD)-SOI MOSFET device. We have measured the photoresponse of the FD-SOI MOSFET under various light illumination conditions and studied systematically the impact of the V_{BG} pulse duty ratio, amplitude, and period on the responsivity and detection range. An optimized device structure, fabricated in an advanced ultrathin body and buried oxide (BOX) (UTBB) SOI technology, shows low operation voltage and extended detection range.**

***Index Terms*— Deep depletion effect, detection range, photodetector, responsivity, SOI.**

I. Introduction

SILICON-ON-INSULATOR (SOI) technology is now mainstream, thanks to exceptional features of fully depleted FD-SOI MOSFETs with ultrathin body and buried oxide (BOX) (UTBB): aggressive downscaling capability, superior RF performance, low-voltage operation, and high resistance to transient radiation effects [1]–[4]. Furthermore, the back-gate voltage V_{BG} provides flexibility to tune the threshold voltage when compared to conventional MOSFETs and FinFETs [5]–[9]. Finally, the different refractive indices of BOX and Si channel also make SOI substrates appealing for application in photonics [10]–[13].

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SOI-based photodetectors play an important role as a bridge connecting electronic and photonic devices and have contributed to the development of electronic–photonic integrated circuits (EPICs) [14]–[17]. However, advances in SOI-based photodetection technologies have been hindered by lower responsivity and quantum efficiency as well as difficulties in fabricating optical sensors in thin Si films [18], [19]. Recently, novel SOI-based photodetector concepts have been proposed, such as the interface-coupled photodetector (ICPD) and field-induced embedded diode with electrostatic doping [20], [21].

In this article, we report a transient effect in SOI substrate that makes the drain current of a fully depleted transistor change slowly under sharp back-gate pulse. This abnormal drain current behavior arises from a deep depletion effect in the SOI substrate triggered by V_{BG} pulse, as validated by both experiments and TCAD simulations. Furthermore, the depletion effect is modulated by light, making it useful as an operating mechanism for photodetection. By using V_{BG} pulses with various duty ratios and time periods, we successfully demonstrate the tunability of the responsivity and detection range. Finally, we present and characterize fabricated photodetectors in an advanced UTBB technology, demonstrating the reduction of the operating voltage (V_{BG}) without degrading the detection range.

II. Device Fabrication and Electrical Characteristics

Fig. 1(a) shows the top-down SEM image of a device, fabricated by a simplified process of lithography and wet etching in tetramethylammonium hydroxide (TMAH). The schematic of the device is shown in Fig. 1(b). It is essentially a Schottky barrier FET (SB-FET) controlled by a tunable V_{BG}, much like a pseudo-MOSFET [22], [23]. We used SOI wafers with top silicon thickness $T_{Si} = 100$ nm, lightly p-type doped (10^{15} cm^{-3}) bulk substrate, and BOX thickness $T_{BOX} = 145$ nm. The length and width of the channel are 10 μm. The active layer is defined by photolithography followed by O_2 reactive ion etching (RIE) to remove the residual resist, with RIE done at 50-W power, chamber pressure of 4 Pa, and O_2 gas flow of 20 sccm for 30 s. Then, the silicon etching is done by a mixture of TMAH, alcohol, and distilled

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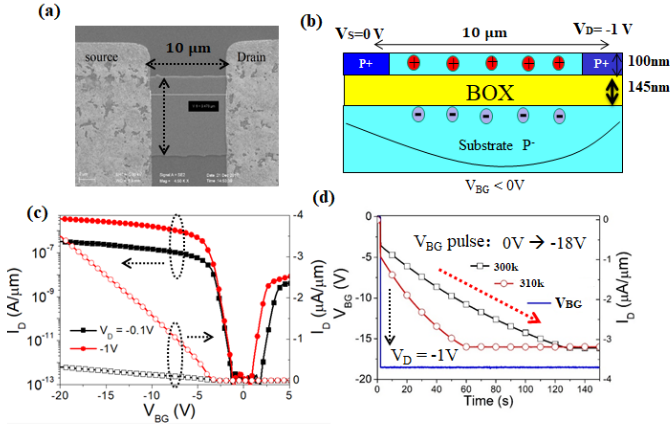

Fig. 1. (a) SEM image of the top view of the fabricated device. (b) Schematic of FD-SOI MOS device. (c) Static dc scan of drain current I_D versus back-gate voltage V_{BG}. (d) Transient drain current evolution after pulsing the V_{BG} to -18 V at $T = 300$ and 310 K.

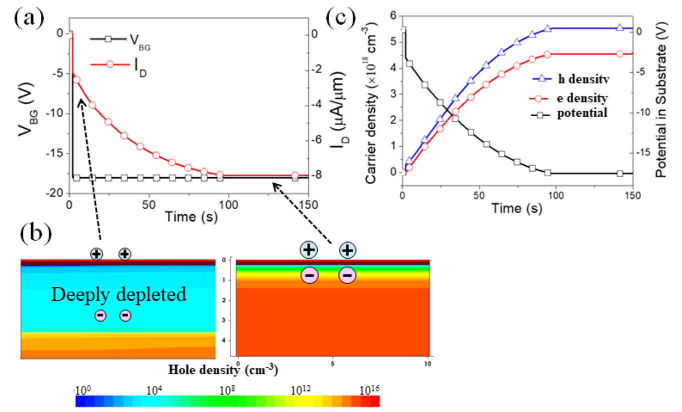

Fig. 2. TCAD simulation results showing (a) evolution of I_D against time after V_{BG} pulse. (b) Hole density distributions after 2 and 150 s. (c) Evolution of carrier densities and potential at the BOX/substrate interface.

water with a proportion of 3:2:5 at a temperature of 50 °C for 5 min. Source and drain contact regions are patterned by lithography and 10/110 nm Cr/Au metal electrodes are deposited by evaporation followed by lift-off in acetone for 10 min. Finally, the contacts are annealed at 300 °C for 5 min.

The static $I_D - V_{BG}$ characteristics show conventional p-type MOSFET behavior in which the device can be turned on by a negative V_{BG}, as seen in Fig. 1(c). A positive V_{BG} can turn on the n-type MOSFET, but the currents are much lower due to high contact resistance set by the work function of Cr (near the Si valence band).

The response of this pseudo-type MOSFET to a transient V_{BG} pulse is shown in Fig. 1(d). With the drain contact biased at a relatively low constant at -1 V and the Si substrate pulsed with a V_{BG} step voltage going from 0 to -18 V, the drain current I_D increases slowly rather than abruptly. It reaches the steady-state value of -3.2 μA/μm after about 150 s at room temperature (and somewhat faster at higher temperature of $T = 310$ K [see Fig. 1(d)].

To understand the qualitative difference between dc scan and transient characteristics, we performed TCAD simulations with Synopsys Sentaurus. The carrier lifetime in the substrate was set to 0.1 ms and we used doping-dependent Schottky–Read–Hall (SRH) and electric field-dependent mobility [24], [25]. The simulation results reproduce the experimental results fairly well: I_D increases slowly after the applied V_{BG} pulse and saturates in about 100 s, as shown in Fig. 2(a).

To further document the physical mechanism, Fig. 2(b) compares the hole densities at $t = 2$ s right after the V_{BG} pulse, and at $t = 150$ s when I_D reaches saturation. A deep depletion region extending ~3 μm under the BOX is initially formed in the Si substrate due to the V_{BG} pulse. However, the depletion region shrinks as time passes and thermally generated electrons accumulate at the BOX/substrate interface and modify the hole distribution, as shown in the $t = 150$ s panel of Fig. 2(b). These accumulated electrons induce the same number of holes in the top Si channel as in a capacitor.

Fig. 2(c) shows the evolution of electron density at the BOX/substrate interface and hole density in the top Si channel. Clearly, the electron density at the bottom interface increases with time due to thermal generation. This causes a drop of effective potential at the BOX/substrate interface and thus increases the hole density and I_D in the top channel. At higher temperature, the thermal generation rate is more efficient; hence, I_D increases faster, as shown in Fig. 1(d). This transient effect has also been observed previously in pseudo-MOS and used to extract the carrier lifetime in SOI [26], [27].

III. Photodetection Application

The deep-depletion effect discussed above can be used for photodetection purposes in which light can accelerate the generation of electrons in the substrate. The responsivity and detection range are two important performance metrics for a photodetector. With high responsivity, the photodetector is sensitive to low light intensity, whereas the detection range defines the highest light intensity before the response saturates. Conventional photodetectors typically have a fixed responsivity and detection range [28], [29]. The ability to tune the responsivity and detection range is of great interest for a number of applications in optoelectronics [30]–[32].

In this section, we investigate the photoresponse of the device under various light intensities and present the responsivity and detection range. Further, we demonstrate how the responsivity and detection range can be tuned by varying the V_{BG} pulse properties.

A. Photoresponse and Definition of Metrics

A V_{BG} pulse train with anamplitude of -20 V, period of 20 ms, and duty ratio of 50% is applied when the device is subjected to light with various intensities from 0 (dark) to 29.2 μW/cm^2. The light is generated by a light-emitting diode (LED) with a center wavelength of 620 nm. LED light intensity is adjusted by a voltage regulator.

Fig. 3(a) shows the measured drain current waveforms. In the dark, pulsing V_{BG} from 0 down to -20 V leads to an $I_D \sim 1$ μA/μm that remains constant on the 10-ms time scale.

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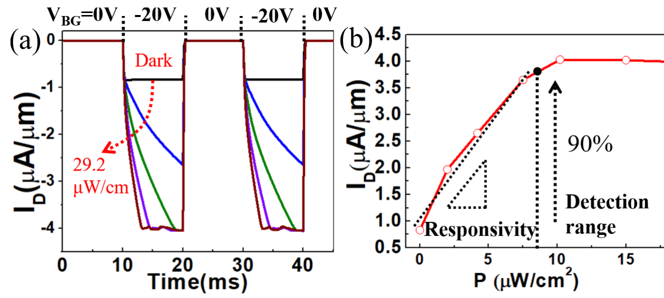

Fig. 3. (a) Response of I_D to V_{BG} pulses under various light illumination conditions. (b) Relation between peak I_D and light intensity.

However, when the device is illuminated, a sawtooth-like waveform is observed, in which the current increases during the $V_{BG} = -20$ V phase and then resets to the dark value as V_{BG} returns to zero. At higher light intensities, I_D exhibits a sharper increase during the V_{BG} pulse. Eventually, at sufficiently high light intensity, I_D saturates at $\sim 4\ \mu A/cm^2$ [see Fig. 3(b)].

The evolution of the current under various light intensities can be easily understood by considering the photogeneration in the substrate. As the $V_{BG} = -20$ V pulse is applied, the deep depletion region is formed in the substrate as explained above. Since the thermal generation rate is very low, a negligible number of electrons are generated during the 10 ms of applied V_{BG} at room temperature. Thus, the dark I_D does not change during the $V_{BG} = -20$ V phase. However, under illumination, the light absorbed by the Si substrate can generate photoelectrons that accumulate at the BOX/depleted substrate interface. These photoelectrons increase the drain current in the top Si channel, similar to the effect induced by thermally generated electrons discussed in Section II. Since the photogeneration rate is much faster than the thermal generation, I_D shows a significant increase even during a short 10-ms time period. At higher light intensities, the photogeneration rate is enhanced, resulting in an increasing drain current. However, when photoelectrons completely charge the BOX capacitor, the equilibrium state is reached and I_D saturates. The maximum photoelectron charge that the BOX capacitor can accommodate is approximately given by

$$Q_{ph} = \Delta V_{BG} \times C_{BOX} \quad (1)$$

where the ΔV_{BG} is the amplitude of the applied V_{BG} pulse and C_{BOX} is the BOX capacitance. After the V_{BG} is reset from -20 back to 0 V, the device is reset and all photoelectrons at the BOX/substrate interface are evacuated via the back-gate contact.

The peak I_D values under V_{BG} pulses in Fig. 3(a) can be used to represent the photoresponse of the device. In a real application, this can be done by a peak detector circuit [33]–[35]. The relation between the peak I_D and the light intensity is plotted in Fig. 3(b), from which the responsivity and detection range are extracted. The responsivity R is defined as

$$R = \frac{I_{photon}}{P \times A} \quad (2)$$

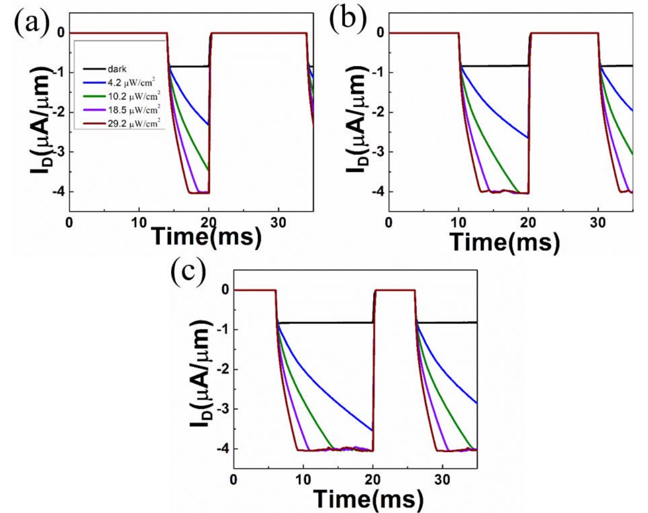

Fig. 4. Response of I_D after continuous $V_{BG} = -20$ V pulse train of 20-ms time period, in the dark (black) and under different light intensities. The duty ratio varies from (a) 30% to (b) 50% and (c) 70%.

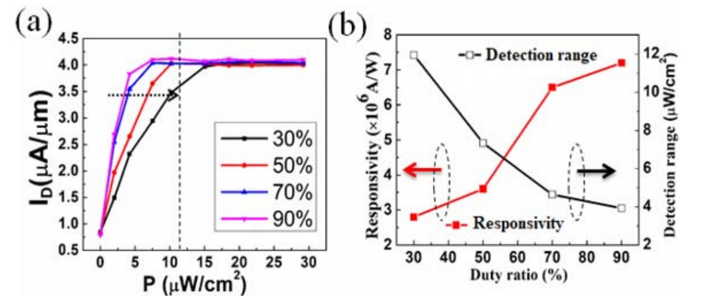

Fig. 5. (a) Evolution of I_D with light intensity as a function of duty ratio of V_{BG} pulse train. (b) Trade-off between responsivity and detection range for various duty ratios.

where the photocurrent I_{photon} is the difference in the drain current with and without the illumination, P is the light intensity, and A stands for the area of the device. It is extracted from the slope of the $I_D - P$ curve in Fig. 3(b) before I_D saturates. On the other hand, the detection range is defined as the light intensity, at which the I_D increases to over 90% of its full swing.

B. Impact of the Duty Ratio of V_{BG} Pulse

We have studied the effect of the V_{BG} duty ratio by applying continuous V_{BG} pulse trains with amplitude of -20 V, time period of 20 ms, and duty ratios varying from 30% to 70%. The corresponding I_D waveforms are shown in Fig. 4(a)–(c). Apparently, with a larger duty ratio, I_D reaches higher values under a fixed light intensity, whereas the saturation current value of $\sim 4\ \mu A/\mu m$ is unaffected.

The relationship between the peak I_D value and the corresponding light intensity is shown in Fig. 5(a). From the slope of I_D–P relation, the responsivity can be extracted: up to 2.9×10^6 A/W at a 30% duty ratio. The current saturates when the light intensity goes over 11.9 $\mu W/cm^2$. With a higher duty ratio of V_{BG} pulse, the responsivity is higher and exceeds 7.2×10^6 A/W for a duty ratio of 90%. However, there is trade-off, as I_D reaches the saturation limit earlier and

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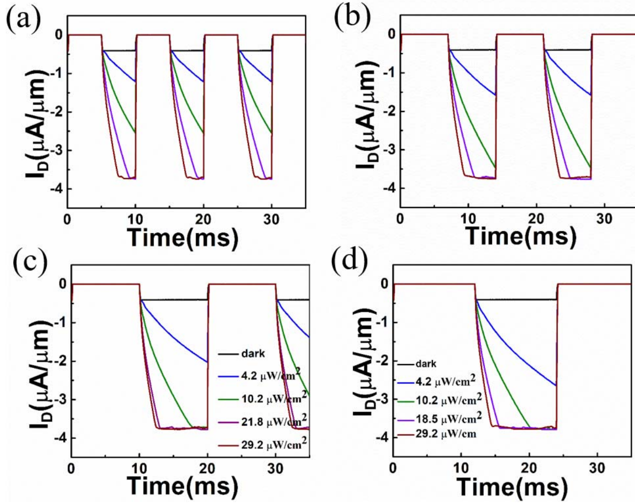

Fig. 6. Response of I_D to a continuous $V_{BG} = -20$ V pulse train of 50% duty ratio and under various light intensities. The period of V_{BG} pulse is (a) 10, (b) 14, (c) 20, and (d) 24 ms.

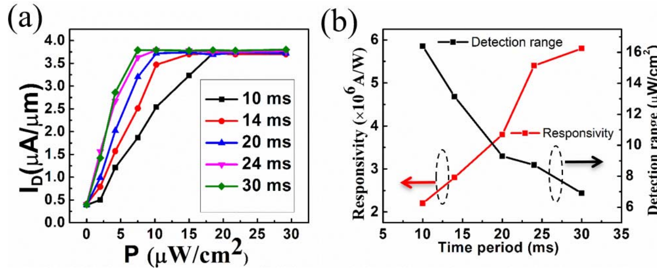

Fig. 7. (a) Peak output current versus the light intensity as a function of the time period of the V_{BG} pulse. (b) Compromise between responsivity and detection range in terms of time periods of V_{BG} pulse.

the detection range drops from 11.9 to around 3.9 μW/cm^2, as shown in Fig. 5(b).

With a higher duty ratio, the light can generate more photoelectrons before the reset of the device, which results in higher drain current. On the other hand, the detection range degrades with larger duty ratio since the maximum photoelectron capacity of (1) is reached with lower light intensity and longer exposure duration. Thus, the duty ratio of V_{BG} pulse paves a way to flexibly tune the compromise between responsivity and detection range.

C. Impact of the Time Period of V_{BG} Pulse

We further explore the responsivity and detection range by adjusting the time period of the applied V_{BG} pulse train. The duty ratio and amplitude of the V_{BG} pulses are fixed at 50% and -20 V, respectively. Fig. 6(a)–(c) shows the drain current transients for four different V_{BG} pulse periods of 10, 14, 20, and 24 ms, respectively. The corresponding I_D–P relations are compared in Fig. 7(a). With a longer V_{BG} period, I_D reaches a higher peak value, indicating higher responsivity.

The high responsivity comes at the cost of a degraded detection range. As summarized in Fig. 7(b), the responsivity increases from 2.2×10^6 to 5.8×10^6 A/W as the time period of V_{BG} increases from 10 to 30 ms. In contrast, the detection range degrades gradually from 16.4 to 6.9 μW/cm^2 against the increase of time period of V_{BG}. The impact of the V_{BG} pulse period on the responsivity and detection range arises from the change of the width of V_{BG} pulse. With a longer period at a fixed duty ratio, the width of V_{BG} pulse is increased, creating more photoelectrons before the reset. Thus, the responsivity rises and the detection range drops. Changing the V_{BG} pulse period provides an alternative way to flexibly tune the trade-off between responsivity and detection range.

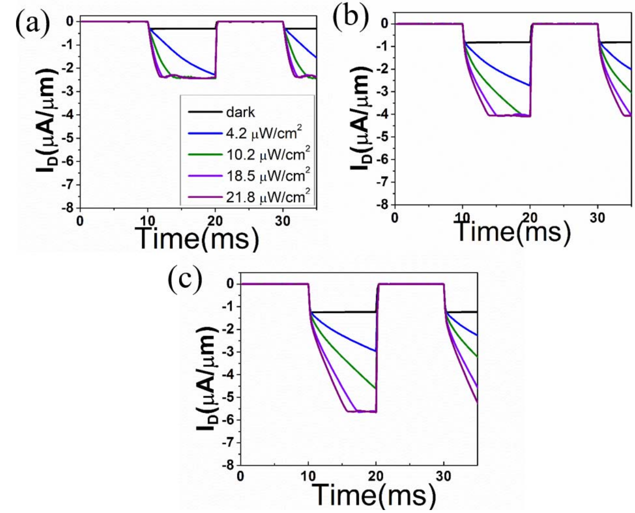

Fig. 8. Transient response of I_D to a continuous V_{BG} pulse train with fixed duty ratio of 50% and time period of 20 ms, under various light intensities. The V_{BG} pulse varies from (a) -10, (b) -20, and (c) -30 V.

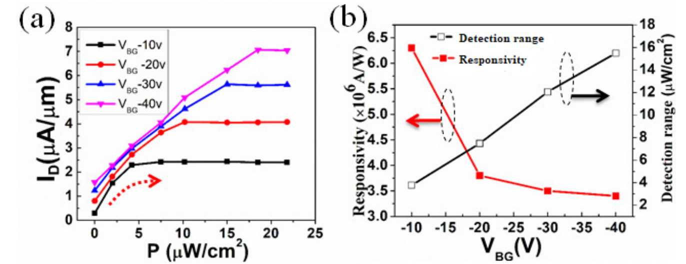

Fig. 9. (a) Maximum output current versus light intensity for various V_{BG} pulse amplitudes. (b) Responsivity and detection range versus V_{BG} pulse amplitude.

D. Impact of Pulse Amplitude

We have also measured the device as a function V_{BG} pulse amplitude, while keeping a fixed duty ratio of 50% and a time period of 20 ms. Fig. 8(a)–(c) presents the response of the device as a function of V_{BG} amplitude ranging from -10 to -30 V. The corresponding I_D–P relations are shown in Fig. 9(a): we find that I_D saturates earlier at lower V_{BG} amplitude, whereas the I_D–P curves before saturation almost coincide.

Fig. 9(b) demonstrates the impact of V_{BG} amplitude on the responsivity and detection range. The responsivity is almost constant for $V_{BG} = -20$ V or more negative, whereas the $V_{BG} = -10$ V pulse amplitude produces a very high responsivity rises up to 6.3×10^6 A/W. We attribute this to the fact that the device operates in the subthreshold region under low V_{BG}, making I_D very sensitive to changes in V_{BG}. The response of the device pulsed at $V_{BG} = -10$ V is nonlinear in light intensity [see Fig. 9(a)].

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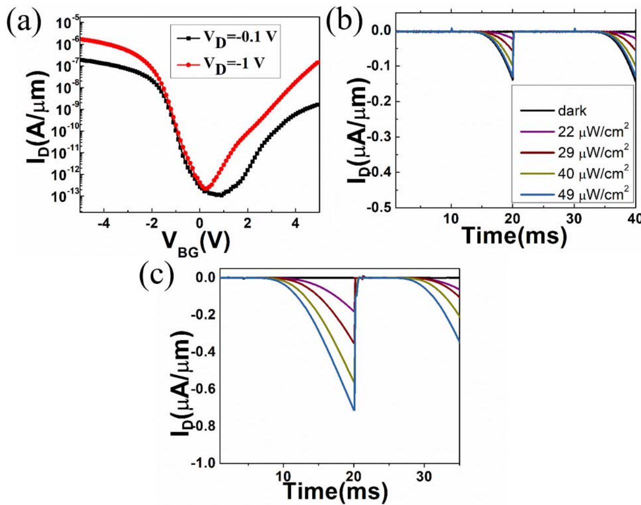

Fig. 10. (a) Static dc scan of drain current during the back-gate voltage sweep. (b) Evolution of I_D for a continuous $V_{BG} = -5$ V pulse train with 20-ms time period and duty ratio of 50% and (c) 90% under various light intensities.

With the reduction of V_{BG} pulse amplitude, the detection range is degraded from 15.45 to 3.77 μW/cm^2. This is mainly because the detection range is determined by the maximum charge that the BOX capacitor allows, which is proportional to the applied V_{BG} [see (1)]. However, there is no apparent change in responsivity because the duty ratio and period of V_{BG} pulse are fixed. The slope of I_D–P curve above the subthreshold region is approximately constant, indicating no apparent change in responsivity due to the fixed width of V_{BG} pulse train, creating the same number of photoelectrons before the reset of the device [see Fig. 9(a)]. The higher V_{BG} amplitude increases the number of maximum photoelectron charges that BOX capacitor can accommodate which results in the increase of detection range. Hence, the change of V_{BG} amplitude impacts on the detection range. However, the responsivity remains nearly constant above the subthreshold region [see Fig. 9(b)].

Since reducing the V_{BG} can seriously degrade the detection range of the photodetector and cause undesirable nonlinearity, further optimization of the device structure is needed.

IV. Optimization of the Device

The amplitude of $V_{BG} = -20$ V (or larger) pulses required for high sensitivity and detection range is undesirable for practical applications. In order to scale down V_{BG} without degrading the detection range, the key is to reduce the BOX thickness. With thinner BOX, the capacitance and its maximum stored charge limit can be increased even for lower V_{BG} pulses [see (1)]. To verify this, we fabricated a new set of devices in an advanced UTBB SOI substrate with 20-nm BOX and 12-nm top Si layer, using the same fabrication steps as described in Section II.

The I_D–V_{BG} dc characteristics of the fabricated device are shown in Fig. 10(a). The UTBB device is fully turned on by $V_{BG} = -5$ V, much lower than that required for 145-nm BOX devices of Fig. 1. Fig. 10(b) and (c) shows the transient measurements under various duty ratios of V_{BG} pulse from 50% to 90%, with the V_{BG} amplitude fixed at -5 V.

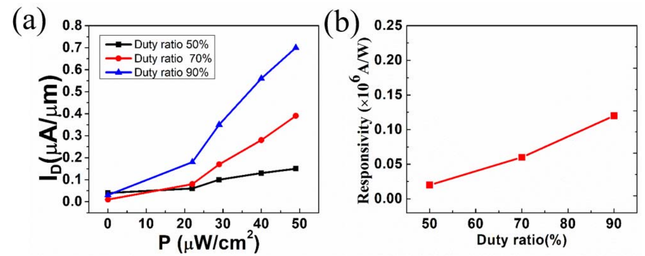

Fig. 11. (a) Peak values of output current versus light intensity as a function of duty ratio. (b) Plot of responsivity versus duty ratio.

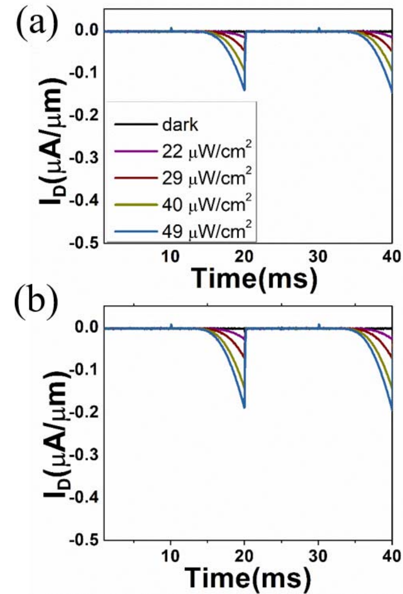

Fig. 12. Response of I_D to continuous V_{BG} pulse trains of amplitude (a) -4 and (b) -6 V, with a fixed duty ratio of 50% and a fixed time period of 20 ms, under various light intensities.

The responsivity increases with duty ratio and we find that at 90% duty ratio the current does not show any saturation at intensities up to 49 μW/cm^2, which is the upper limit of our LED light source.

The relation between the maximum I_D and the light intensity is shown in Fig. 11(a). The responsivity increases with duty ratio as summarized in Fig. 11(b). Due to the imperfect Schottky source/drain contacts, the ON-current and responsivity of the UTBB SOI device are lower than in Section III devices. However, the detection range is markedly improved under much lower applied V_{BG}.

The downscaling of V_{BG} is further explored by measuring the device under V_{BG} amplitudes of -4 and -6 V at a fixed duty ratio of 50% and time period of 20 ms, as shown in Fig. 12(a) and (b). The current does not show any sign of saturation even with V_{BG} pulse as low as -4 V. The I_D–P and responsivity versus V_{BG} relations are summarized in Fig. 13(a) and (b), respectively, and show almost the same responsivity under various V_{BG} amplitudes. Compared to the device with 145-nm BOX, the device with 20-nm BOX demonstrates successful operation with V_{BG} pulses of -4 V amplitude and the improvement in detection range to over 49 μW/cm^2.

To confirm the increased detection range with UTBB SOI structure, we performed the TCAD simulations, with fixed

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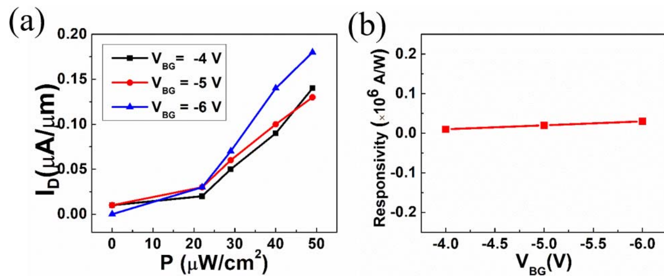

Fig. 13. (a) Maximum I_D current versus light intensity as a function of V_{BG} amplitude. (b) Plot of responsivity versus V_{BG} amplitude.

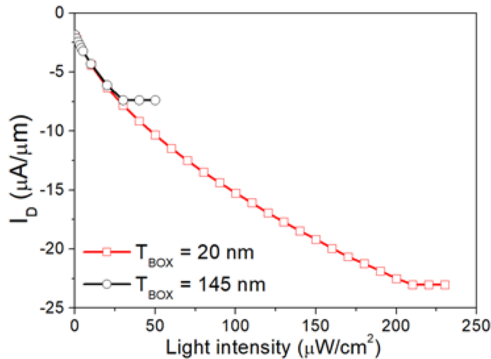

Fig. 14. TCAD simulation results showing enhancement of detection range with UTBB SOI structure. Comparison of I_D-light intensity relations between devices with BOX thicknesses of 145 and 20 nm.

$T_{si} = 6$ nm and two different BOX thicknesses (T and T nm) for comparison. The Si substrate is biased with a V_{BG} pulse from 0 to -5 V with a fixed drain voltage of -1 V. The relation between the peak I_D and the corresponding light intensity is shown in Fig. 14. The I_D saturates early in the device with 145-nm BOX, indicating a low detection range down to 30 μW/cm^2. However, the device with 20-nm BOX shows a very high detection range up to 210 μW/cm^2. The detection range is determined by the maximum charge that the BOX capacitor stores. This is proportional to the BOX capacitance (C_{BOX}), provided V_{BG} amplitude is fixed [see (1)]. At higher light intensities, the photogeneration rate is enhanced, resulting in an increasing drain current. However, as photoelectrons completely charge the BOX capacitor, the equilibrium state is reached and I_D saturates. Thus, an optimized device structure, with advanced UTBB SOI technology dramatically improves the detection range with low operation voltage.

V. Conclusion

An investigation of the transient effect in SOI substrates under back-gate pulsing has been carried out experimentally and confirmed by TCAD simulation. This transient effect is induced by the V_{BG}-created deep-depletion region in the substrate. Electrons generated in this region by slow thermal generation accumulate in the BOX/substrate interface and result in the gradual increase of I_D. Given the near-instantaneous photogeneration of electrons under illumination, this deep-depletion effect can be exploited for photodetection by using a V_{BG} pulse train. The peak drain current increases almost linearly with the light intensity before saturation. We have studied the impact of various duty ratios, time periods, and amplitude of V_{BG} pulses on the trade-off between responsivity and detection range. A higher duty ratio and a longer time period are both helpful to improve the responsivity, reaching values as high as 7.3×10^6 A/W, albeit with a degraded detection range. Operation at lower V_{BG} has been demonstrated by using advanced UTBB SOI with thinner BOX. Device operation with V_{BG} down to -4 V and a remarkable detection range of over 49 μW/cm^2 have been demonstrated. A crucial property for practical applications is the tunability of the responsivity and detection range. This device concept can be adapted to fully processed MOSFETs with underlapped top gate.

References

[1] C. Sun *et al.*, "A 45 nm CMOS-SOI monolithic photonics platform with bit-statistics-based resonant microring thermal tuning," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 893–907, Apr. 2016, doi: 10.1109/JSSC.2016.2519390.

[2] W. Zhang, M. Chan, S. K. H. Fung, and P. K. Ko, "Performance of a CMOS compatible lateral bipolar photodetector on SOI substrate," *IEEE Electron Device Lett.*, vol. 19, no. 11, pp. 435–437, Nov. 1998, doi: 10.1109/55.728904.

[3] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling," *Solid-State Electron.*, vols. 65–66, pp. 226–233, Nov. 2011, doi: 10.1016/j.sse.2011.06.012.

[4] R. Taco, I. Levi, A. Fish, and M. Lanuzza, "Exploring back biasing opportunities in 28 nm UTBB FD-SOI technology for subthreshold digital design," in *Proc. IEEE 28th Conv. Electr. Electron. Eng. Isr. (IEEEI)*, Dec. 2014, pp. 1–4, doi: 10.1109/EEEI.2014.7005822.

[5] H. Yamamoto, K. Taniguchi, and C. Hamaguchi, "High-sensitivity SOI MOS photodetector with self-amplification," *Jpn. J. Appl. Phys.*, vol. 35, no. 2S, p. 1382, 1996, doi: 10.1143/JJAP.35.1382.

[6] S. Cristoloveanu, "Introduction to silicon on insulator materials and devices," *Microelectron. Eng.*, vol. 39, nos. 1–4, pp. 145–154, 1997, doi: 10.1016/S0167-9317(97)00172-X.

[7] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 179–181, Feb. 2012, doi: 10.1109/LED.2011.2176908.

[8] N. Abdo, D. Sallin, A. Koukab, M. Estribeau, P. Magnan, and M. Kayal, "Silicon-on-insulator technology for imaging and application to a switching photodetector," *Int. J. Microelectron. Comput. Sci.*, vol. 6, no. 4, pp. 136–141, 2015.

[9] M. Horstmann *et al.*, "Advanced SOI CMOS transistor technologies for high-performance microprocessor applications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 149–152, doi: 10.1109/CICC.2009.5280865.

[10] H. Inokawa, H. Satoh, and T. Ueta, "Highly sensitive and functional photodetectors based on silicon-on-insulator," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Aug. 2016, pp. 452–455, doi: 10.1109/EDSSC.2016.7785305.

[11] J. Wang, M. Yu, G. Lo, D.-L. Kwong, and S. Lee, "Silicon waveguide integrated germanium JFET photodetector with improved speed performance," *IEEE Photon. Technol. Lett.*, vol. 23, no. 12, pp. 765–767, Jun. 2011, doi: 10.1109/LPT.2011.2132794.

[12] G. Li *et al.*, "Silicon-on-insulator photodiode on micro-hotplate platform with improved responsivity and high-temperature application," *IEEE Sensors J.*, vol. 16, no. 9, pp. 3017–3024, May 2016, doi: 10.1109/JSEN.2016.2530020.

[13] S. Sahni, X. Luo, J. Liu, Y.-H. Xie, and E. Yablonovitch, "Junction field-effect-transistor-based germanium photodetector on silicon-on-insulator," *Opt. Lett.*, vol. 33, no. 10, pp. 1138–1140, 2008, doi: 10.1364/OL.33.001138.

[14] L. Kadura *et al.*, "Extending the functionality of FDSOI N- and P-FETs to light sensing," in *IEDM Tech. Dig.*, Dec. 2016, pp. 32.6.1–32.6.4, doi: 10.1109/IEDM.2016.7838530.

[15] G. Li, K. Maekita, H. Mitsuno, T. Maruyama, and K. Iiyama, "Over 10 GHz lateral silicon photodetector fabricated on silicon-on-insulator substrate by CMOS-compatible process," *Jpn. J. Appl. Phys.*, vol. 54, no. 4S, Mar. 2015, Art. no. 04DG06, doi: 10.7567/JJAP.54.04DG06.

[16] C. Xu, W. Zhang, and M. Chan, "A low voltage hybrid bulk/SOI CMOS active pixel image sensor," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 248–250, May 2001, doi: 10.1109/55.919244.

Authorized licensed use limited to: Brown University. Downloaded on August 15,2020 at 16:33:05 UTC from IEEE Xplore. Restrictions apply.

[17] W. Zhang, M. Chan, and P. K. Ko, "Performance of the floating gate/body tied NMOSFET photodetector on SOI substrate," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1375–1384, Jul. 2000, doi: 10.1109/16.848280.

[18] G. Li, Y. Zeng, W. Hu, and Y. Xia, "Analysis and simulation for current–voltage models of thin-film gated SOI lateral PIN photodetectors," *Optik*, vol. 125, no. 1, pp. 540–544, Jan. 2014, doi: 10.1016/j.ijleo.2013.07.030.

[19] R. A. Katia Sasaki, R. C. Rangel, L. S. Yojo, and J. A. Martino, "Third generation BESOI (back-enhanced SOI) pMOSFET fabricated on UTBB wafer," in *Proc. 34th Symp. Microelectron. Technol. Devices (SBMicro)*, Aug. 2019, pp. 1–4, doi: 10.1109/SBMicro.2019.8919335.

[20] J. Deng *et al.*, "Interface coupled photodetector (ICPD) with high photoresponsivity based on silicon-on-insulator substrate (SOI)," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 557–564, 2018, doi: 10.1109/JEDS.2017.2788403.

[21] X.-Y. Cao *et al.*, "An SOI photodetector with field-induced embedded diode showing high responsivity and tunable response spectrum by backgate," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5412–5418, Dec. 2018, doi: 10.1109/TED.2018.2876137.

[22] W. Van Den Daele, C. Malaquin, N. Baumel, O. Kononchuk, and S. Cristoloveanu, "Adaptation of the pseudo-metal–oxide–semiconductor field effect transistor technique to ultrathin silicon–on-insulator wafers characterization: Improved set-up, measurement procedure, parameter extraction, and modeling," *J. Appl. Phys.*, vol. 114, no. 16, Oct. 2013, Art. no. 164502, doi: 10.1063/1.4826631.

[23] I. Ionica *et al.*, "Advances in the pseudo-MOSFET characterization method," in *Proc. CAS Proc. (Int. Semiconductor Conf.)*, vol. 1, Oct. 2010, pp. 45–51, doi: 10.1109/SMICND.2010.5650923.

[24] V. Tilak, K. Matocha, and G. Dunne, "Electron-scattering mechanisms in heavily doped silicon carbide MOSFET inversion layers," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2823–2829, Nov. 2007, doi: 10.1109/TED.2007.906929.

[25] S. Cristoloveanu, D. Munteanu, and M. S. T. Liu, "A review of the pseudo-MOS transistor in SOI wafers: Operation, parameter extraction, and applications," *IEEE Trans. Electron Devices*, vol. 47, no. 5, pp. 1018–1027, May 2000, doi: 10.1109/16.841236.

[26] S. Cristoloveanu and T. Elewa, "Model for carrier lifetime extraction from pseudo-MOSFET transients," *Electron. Lett.*, vol. 32, no. 21, pp. 2021–2023, Oct. 2002, doi: 10.1049/el:19961319.

[27] T. Elewa, H. Haddar, and S. Cristoloveanu, "Carrier generation and trapping properties in SIMOX structures," in *Proc. 17th Eur. Solid State Device Res. Conf. (ESSDERC)*, Sep. 1987, pp. 529–532.

[28] W. N. Ye and Y. Xiong, "Review of silicon photonics: History and recent advances," *J. Modern Opt.*, vol. 60, no. 16, pp. 1299–1320, Sep. 2013, doi: 10.1080/09500340.2013.839836.

[29] L. Shi and S. Nihtianov, "Comparative study of silicon-based ultraviolet photodetectors," *IEEE Sensors J.*, vol. 12, no. 7, pp. 2453–2459, Jul. 2012, doi: 10.1109/JSEN.2012.2192103.

[30] S. Liu *et al.*, "Tunable hybrid photodetectors with superhigh responsivity," *Small*, vol. 5, no. 21, pp. 2371–2376, Nov. 2009, doi: 10.1002/smll.200900576.

[31] H. Xu, J. Wu, Q. Feng, N. Mao, C. Wang, and J. Zhang, "High responsivity and gate tunable graphene-MoS_2 hybrid phototransistor," *Small*, vol. 10, no. 11, pp. 2300–2306, Jun. 2014, doi: 10.1002/smll.201303670.

[32] K. Thakar, B. Mukherjee, S. Grover, N. Kaushik, M. Deshmukh, and S. Lodha, "Multilayer ReS_2 photodetectors with gate tunability for high responsivity and high-speed applications," *ACS Appl. Mater. Interface*, vol. 10, no. 42, pp. 36512–36522, Oct. 2018, doi: 10.1021/acsami.8b11248.

[33] P. B. Petrović, "A new tunable current-mode peak detector," *Microelectron. J.*, vol. 45, no. 6, pp. 805–814, Jun. 2014, doi: 10.1016/j.mejo.2014.02.019.

[34] M. W. Kruiskamp and D. M. W. Leenaerts, "A CMOS peak detect sample and hold circuit," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 1, pp. 295–298, 1994, doi: 10.1109/23.281513.

[35] K. Koli and K. Halonen, "Low voltage MOS-transistor-only precision current peak detector with signal independent discharge time constant," in *Proc. IEEE Int. Symp. Circuits Systems. Circuits Syst. Inf. Age (ISCAS)*, vol. 3, Jun. 1997, pp. 1992–1995, doi: 10.1109/ISCAS.1997.621544.

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